

# M62358P,FP

## 8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

### DESCRIPTION

The M62358 is a 12-channel 8-bit voltage output digital to analog converter.

The M62358 includes data latch circuit and gain change circuit of output amplifiers.

Input data is a easy-to-use three-wires serial interface.It is able to cascading serial use with Do terminal.

Gain set up data change a case the each channel's output voltage range is change ,and each channel's output voltage range is able to change severally make use of gain set up data.

### FEATURES

- All channel includes gain change latch circuit with output amplifiers.
- 14-bit serial data input
- Built-in reset circuit

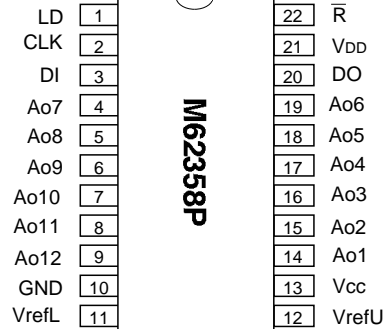
### APPLICATION

Conversion from digital control data to analog control data for home-use and industrial equipment.

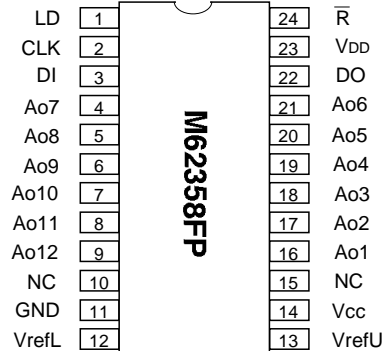
Automatic adjustment by combination with EEPROM and microcomputer(replacement of conventional half-fixed resistor).

Signal gain control of DISPLAY-MONITOR or CTV.

### PIN CONFIGURATION (TOP VIEW)



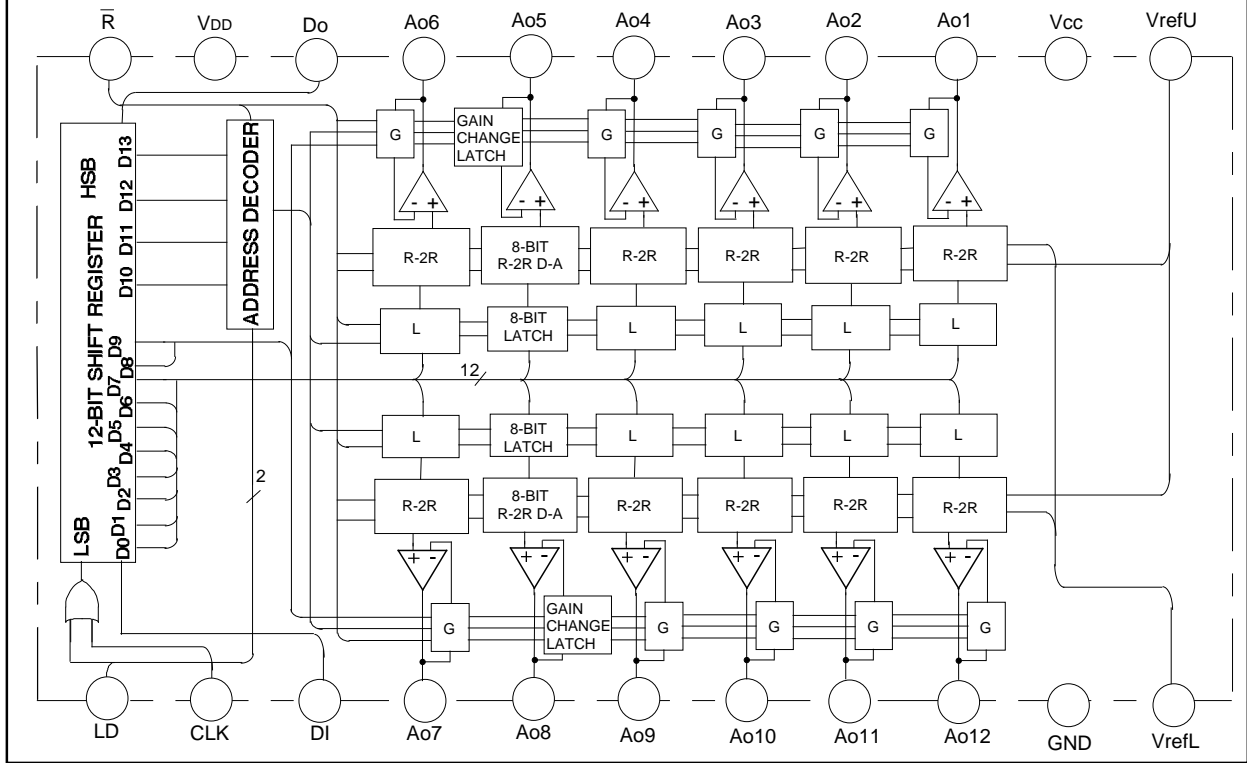
Outline 22P4H



Outline 24P2-E

NC:NO CONNECTION

### BLOCK DIAGRAM



**M62358P,FP****8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS****EXPLANATION OF TERMINALS**

Pin No.	Symbol	Function
③	DI	Serial data input terminal
⑳	DO	Serial data output terminal
②	CLK	Serial clock input terminal
①	LD	LD terminal input high level than latch circuit data load *1
⑳	V <sub>DD</sub>	Digital power supply terminal
⑬	V <sub>CC</sub>	Analog power supply terminal
⑩	GND	Digital and Analog common GND
⑫	V <sub>refU</sub>	D-A converter high level reference voltage input terminal
⑪	V <sub>refL</sub>	D-A converter low level reference voltage input terminal
⑳	$\bar{R}$	Reset terminal
⑭	Ao1	8-bit D-A converter output terminal
⑮	Ao2	
⑯	Ao3	
⑰	Ao4	
⑱	Ao5	
⑲	Ao6	
④	Ao7	
⑤	Ao8	
⑥	Ao9	
⑦	Ao10	
⑧	Ao11	
⑨	Ao12	

\*1 When the LD terminal is "H" input data has load.

**ABSOLUTE MAXIMUM RATINGS**(T<sub>a</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.3~13.5	V
V <sub>DD</sub>	Supply voltage		-0.3~7	V
V <sub>refU</sub>	D-A converter high level reference voltage		V <sub>DD</sub>	V
V <sub>IN</sub>	Input voltage		-0.3~V <sub>DD</sub> +0.3	V
I <sub>DO</sub>	Output current		-5~+5	mA
I <sub>AO</sub>	Buffer amplifier output current range		-5~+5	mA
T <sub>opr</sub>	Operating temperature		-20~+85	°C
T <sub>stg</sub>	Storage temperature		-40~+125	°C

**RECOMMENDED OPERATING CONDITIONS**

- Digital supply voltage V<sub>DD</sub> 5V±10%
- Analog supply voltage V<sub>CC</sub> V<sub>DD</sub>-13V

**ELECTRICAL CHARACTERISTICS**

**Digital part**(V<sub>CC</sub>=13V, V<sub>DD</sub>=V<sub>refU</sub>=5V, T<sub>a</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>DD</sub>	Supply voltage		4.5		5.5	V
I <sub>DD</sub>	Circuit current	CLK=1MHz in action			1	mA
V <sub>IL</sub>	Input low voltage				0.2V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage		0.8V <sub>DD</sub>			V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> =1.0mA			0.4	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> =-400μA	V <sub>DD</sub> -0.4			V

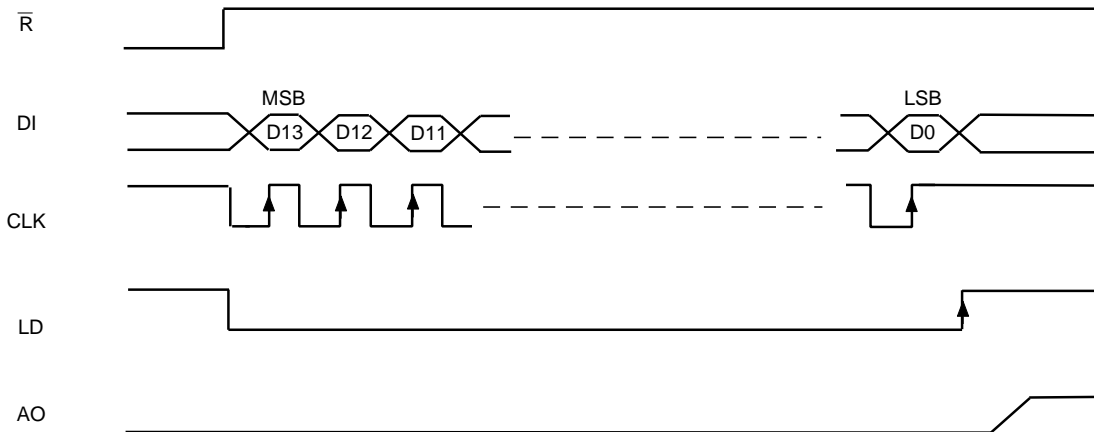
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## 8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

Analog part ( $V_{CC}=13V, V_{DD}=V_{refU}=5V, T_a=-20^{\circ}C \sim +85^{\circ}C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{CC}$	Supply voltage		$V_{DD}$		13	V
$I_{CC}$	Circuit current			3	6	mA
$I_{refU}$	D-A converter high level reference input current	All ch's set up at 107/256		2	4	mA
$V_{refU}$	D-A converter high level reference voltage range		3.5		$V_{DD}$	V
$V_{refL}$	D-A converter low level reference voltage range		0		1.5	V
$V_{AO}$	D-A converter output voltage range	$I_{AO} = \pm 500\mu A$	0.1		$V_{CC}-0.1$	V
		$I_{AO} = \pm 1mA$	0.2		$V_{CC}-0.2$	
$I_{AO}$	Buffer amplifier output current range				$\pm 2.5$	mA
DNL	Differential nonlinearity	Guaranteed monotonic	-1.0		1.0	LSB
NL	Nonrinality		-1.5		1.5	LSB
EZ	Zero code error	$V_{refU}=4.79V$	-2		2	LSB
EF	Full scale error	$V_{refL}=0.95V$ without load	-2		2	LSB
$E_o$	Gain error		-3		3	%
SR	Output slew rate			0.2		V/ $\mu s$

### TIMING CHART (MODEL)



Input data is carried out LD signal Low besides CLK signal positive edge.  
CLK,LD is keep generally High level.

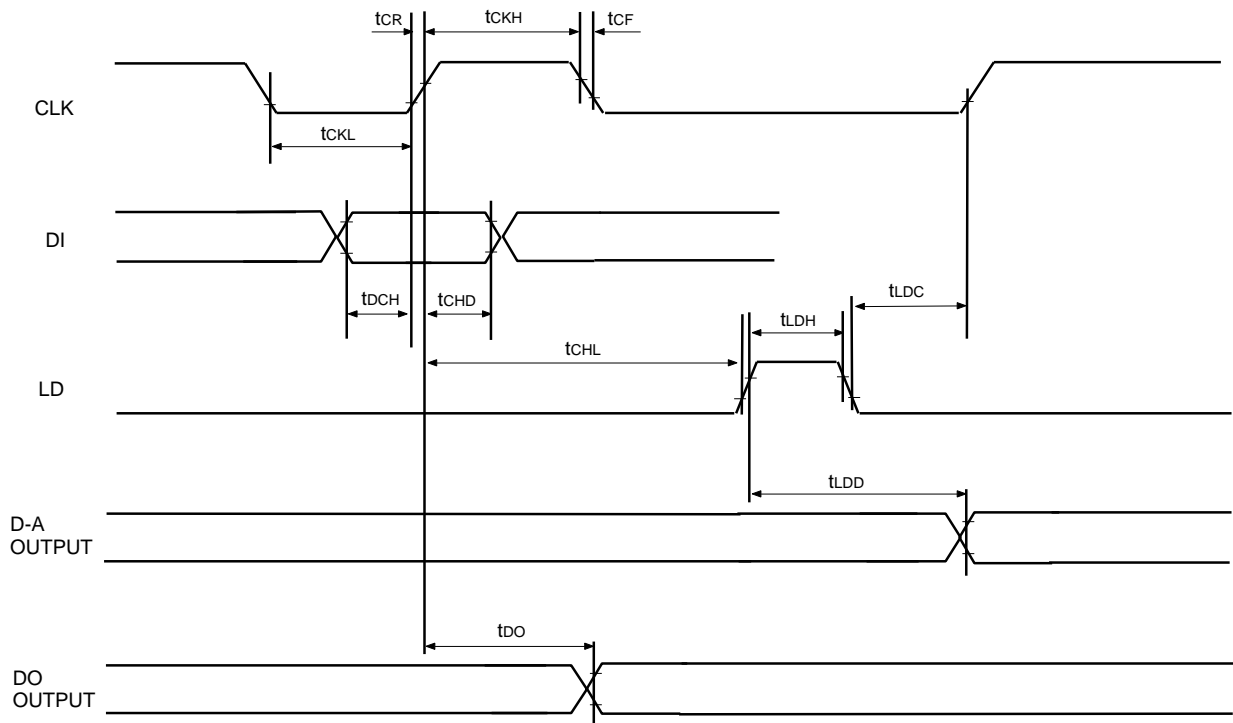
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## 8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

**AC CHARACTERISTICS**( $T_a=-20\sim 85^{\circ}\text{C}$ ,  $V_{cc}=13\text{V}$ ,  $V_{DD}=V_{refU}=5\text{V}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>CKL</sub>	Clock "L" pulse width		200			ns
t <sub>CKH</sub>	Clock "H" pulse width		200			ns
t <sub>CR</sub>	Clock rise time				200	ns
t <sub>CF</sub>	Clock fall time				200	ns
t <sub>DCH</sub>	Data set up time		60			ns
t <sub>CHD</sub>	Data hold time		100			ns
t <sub>CHL</sub>	LD setup time		200			ns
t <sub>LDC</sub>	LD hold time		100			ns
t <sub>LDH</sub>	LD "H" pulse width		100			ns
t <sub>DO</sub>	Data output delay time	$C_L=100\text{pF}$	70		350	ns
t <sub>LDD</sub>	D-A output setting time	Without load			300	$\mu\text{s}$

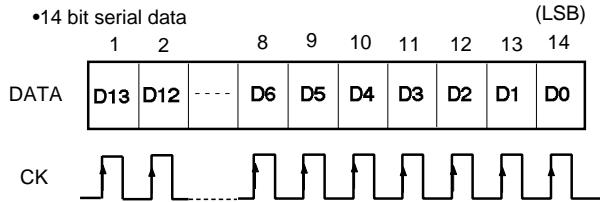
### TIMING CHART



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## 8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

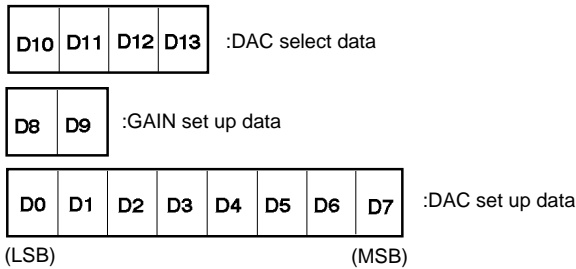
### DIGITAL FORMAT



•DAC select data

D10	D11	D12	D13	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2 selection
0	0	1	1	Ao3 selection
0	1	0	0	Ao4 selection
0	1	0	1	Ao5 selection
0	1	1	0	Ao6 selection
0	1	1	1	Ao7 selection
1	0	0	0	Ao8 selection
1	0	0	1	Ao9 selection
1	0	1	0	Ao10 selection
1	0	1	1	Ao11 selection
1	1	0	0	Ao12 selection
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

•Data assignment



•GAIN set up data

D8	D9	K	DAC output range (VrefU=5V,VrefL=0V)
0	0	1	0~5V
1	0	1.6	0~8V
0	1	1.8	0~9V
1	1	2.4	0~12V

•DAC set up data

(LSB)							(MSB)	DAC voltage
D0	D2	D3	D4	D5	D6	D7		
0	0	0	0	0	0	0	$1/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
1	0	0	0	0	0	0	$2/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
0	0	0	0	0	0	0	$3/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
1	0	0	0	0	0	0	$4/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0	1	1	1	1	1	1	$255/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
1	1	1	1	1	1	1	$256/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	

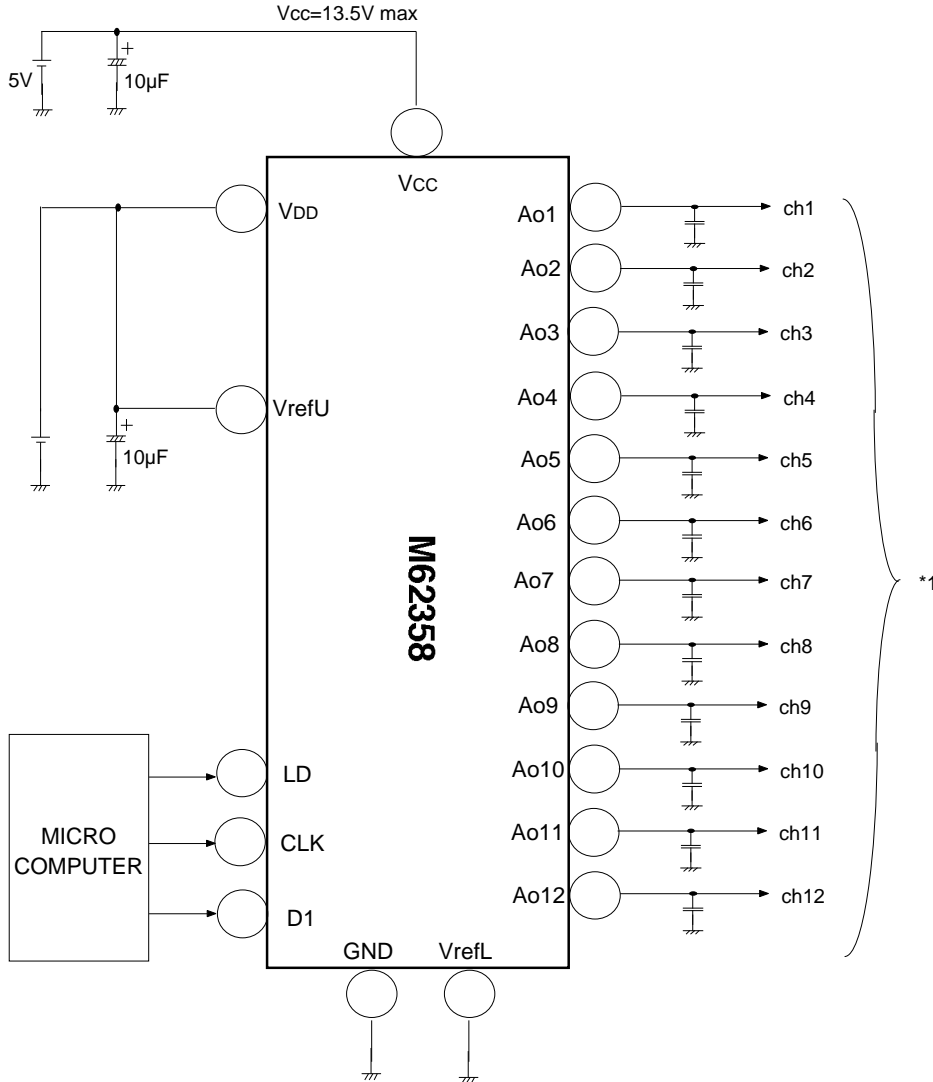
$$A_o = \frac{2^0 \times D_0 + 2^1 \times D_1 + 2^2 \times D_2 + \dots + 2^6 \times D_6 + 2^7 \times D_7 + 1}{256} \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$$

K: Amplifiers gain

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### APPLICATION CIRCUIT



This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when connect capacitor among output to GND for every noise eliminate.

\*1 If be used in a cathode-ray tube sets and high voltage sets, please connect capacitor among output to GND, about 0.1µF~1µF, because keep off effect of spark and electric discharge etc.