M62359P,FP

8-BIT 8CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62359 is a 8-channel 8-bit voltage output digital to analog converter.
The M62359 includes data latch circuit and gain change circuit of output amplifiers.
Input data is a easy-to-use three-wires serial interface.
It is able to cascading serial use with Do terminal.
Gain set up data change a case the each channel`s output voltage range is change ,and each channel`s output voltage range is able to change severally make use of gain set up data.

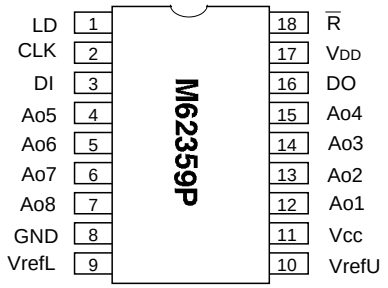
FEATURES

- All channel includes gain change latch circuit with output amplifiers.
- 14-bit serial data input
- Built-in reset circuit

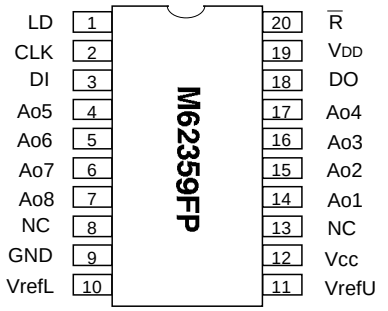
APPLICATION

Conversion from digital control data to analog control data for home-use and industrial equipment.
Automatic adjustment by combination with EEPROM and microcomputer(replacement of conventional half-fixed resistor).
Signal gain control of DISPLAY-MONITOR or CTV.

PIN CONFIGURATION (TOP VIEW)



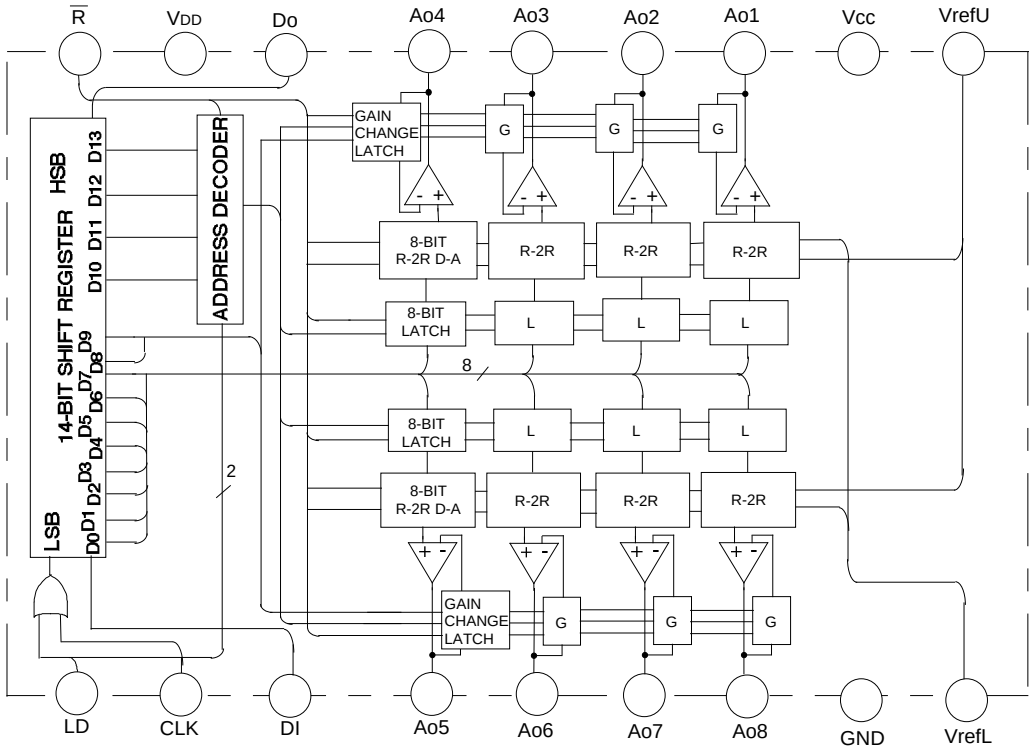
Outline 18P4



Outline 20P2N-A

NC:NO CONNECTION

BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
③	DI	Serial data input terminal
⑯	DO	Serial data output terminal
②	CLK	Serial clock input terminal
①	LD	LD terminal input high level than latch circuit data load *1
⑰	V_{DD}	Digital power supply terminal
⑪	Vcc	Analog power supply terminal
⑧	GND	Digital and Analog common GND
⑩	VrefU	D-A converter high level reference voltage input terminal
⑨	VrefL	D-A converter low level reference voltage input terminal
⑱	$\overline{R}$	Reset terminal
⑫	Ao1	8-bit D-A converter output terminal
⑬	Ao2	
⑭	Ao3	
⑮	Ao4	
④	Ao5	
⑤	Ao6	
⑥	Ao7	
⑦	Ao8	

*1 When the LD terminal is "H" input data has load.

ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~13.5	V
V_{DD}	Supply voltage		-0.3~7	V
V_{refU}	D-A converter high level reference voltage		V_{DD}	V
V_{IN}	Input voltage		-0.3~V_{DD}+0.3	V
I_{DO}	Output current		-5~+5	mA
I_{AO}	Buffer amplifier output current range		-5~+5	mA
T_{opr}	Operating temperature		-20~+85	℃
T_{stg}	Storage temperature		-40~+125	℃

RECOMMENDED OPERATING CONDITIONS

•Digital supply voltage V_{DD} 5V±10%

•Analog supply voltage Vcc V_{DD}~13V

ELECTRICAL CHARACTERISTICS

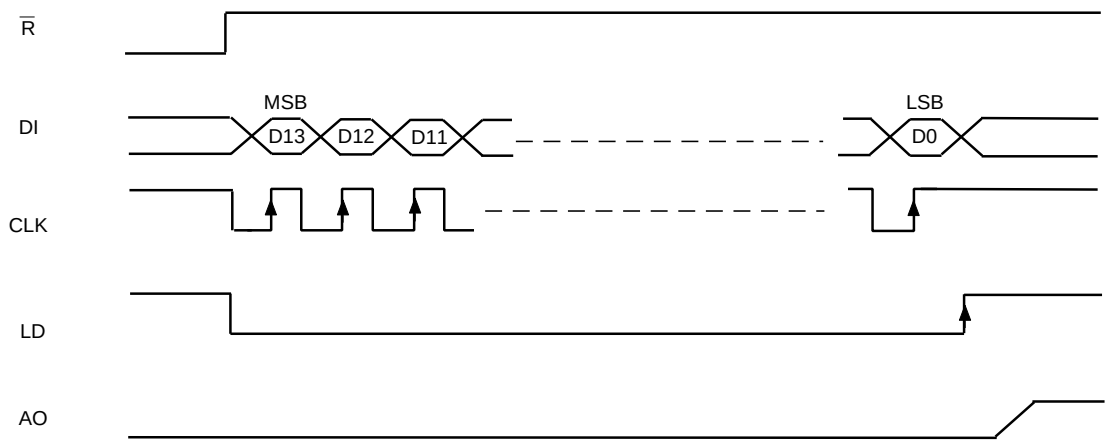
Digital part(Vcc=13V,V_{DD}=VrefU=5V, Ta=-25 to +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.5		5.5	V
I_{DD}	Circuit current	CLK=1MHz in action			1	mA
V_{IL}	Input low voltage				0.2V_{DD}	V
V_{IH}	Input high voltage		0.8V_{DD}			V
V_{OL}	Output low voltage	I_{OL}=1.0mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-400μA	V_{DD}-0.4			V

Analog part(Vcc=13V,V_{DD}=VrefU=5V,Ta=-20°C~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		V_{DD}		13	V
Icc	Circuit current			2	4	mA
IrefU	D-A converter high level reference input current	All ch's set up at 107/256		1.2	2.5	mA
V_{refU}	D-A converter high level reference voltage range		3.5		V_{DD}	V
V_{refL}	D-A converter low level reference voltage range		0		1.5	V
V_{AO}	D-A converter output voltage range	I_{AO} =±500µA	0.1		Vcc-0.1	V
		I_{AO} =±1mA	0.2		Vcc-0.2	
I_{AO}	Buffer amplifier output current range				±2.5	mA
DNL	Differential nonlinearity	Guaranteed monotonic	-1.0		1.0	LSB
NL	Nonrineality		-1.5		1.5	LSB
EZ	Zero code error	VrefU=4.79V VrefL=0.95V without load	-2		2	LSB
EF	Full scale error		-2		2	LSB
Eo	Gain error		-3		3	%
SR	Output slew rate			0.2		V/µs

TIMING CHART (MODEL)

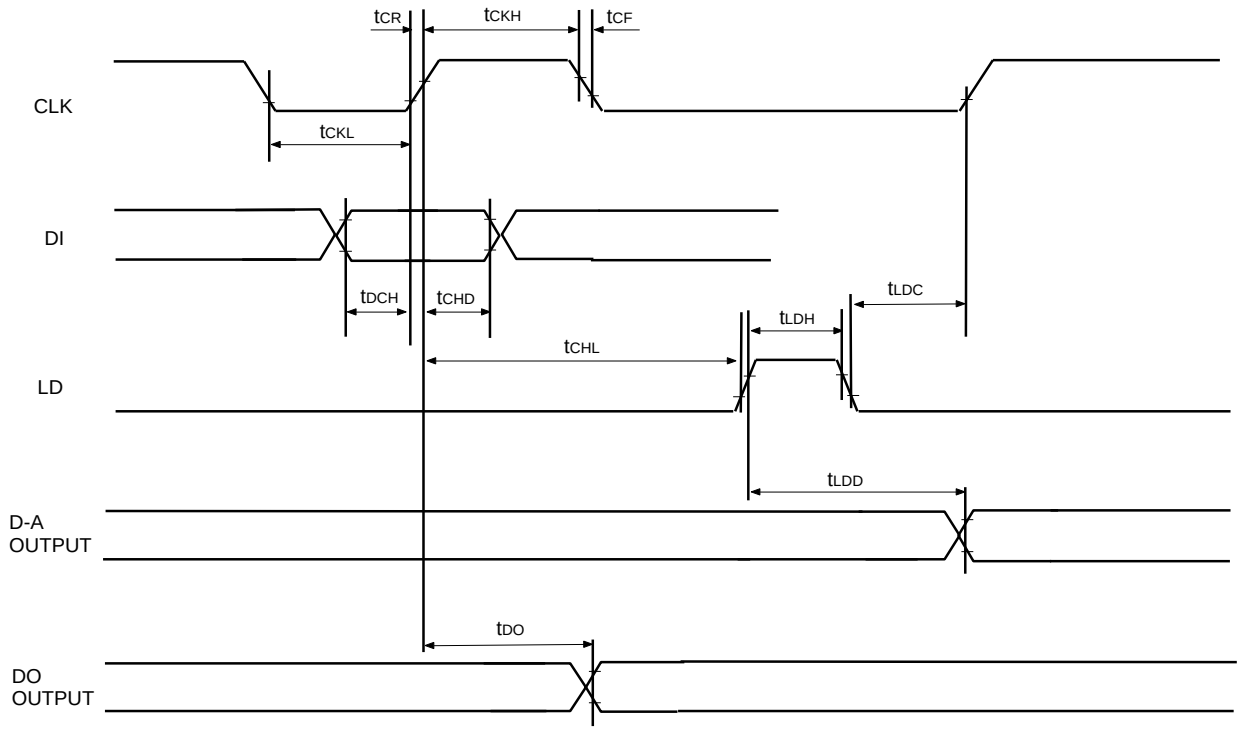


Input data is carried out LD signal Low besides CLK signal positive edge.
CLK,LD is keep generally High level.

AC CHARACTERISTICS(Ta=25°C,V_{CC}=13V,V_{DD}=VrefU=5V,VrefL=0V,unless otherwise noted)

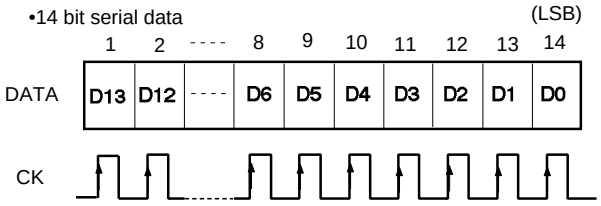
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CKL}	Clock "L"pulse width		200			ns
t_{CKH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data set up time		60			ns
t_{CHD}	Data hold time		100			ns
t_{CHL}	LD setup time		200			ns
t_{LDC}	LD hold time		100			ns
t_{LDH}	LD "H" pulse width		100			ns
t_{DO}	Data output delay time	C_L=100pF	70		350	ns
t_{LDD}	Data output setting time	Without load			300	µs

TIMING CHART

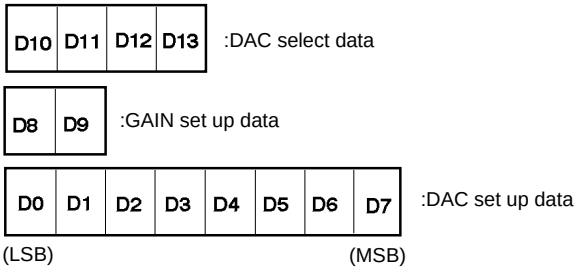


DIGITAL FORMAT

•14 bit serial data



•Data assignment



•DAC select data

D10	D11	D12	D13	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2 selection
0	0	1	1	Ao3 selection
0	1	0	0	Ao4 selection
0	1	0	1	Ao5 selection
0	1	1	0	Ao6 selection
0	1	1	1	Ao7 selection
1	0	0	0	Ao8 selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

•GAIN set up data

D8	D9	K	DAC output range (VrefU=5V,VrefL=0V)
0	0	1	0~5V
1	0	1.6	0~8V
0	1	1.8	0~9V
1	1	2.4	0~12V

•DAC set up data

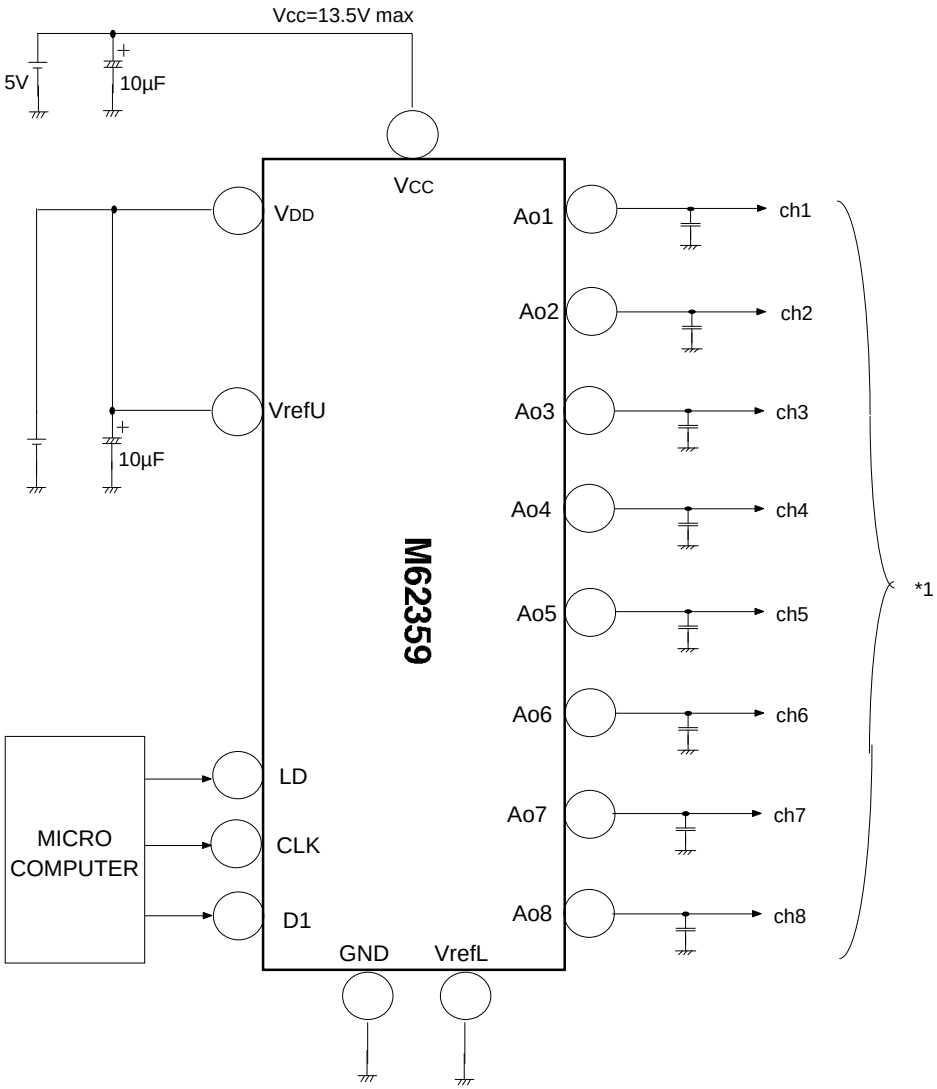
(LSB) (MSB)

D0	D2	D3	D4	D5	D6	D7	DAC voltage
0	0	0	0	0	0	0	1/256•(VrefU-VrefL) •K +VrefL
1	0	0	0	0	0	0	2/256•(VrefU-VrefL) •K +VrefL
0	0	0	0	0	0	0	3/256•(VrefU-VrefL) •K +VrefL
1	0	0	0	0	0	0	4/256•(VrefU-VrefL) •K +VrefL
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	255/256•(VrefU-VrefL) •K +VrefL
1	1	1	1	1	1	1	256/256•(VrefU-VrefL) •K +VrefL

$$Ao = \frac{2^0 X\ D0 + 2^1 X\ D1 + 2^2 X\ D2 + \cdots\cdots + 2^6 X\ D6 + 2^7 X\ D7 + 1}{256} \bullet (VrefU - VrefL) \bullet K + VrefL$$

K:Amplifiers gain

APPLICATION CIRCUIT



This IC`s output amplifier has an advantage to capacitive load.So it`s no problem at device action when connect capacitor among output to GND for every noise eliminate.

*1 If be used in a cathode-ray tube sets and high voltage sets,please connect capacitor among output to GND,about 0.1µF~1µF,because keep off effect of spark and electric discharge etc.