

## HAT2265H

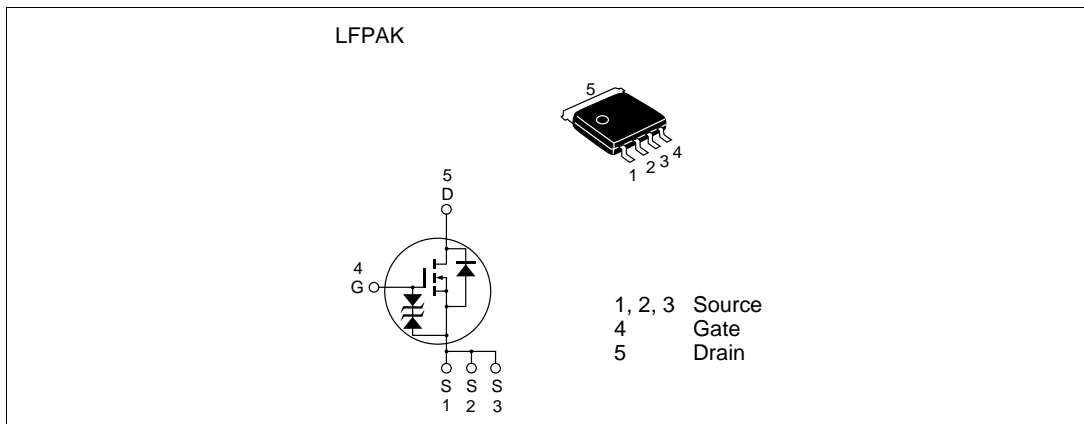
Silicon N Channel Power MOS FET Power Switching

Rev.0.00  
Sept.2004

### Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 2.5 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )
- Lead Free

### Outline



## HAT2265H

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### Absolute Maximum Ratings

(T<sub>a</sub> = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	30	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	55	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	220	A
Body-drain diode reverse drain current	I <sub>DR</sub>	55	A
Avalanche current	I <sub>AP</sub> <sup>Note2</sup>	30	A
Avalanche energy	E <sub>AR</sub> <sup>Note2</sup>	90	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	30	W
Channel to Case Thermal Resistance	θ <sub>ch-C</sub>	4.17	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω  
3. T<sub>c</sub> = 25°C

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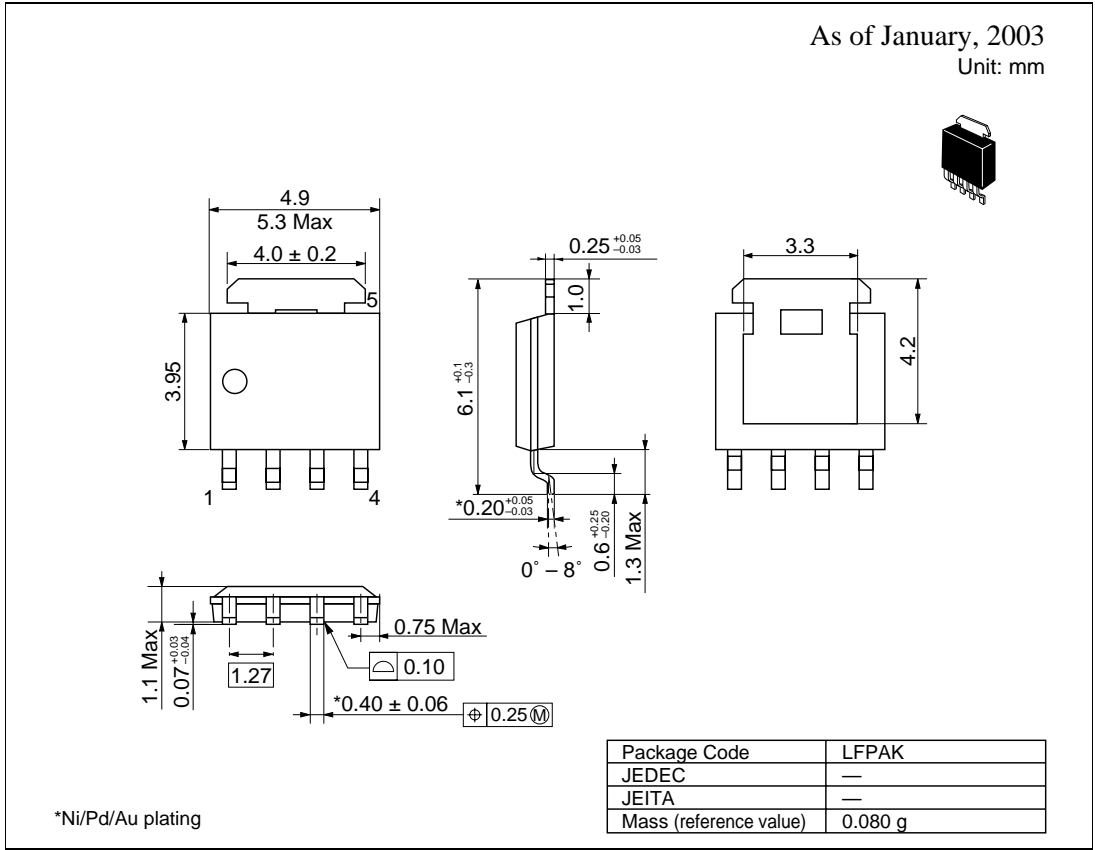
### Electrical Characteristics

(T<sub>a</sub> = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	30	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	± 20	—	—	V	I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	± 10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	1.6	—	2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	2.5	3.3	mΩ	I <sub>D</sub> = 27.5 A, V <sub>GS</sub> = 10 V <sup>Note4</sup>
	R <sub>DS(on)</sub>	—	3.4	5.3	mΩ	I <sub>D</sub> = 27.5 A, V <sub>GS</sub> = 4.5 V <sup>Note4</sup>
Forward transfer admittance	y <sub>fs</sub>	60	100	—	S	I <sub>D</sub> = 27.5 A, V <sub>DS</sub> = 10 V <sup>Note4</sup>
Input capacitance	C <sub>iss</sub>	—	5180	—	pF	V <sub>DS</sub> = 10 V
Output capacitance	C <sub>oss</sub>	—	1200	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	380	—	pF	f = 1 MHz
Gate Resistance	R <sub>g</sub>	—	0.5	—	Ω	
Total gate charge	Q <sub>g</sub>	—	33	—	nc	V <sub>DD</sub> = 10 V
Gate to source charge	Q <sub>gs</sub>	—	15	—	nc	V <sub>GS</sub> = 4.5 V
Gate to drain charge	Q <sub>gd</sub>	—	7.1	—	nc	I <sub>D</sub> = 55 A
Turn-on delay time	t <sub>d(on)</sub>	—	13	—	ns	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 27.5 A
Rise time	t <sub>r</sub>	—	65	—	ns	V <sub>DD</sub> = 10 V
Turn-off delay time	t <sub>d(off)</sub>	—	60	—	ns	R <sub>L</sub> = 0.36 Ω
Fall time	t <sub>f</sub>	—	9.5	—	ns	R <sub>g</sub> = 4.7 Ω
Body-drain diode forward voltage	V <sub>DF</sub>	—	0.81	1.06	V	I <sub>F</sub> = 55 A, V <sub>GS</sub> = 0 <sup>Note4</sup>
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	40	—	ns	I <sub>F</sub> = 55 A, V <sub>GS</sub> = 0 diF/ dt = 100 A/ μs

Notes: 4. Pulse test

Package Dimensions



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