HAT2265H

Silicon N Channel Power MOS FET Power Switching

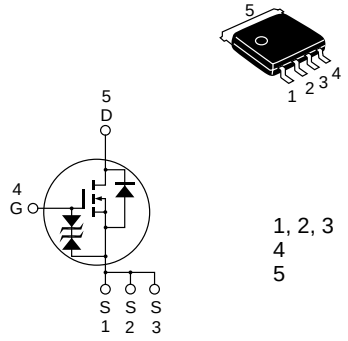
Rev.0.00
Sept.2004

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 2.5 mΩ typ. (at V_{GS} = 10 V)
- Lead Free

Outline

LFPAK



1, 2, 3	Source
4	Gate
5	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	55	A
Drain peak current	$I_{D(pulse)}$ Note1	220	A
Body-drain diode reverse drain current	I_{DR}	55	A
Avalanche current	I_{AP} Note 2	30	A
Avalanche energy	E_{AR} Note 2	90	mJ
Channel dissipation	Pch Note3	30	W
Channel to Case Thermal Resistance	θch-C	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tch = 25° C, Rg ≥ 50 Ω
3. Tc = 25°C

Electrical Characteristics

(Ta = 25°C)

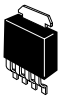
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	± 10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.6	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	2.5	3.3	mΩ	I_D = 27.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	3.4	5.3	mΩ	I_D = 27.5 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	60	100	—	S	I_D = 27.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	5180	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1200	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	380	—	pF	f = 1 MHz
Gate Resistance	Rg	—	0.5	—	Ω	
Total gate charge	Qg	—	33	—	nc	V_{DD} = 10 V
Gate to source charge	Qgs	—	15	—	nc	V_{GS} = 4.5 V
Gate to drain charge	Qgd	—	7.1	—	nc	I_D = 55 A
Turn-on delay time	$t_{d(on)}$	—	13	—	ns	V_{GS} = 10 V, I_D = 27.5 A
Rise time	t_r	—	65	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	R_L = 0.36 Ω
Fall time	t_f	—	9.5	—	ns	Rg = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.81	1.06	V	IF = 55 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	40	—	ns	IF = 55 A, V_{GS} = 0 diF/ dt = 100 A/ µs

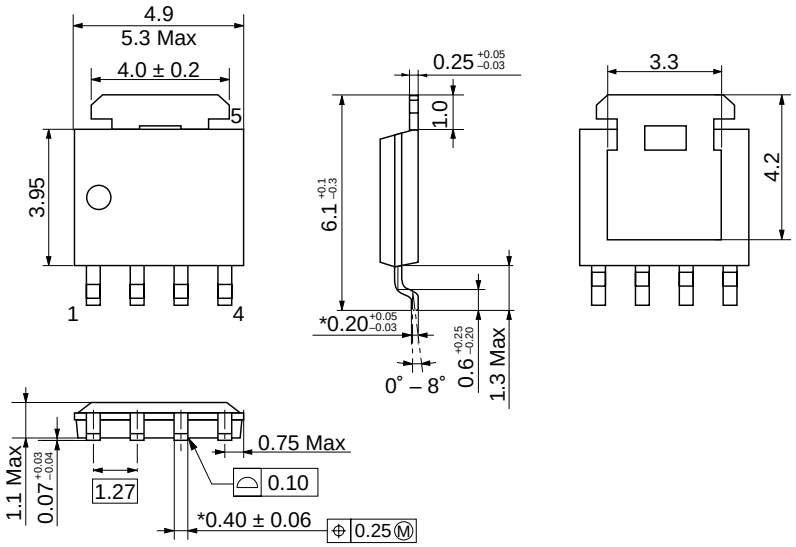
Notes: 4. Pulse test

Package Dimensions

As of January, 2003

Unit: mm





Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

*Ni/Pd/Au plating

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