DDR V_{DDQ} and Termination Voltage Regulator

Features

- Two linear regulators
  -Maximum 2A current from V_{DDQ}
  -Source and sink up to 2A V_{TT} current
- 1.7V to 2.8V adjustable V_{DDQ} output voltage
- 500mV typical V_{DDQ} dropout voltage at 2A
- V_{TT} tracking at 50% of V_{DDQ}
- Excellent load and line regulation, low noise
- Fast transient response
- Meet JEDEC DDR-I and DDR-II memory power spec.
- Linear regulator design requires no inductors and has low external component count
- Integrated power MOSFETs
- Dual purpose ADJ/Shutdown pin
- Built-in over-current limit with short-circuit foldback and thermal shutdown for V_{DDQ} and V_{TT}
- Fast transient response
- 5mA quiescent current
- TDFN-8 and SOIC-8 packages for high performance thermal dissipation and easy PC board layout
- Optional RoHS Compliant Lead-free packaging

Applications

- DDR memory and active termination buses
- Desktop Computers, Servers
- Residential and Enterprise Gateways
- DSL Modems
- Routers and Switchers
- DVD recorders
- 3D AGP cards
- LCD TV and STB

Product Description

The CM3202 is a dual-output low noise linear regulator designed to meet SSTL-2 and SSTL-3 specifications for DDR-SDRAM V_{DDQ} supply and termination voltage V_{TT} supply. With integrated power MOSFET's, the CM3202 can source up to 2A of V_{DDQ} current, and source or sink up to 2A V_{TT} current. The typical drop-out voltage for V_{DDQ} is 500 mV at 2A load current.

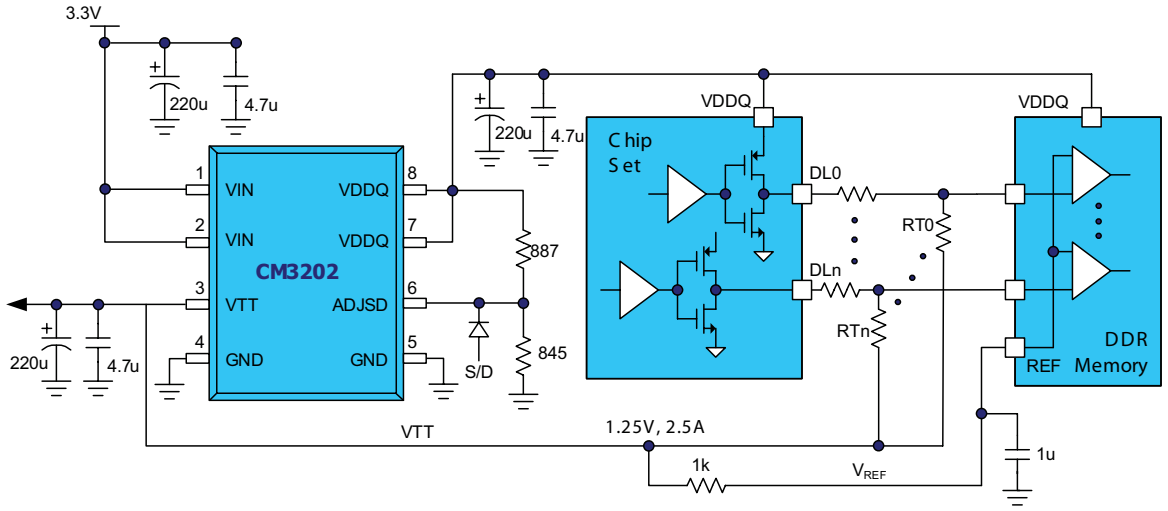
The CM3202 provides fast response to transient load changes. Load regulation is excellent, less than 1%, from no load to full load. It also has built-in over-current limits and thermal shutdown at 170°C.

The CM3202 is packaged in an easy-to-use TDFN-8 and SOIC-8. Low thermal resistance (55°C/W) allows it to withstand 1.55W (1) dissipation at 85°C ambient. It can operate over the industrial ambient temperature range of –40°C to 85°C.

Note(1) :

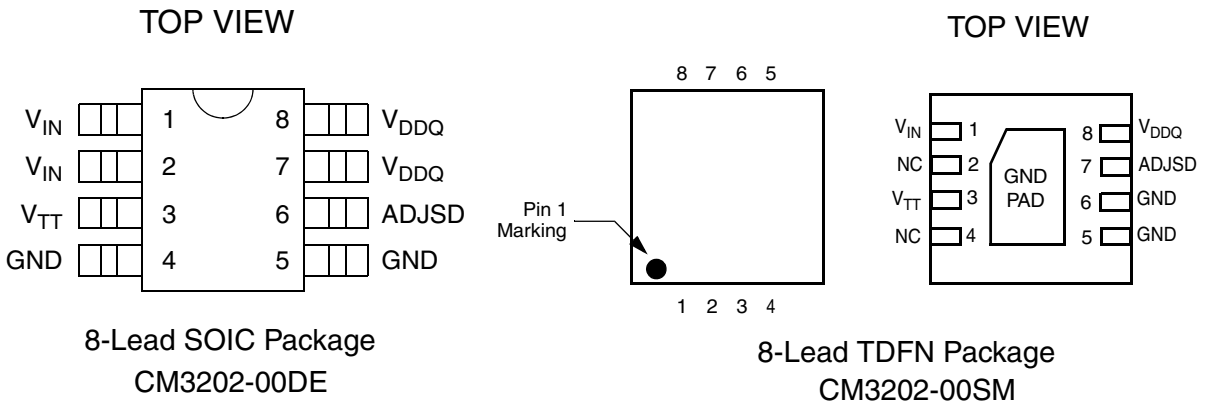
If TDFN-8 is mounted on a double-sided printed circuit board with two square inches of copper area, it can to withstand 2W dissipation at 85°C ambient then.

Typical Application



Package Pinout

PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale.

Ordering Information

PART NUMBERING INFORMATION

Pins	Package	Lead-free Finish	
		Ordering Part Number[1]	Part Marking
8	TDFN	CM3202-00DE	CM3202
8	SOIC	CM3202-00SM	CM3202

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS

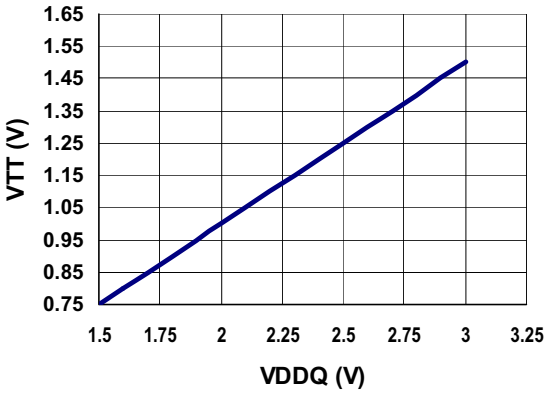
PARAMETER	RATING	UNITS
VIN to GND	[GND - 0.3] to +6.0	V
Pin Voltages V_{DDQ} ,V_{TT} to GND ADJSD to GND	 [GND - 0.3] to +6.0 [GND - 0.3] to +6.0	 V V
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range	-40 to +85	°C
Lead Temperature (Soldering, 10s)	300	°C

Specifications (cont'd)

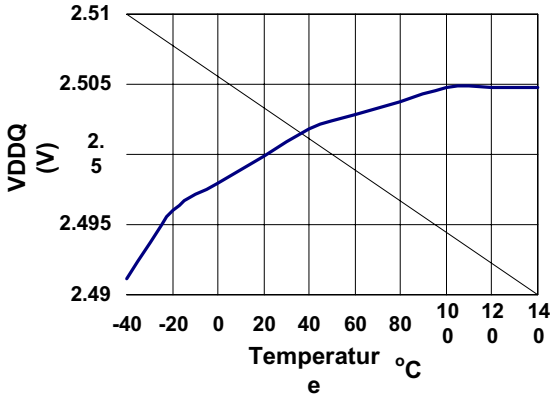
ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
V_{IN} = 3.3V, typical values are at T_A = 25°C (unless otherwise specified)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
VIN						
V_{IN}	Supply Voltage Range		3	3.3	3.6	V
V_{UVLO}	Under-voltage Lockout	All outputs are no load		2.5		V
	UVLO Hysterisis			200		mV
I_Q	Quiescent Current	V_{DDQ} = 0V, V_{TT} = 0V, ADJSD = 3.3V (shutdown)		200		mA
		V_{DDQ} = 2.5V, V_{TT} = 1.25V, (no load)		5		mA
V_{DDQ} Regulator						
	Output Current Limit	V_{OUT} = 2.5V		2.8		A
V_{REF}	Reference Voltage		1.235	1.250	1.265	V
I_{BIAS}	Input Bias Current (I_{ADJ})	VADJSD = V_{REF}		30	200	nA
$V_{R\ LOAD}$	Load Regulation	I_O = 10mA to 2A		1		%
$V_{R\ LINE}$	Line Regulation	V_{IN} = 3.15V to 3.5V, I_O = 10mA		1		%
$V_{DROPOUT}$	Dropout Voltage	V_{IN} = 3.15V, I_O = 2A		500		mV
V_{TT} Regulator						
	Output Current Limit (Source)	V_{OUT} = 1.25V		2.8		A
	Output Current Limit (Sink)	V_{OUT} = 1.25V		2.8		A
$V_{R\ VTTLOAD}$	Load Regulation	I_O = 0A to 2A		1		%
		I_O = 0A to -2A		1		%
Over Temperature Protection						
	Thermal Shutdown Temperature			170		°C
	Thermal Shutdown Hysteresis			50		°C

Typical Operating Characteristics

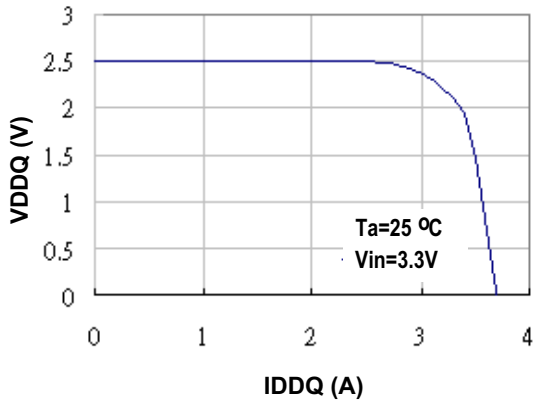
VTT vs. VDDQ



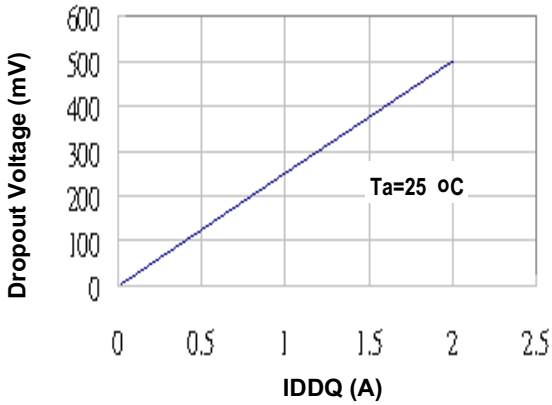
VDDQ vs. Temperature



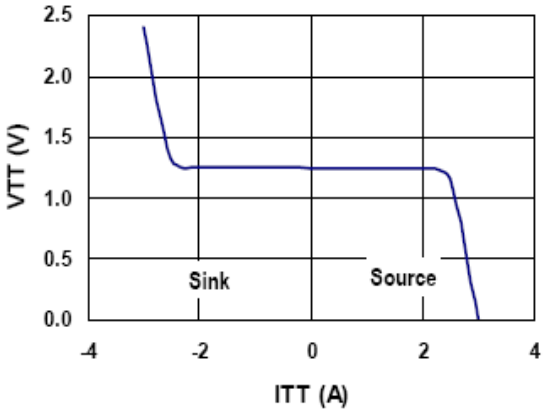
VDDQ vs. Load Current



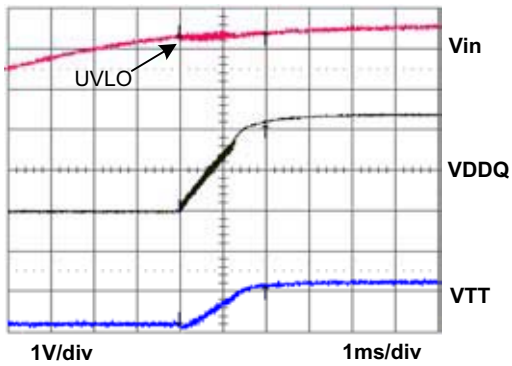
VDDQ Dropout vs. IDDQ



VTT vs. Load Current

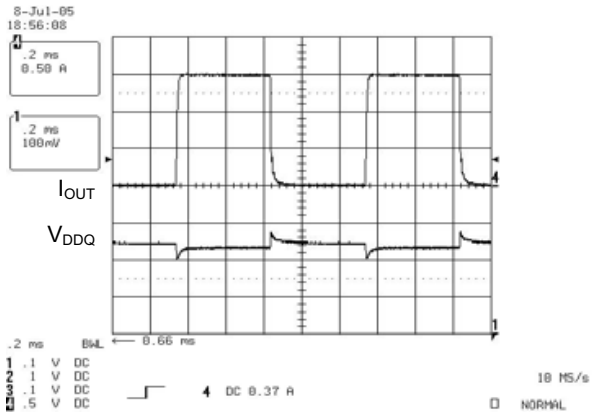


Startup into Full Load



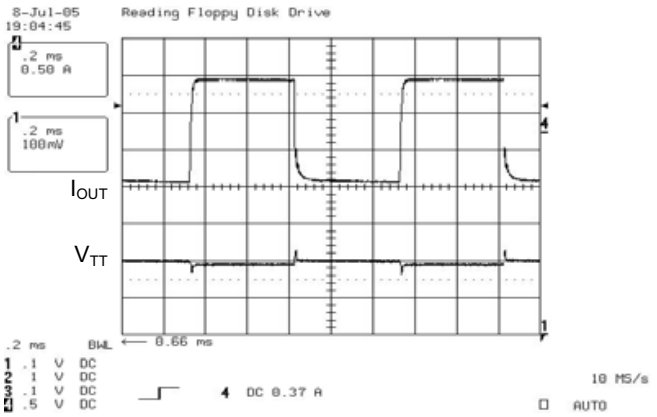
Typical Operating Characteristics (cont'd)

VDDQ Transient Response



V_{IN} = 3.3V
I_{OUT} Step: 15mA ~ 1.5A

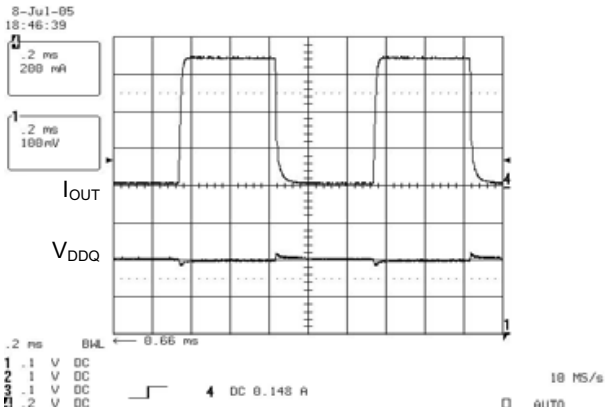
VTT Transient Response



V_{IN} = 3.3V
I_{OUT} Step: -750mA ~ +750mA

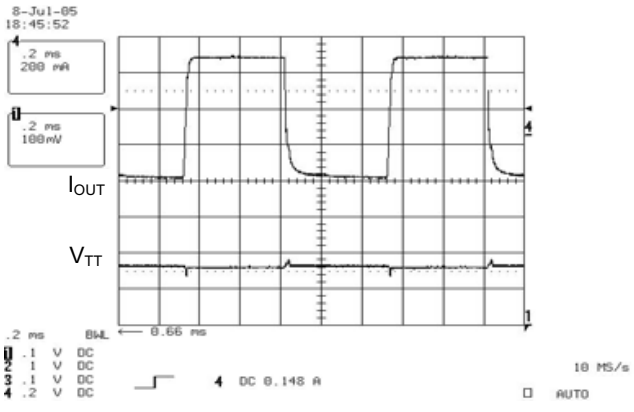
With TDFN-8 Package

VDDQ Transient Response



V_{IN} = 3.3V
I_{OUT} Step: 15mA ~ 700mA

VTT Transient Response



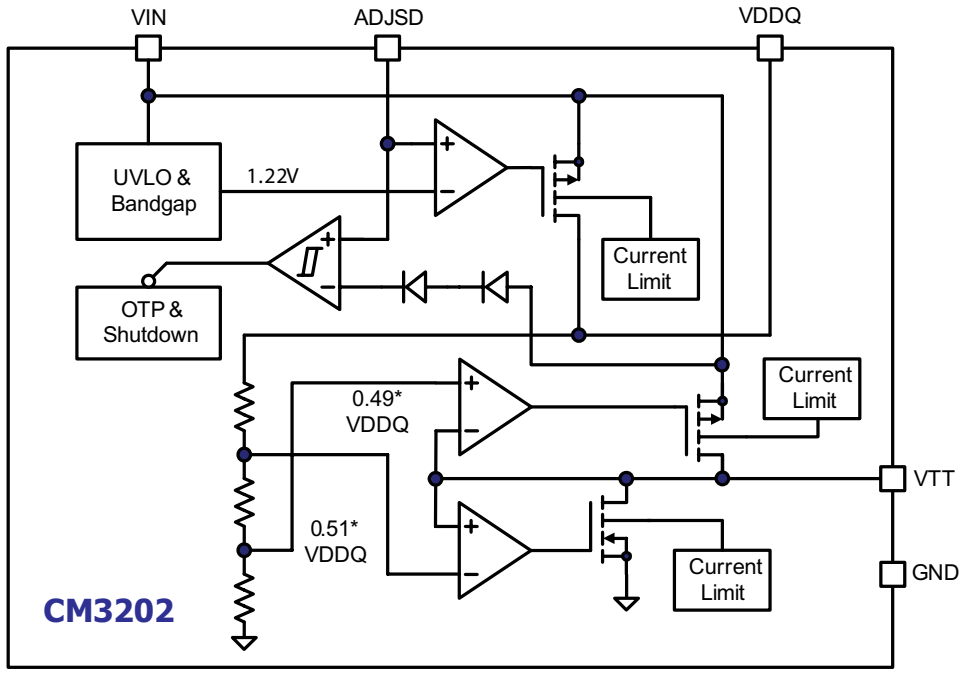
V_{IN} = 3.3V
I_{OUT} Step: -350mA ~ +350mA

With SOIC-8 Package

Pin Description
Pin Descriptions

PIN DESCRIPTIONS			
PIN(S) TDFN 8	**PIN(S) SOIC 8**	**NAME**	**DESCRIPTION**
1	1, 2	V_{IN}	Input voltage pin, typically 3.3V from the silver box.
2, 4		NC	
3	3	V_{TT}	V_{TT} regulator output voltage pin, which is preset to 50% of V_{DDQ}.
5, 6	4, 5	GND	Ground pin. The back tab is also ground and serves as the package heatsink. It should be soldered to the circuit board copper to remove excess heat from the IC.
7	6	ADJSD	This pin is for V_{DDQ} output voltage Adjustment. The V_{DDQ} output voltage is set using an external resistor divider connected to ADJSD. The output voltage is determined by the following formula $V_{DDQ} = 1.25V \times \frac{R1 + R2}{R1}$ where R1 is the ground-side resistor and R2 is the upper resistor of the divider. Connect these resistors to the V_{DDQ} output at the point of regulation. In addition, functions as a Shutdown pin. Apply a voltage higher than V_{IN}-0.6V to this pin to simultaneously shutdown both V_{DDQ} and V_{TT} outputs. The outputs are restored when the voltage is lowered below V_{IN}-0.6V. A low-leakage diode in series with the Shutdown signal is recommended to avoid interference with the voltage adjustment setting.
8	7, 8	V_{DDQ}	V_{DDQ} regulator output voltage pin.

Application Information (cont'd)



Application Information

Powering DDR Memory

Double-Data-Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAM's transmit data at both the rising falling edges of the memory bus clock.

DDR's use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power-supply rejection, while reducing power dissipation. To achieve this performance improvement, DDR requires more complex power management architecture than previous RAM technology.

Unlike the conventional DRAM technology, DDR SDRAM uses differential inputs and a reference voltage for all interface signals. This increases the data bus bandwidth, and lowers the system power consumption. Power consumption is reduced by lower operating voltage, a lower signal voltage swing associated with Stub Series Terminated Logic (SSTL_2) and by the use of a termination voltage, V_{TT}. SSTL_2 is an industry standard, defined in JEDEC document JESD8-9. SSTL_2 maintains high-speed data bus signal integrity by reducing transmission reflections. JEDEC further defines the DDR SDRAM specification in JESD79C.

DDR memory requires three tightly regulated voltages: V_{DDQ}, V_{TT}, and V_{REF} (see Figure 1). In a typical SSTL_2 receiver, the higher current V_{DDQ} supply voltage is normally 2.5V with a tolerance of ±200 mV. The active bus termination voltage, V_{TT}, is half of V_{DDQ}. V_{REF} is a reference voltage that tracks half of V_{DDQ}, ± 1%, and is compared with the V_{TT} terminated signal at the receiver. V_{TT} must be within ±40 mV of V_{REF}.

Application Info (cont'd)

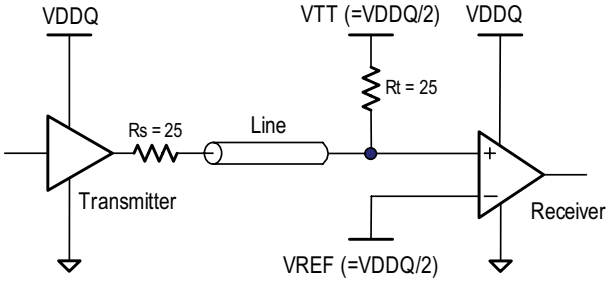


Figure 1. Typical DDR terminations, Class II

The V_{TT} power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2 mA to achieve the 405 mV minimum over V_{TT} needed at the receiver:

$$I_{terminaton} = \frac{405mV}{Rt(25\Omega)} = 16.2mA$$

A typical 64 Mbyte SSTL-2 memory system, with 128 terminated lines, has a worst-case maximum V_{TT} supply current up to ± 2.07A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ± 200 mA.

The V_{DDQ} power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 0.5A to 1A, with peaks up to 2A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for V_{TT} to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

CM3202 Regulator

The CM3202 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single TDFN-8 or SOIC-8 package. V_{DDQ} regulator can supply up to 2A current, and the two-quadrant V_{TT} termination regulator has current sink and source capability to ±2A. The V_{DDQ} linear regulator uses a PMOS pass element for a very low dropout voltage, typically 500mV at a 2A output. The output voltage of V_{DDQ} can be set by an external voltage divider. The second output, V_{TT}, is regulated at $V_{DDQ}/2$ by an internal resistor divider. The V_{TT} regulator can source, as well as sink, up to 2A current. The CM3202 is designed for optimal operation from a nominal 3.3VDC bus, but can work with VIN as high as 5V. When operating at higher VIN voltages, attention must be given to the increased package power dissipation and proportionally increased heat generation.

V_{REF} is typically routed to inputs with high impedance, such as a comparator, with little current draw. An adequate V_{REF} can be created with a simple voltage divider of precision, matched resistors from V_{DDQ} to ground. A small ceramic bypass capacitor can also be added for improved noise performance.

Input and Output Capacitors

The CM3202 requires that at least a 220µF electrolytic capacitor be located near the V_{IN} pin for stability and to maintain the input bus voltage during load transients. An additional 4.7µF ceramic capacitor between the V_{IN} and the GND, located as close as possible to those pins, is recommended to ensure stability.

A minimum of a 220µF electrolytic capacitor is recommended for the V_{DDQ} output. An additional 4.7µF ceramic capacitor between the V_{DDQ} and GND, located very close to those pins, is recommended.

A minimum of a 220µF, electrolytic capacitor is recommended for the V_{TT} output. This capacitor should have low ESR to achieve best output transient response. SP or OSCON capacitors provide low ESR at high frequency, and thus are a good choice. In addition, place a 4.7µF ceramic capacitor between the V_{TT} pin and GND, located very close to those pins. The total ESR must be low enough to keep the transient within the V_{TT} window of 40mV during the transition for source to sink. An average current step of ± 0.5A requires:

$$ESR < \frac{40mV}{1A} = 40m\Omega$$

Both outputs will remain stable and in regulation even during light or no load conditions.

Application Info (cont'd)

Adjusting V_{DDQ} Output Voltage

The CM3202 internal bandgap reference is set at 1.25V. The V_{DDQ} voltage is adjustable by using a resistor divider, R1 and R2:

$$V_{DDQ} = V_{ADJ} \times \frac{R1 + R2}{R1}$$

where V_{ADJ} = 1.25V (± 1%). For best regulator stability, we recommend that R1 and R2 not exceed 10kΩ each.

Shutdown

ADJSD also serves as a shutdown pin. When this is pulled high, > (V_{IN} - 0.6V), the V_{DDQ} output is turned off and both source and sink MOSFET's of the V_{TT} regulator are set to a high impedance state. During shutdown, the quiescent current is reduced to less than 3mA, independent of output load.

It is recommended that a 1N914 or equivalent low leakage diode be placed between ADJSD Pin and an external shutdown signal to prevent interference with the ADJ pin's normal operation. When the diode anode is pulled low, or left open, the CM3202 is again enabled.

Current Limit, Foldback and Over-temperature Protection

The CM3202 features internal current limiting with thermal protection. During normal operation, V_{DDQ} limits the output current to approximately 2A and V_{TT} limits the output current to approximately ±2A. When V_{TT} is current limiting into a hard short circuit, the output current folds back to a lower level, about 1A, until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the junction temperature of the device exceeds 170 °C (typical), the thermal protection circuitry triggers and shuts down both outputs. Once the junction temperature has cooled to below about 120 °C, the CM3202 returns to normal operation.

Thermal Considerations

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) primarily consists of two paths in the series. The first path is the junction to the case (θ_{JC}) which is defined by the package style and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any condition can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D \times (\theta_{JC}) + P_D \times (\theta_{CA}) = T_{AMB} + P_D \times (\theta_{CA})$$

When a CM3202 is mounted on a double-sided printed circuit board with two square inches of copper allocated for "heat spreading," the θ_{JA} is approximately 42.5 °C/Watt for the CM3202-00DE (TDFN-8) and 85 °C/Watt for CM3202-00SM (SOIC-8). Based on the over temperature limit of 170°C with an ambient of 85°C, the available power of the package will be:

$$P_{D(TDFN8)} = \frac{170\,°C \quad 85°C}{42.5°C / W} = 2W$$

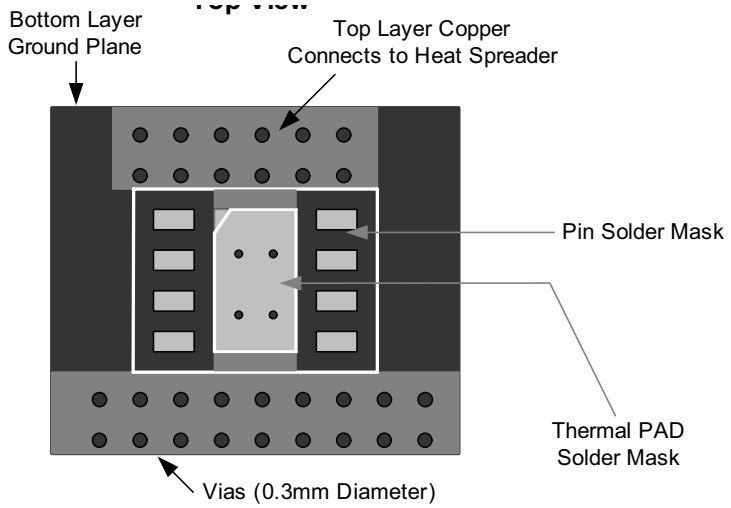
$$P_{D(SOIC8)} = \frac{170\,°C \quad 85°C}{85°C / W} = 1W$$

PCB Layout Considerations

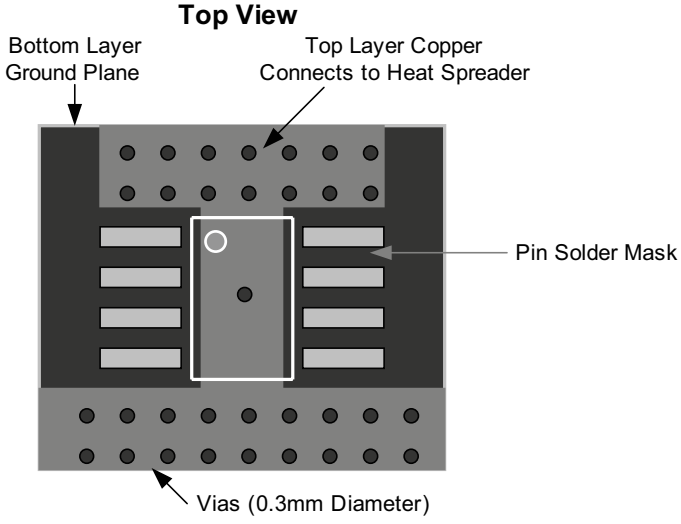
TheCM3202 has a heat spreader attached to the bottom of the TDFN-8 package in order for the heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during the manufacturing, the heat will be transferred between the two pads. See the Figure 2, the CM3202-00DE (TDFN-8) and CM3202-00SM (SOIC-8) show the recommended PCB layout. Please be noted that there are six vias in the SOIC-8 package (four vias in the TDFN-8 package) on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can be resulted in

Application Info (cont'd)

blocking of the solder. The ground and power planes need to be at least 2 square inches of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and not near other heat-dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3202-00DE (TDFN-8) to ambient, θ_{JA}, of approximately 42.5 °C/W, or θ_{JA} of approximately 85 °C/W for the CM3202-00SM (SOIC-8).



(TDFN-8 Package)



(SOIC-8 Package)

Note: This drawing is not to scale

Figure 2. Thermal Layout

Mechanical Details

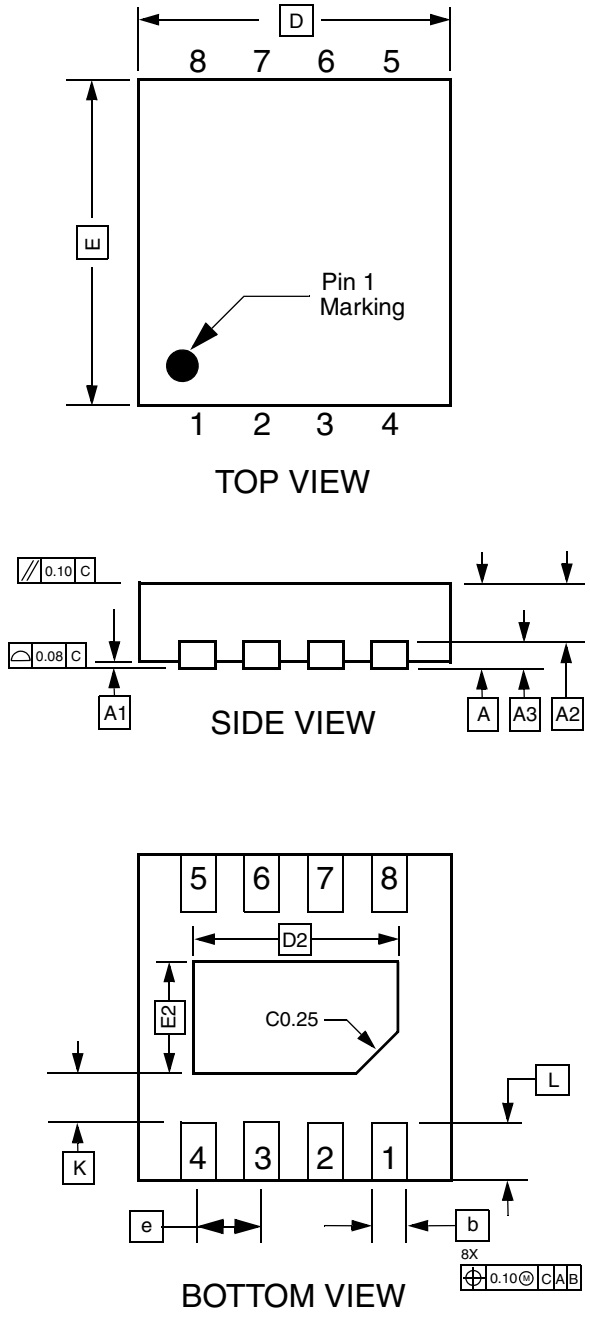
TDFN-08 Mechanical Specifications

The CM3202-00DE is supplied in an 8-lead, 0.65mm pitch TDFN package. Dimensions are presented below.

PACKAGE DIMENSIONS						
Package	TDFN					
JEDEC No.	MO-229 (Var. WEEC-1)[=]					
Leads	6					
Dim.	**Millimeters**			**Inches**		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.45	0.55	0.65	0.018	0.022	0.026
A3		0.20			0.008	
b	0.25	0.30	0.35	0.010	0.012	0.014
D		3.00			0.118	
D2	1.90	2.00	2.10	0.075	0.079	0.083
E		3.00			0.118	
E2	1.60	1.70	1.80	0.063	0.067	0.071
e		0.65			0.026	
K	0.20			0.008		
L	0.20	0.30	0.45	0.008	0.012	0.018
# per tape and reel	3000 pieces					
Controlling dimension: millimeters						

[=]This package is compliant with JEDEC standard MO-229, variation VEEC-1 with exception of the "D2", "E2" and "b" dimensions as called out in the table above.

Mechanical Package Diagrams



Package Dimensions for 8-Lead TDFN

Mechanical Details (cont'd)

SOIC-8 Mechanical Specifications

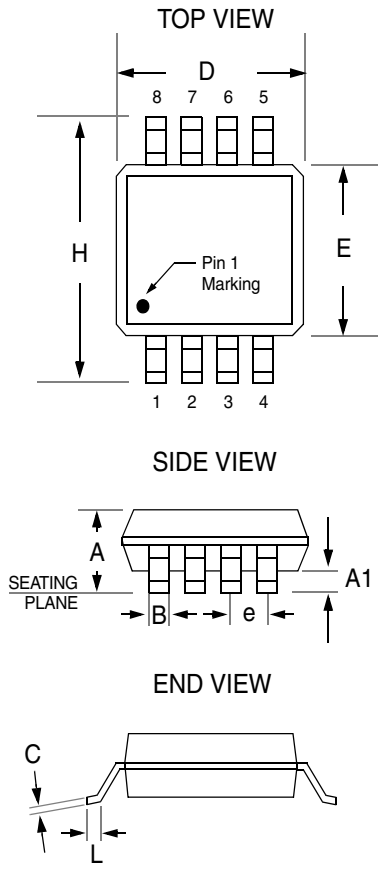
Dimensions for CM3202-00SM devices packaged in 8-lead SOIC packages with an intagrated heatslug are presented below.

PACKAGE DIMENSIONS				
Package	SOIC-8			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.30	1.62	0.051	0.064
A_1	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for SOIC-8