

LSU403 LOW NOISE, LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET



Linear Systems replaces discontinued Siliconix U403

The LSU403 is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The LSU403 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LSU403 features a 5-mV offset and $10-\mu V/^{\circ} C$ drift. The LSU403 is a direct replacement for discontinued Siliconix LSU403.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LSU403 Applications:

- Wideband Differential Amps
- High-Speed,Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES							
LOW DRIFT		$ V_{GS1-2}/T = 10\mu V/^{\circ}C$ TYP.					
LOW NOISE		$e_n = 6nV/Hz @ 10Hz TYP.$					
LOW PINCH	OFF	$V_p = 2.5V TYP.$					
ABSOLUTE MAXIMUM RATINGS							
@ 25°C (unless otherwise noted)							
Maximum Temperatures							
Storage Tem	perature		-65°C to +150°C				
Operating Ju	ınction Temperature		+150°C				
Maximum Voltage and Current for Each Transistor – Note 1							
-V _{GSS}	Gate Voltage to Drain or So	50V					
-V _{DSO}	Drain to Source Voltage	50V					
-I _{G(f)}	Gate Forward Current	10mA					
Maximum Power Dissipation							
Device Dissipation @ Free Air – Total 300mW							

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED								
SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS				
V _{GS1-2} / T max.	DRIFT VS.	25	μV/°C	V_{DG} =10V, I_{D} =200 μ A				
	TEMPERATURE			T _A =-55°C to +125°C				
V _{GS1-2} max.	OFFSET VOLTAGE	10	mV	V_{DG} =10V, I_{D} =200 μ A				

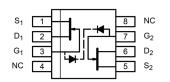
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	50	60		٧	$V_{DS} = 0$ $I_D = 1nA$
BV _{GGO}	Gate- <mark>T</mark> o-G <mark>at</mark> e Breakdown	±50		-	V	$I_G = 1$ nA $I_D = 0$ $I_S = 0$
Y _{fSS}	TRANSCONDUCTANCE Full Conduction	2000	- 1	7000	μmho	$V_{DG} = 10V$ $V_{GS} = 0V$ $f = 1kHz$
Y _{fS}	Typica <mark>l O</mark> per <mark>at</mark> ion	1000		2000	μmho	$V_{DG} = 15V$ $I_{D} = 200 \mu A$ $f = 1 kHz$
Y _{FS1-2} / Y _{FS}	Mismatch		0.6	3	%	
	DRAIN CURRENT					
I _{DSS}	Full Conduction	0.5		10	mA	$V_{DG} = 10V$ $V_{GS} = 0V$
$ I_{DSS1-2}/I_{DSS} $	Mismatch at Full Conduction		1	5	%	
	GATE VOLTAGE					
$V_{GS}(off)$ or V_p	Pinchoff voltage	-0.5		-2.5	V	V_{DS} = 15V I_D = 1nA
V _{GS} (on)	Operating Range			-2.3	V	V_{DS} =15V I_D =200 μ A
	GATE CURRENT					
-I _G max.	Operating		-4	-15	pA	$V_{DG} = 15V I_D = 200 \mu A$
-l _G max.	High Temperature			-10	nA	T _A = +125°C
-I _{GSS} max.	At Full Conduction			100	pA	V _{DS} =0
-I _{GSS} max.	High Temperature	5	5	5	pA	$V_{DG} = 15V$ $T_{A} = +125$ °C
Y _{OSS}	OUTPUT CONDUCTANCE Full Conduction			20	μmho	V _{DG} = 10V V _{GS} = 0V
Y _{OS}	Operating		0.2	2	μmho	$V_{DG} = 15V$ $I_{D} = 500 \mu A$
CMR	-20 log V _{GS1-2} / V _{DS}	95			dB	V _{DS} = 10 to 20V I _D =30μA
	NOISE					V_{DS} = 15V V_{GS} = 0V R_{G} = 10M
NF	Figure			0.5	dB	f= 100Hz NBW= 6Hz
e _n	Voltage		20		nV/√Hz	V _{DS} =15V I _D =200μA f=10Hz NBW=1Hz
C _{ISS}	<u>CAPACITANCE</u> Input			8	pF	V _{DS} = 15V I _D = 200μA f= 1MHz
C _{RSS}	Reverse Transfer			1.5	pF	05

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LSU403 in PDIP / SOIC LSU403 available as bare die

Please contact Micross for full package and die dimensions



PDIP / SOIC (Top View)

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