DAC-1508A/1408A

8-BIT MULTIPLYING
D/A CONVERTERS

Precision Monolithics Inc.

FEATURES

- **Improved Direct Replacement for MC1508/MC1408**
- **0.19% Nonlinearity Maximum Over Temperature Range**
- **Improved Settling Time ..... 250ns, Typ**
- **Improved Power Consumption ..... 157mW, Typ**
- **Compatible with TTL, CMOS Logic**
- **Standard Supply Voltages +5.0V and −5.0V to −15V**
- **Output Voltage Swing ..... +0.5V to −5.0V**
- **High-Speed Multiplying Input 4.0mA/μs**

ORDERING INFORMATION†

RELATIVE ACCURACY % FS	16-PIN DUAL-IN-LINE PACKAGE HERMETIC MILITARY	HERMETIC COMMERCIAL	PLASTIC COMMERCIAL
±0.19%	DAC1508A-8Q	DAC1408A-8Q	DAC1408A-8P
±0.39%	—	DAC1408A-7Q	DAC1408A-7P
±0.78%	—	DAC1408A-6Q	DAC1408A-6P

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

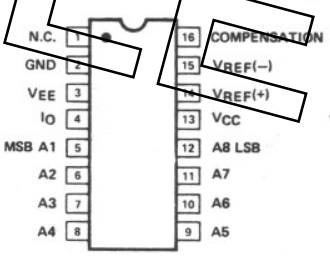
The DAC-1508A/1408A are 8-bit monolithic multiplying digital-to-analog converters consisting of a reference current amplifier, R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full-scale output current of 1.992mA would result from a reference input current of 2.0mA.

The DAC-1508A/1408A is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building tracking and successive approximation analog-to-digital converters.

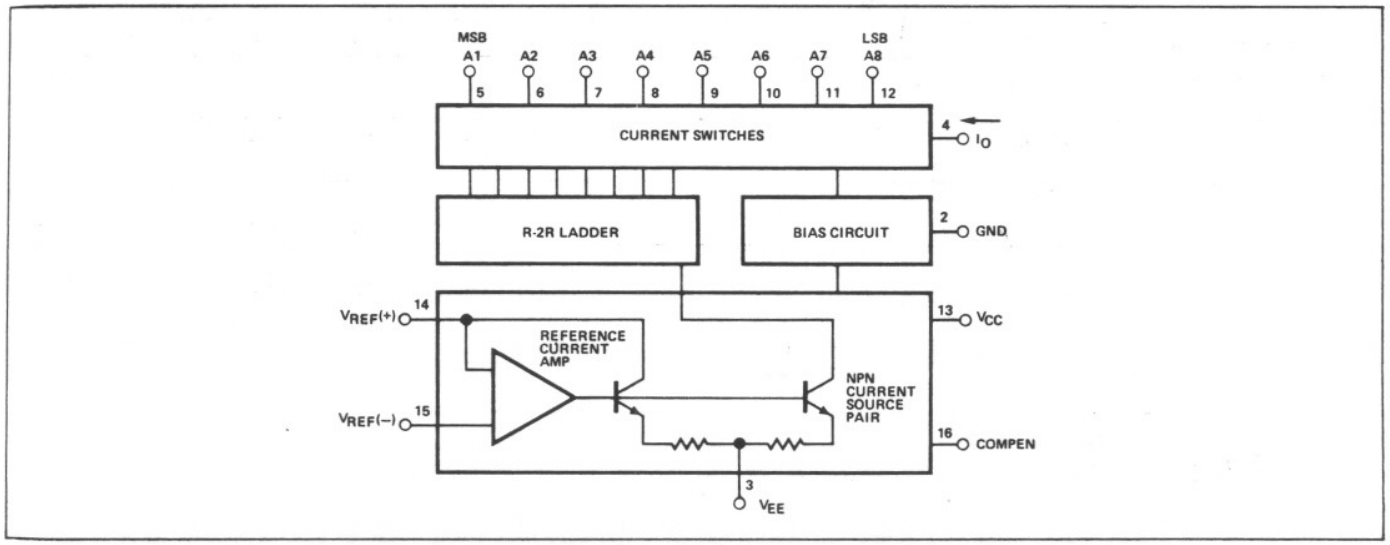
For significantly improved speed and applications flexibility your attention is directed to the DAC-08 8-bit high-speed multiplying D/A converter data sheet. For D/A converters, which include precision voltage references on the chip, please refer to the DAC-210 or the DAC-100 data sheet.

PIN CONNECTIONS



16-PIN DUAL-IN-LINE PACKAGE
HERMETIC (Q)
EPOXY (P)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
- V_{CC} ..... +5.5Vdc
- V_{EE} ..... −16.5Vdc

Digital Input Voltage, V_5 through V_{12} ..... +5.5, 0Vdc
Applied Output Voltage ..... +0.5, −5.2Vdc
Reference Current, I_{14} 5mA
Power Dissipation (Package Limitation), P_d
- Ceramic Package (or Epoxy B Package) 100mW
- Derate above $T_A = +25°C$ ..... 6.7mW/°C
- Derate above $T_A = +100°C$ for Epoxy B Package ..... 5.3mW/°C

Operating Temperature Range, T_A
- DAC-1508A ..... −55°C to +125°C
- DAC-1408A ..... 0°C to +75°C

DICE Junction Temperature (T_j) ..... −65°C to 150°C
Storage Temperature Range, T_{stg} ..... −65°C to +150°C
- Plastic Package Only ..... −65°C to +125°C

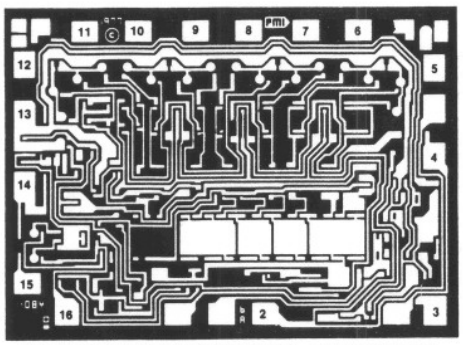
NOTE: Ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_{CC} = +5Vdc, V_{EE} = −15Vdc, $V_{REF}/R14$ = 2mA, −55°C ≤ T_A ≤ +125°C for DAC-1508A-8, 0°C ≤ T_A ≤ +75°C for DAC-1408A, unless otherwise noted. All digital inputs at logic high level.

PARAMETER	SYMBOL	CONDITIONS	DAC-1508A/1408A MIN	TYP	MAX	UNITS
Relative Accuracy (error relative to Full-Scale I_O)						
DAC-1508A-8, DAC-1408A-8			—	—	±0.19	
DAC-1408A-7	E_r		—	—	±0.39	%IFS
DAC-1408A-6			—	—	±0.78	
Settling Time to within 1/2 LSB (includes t_{PLH})	t_S	$T_A = +25°C$	—	250	—	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	$T_A = +25°C$, (Note 1)	—	30	100	ns
Output Full-Scale Current Drift	TCI_O		—	±20	—	ppm/°C
Digital Input Logic Levels (MSB)						
High Level, Logic "1"	V_{IH}		2	—	—	Vdc
Low Level, Logic "1"	V_{IL}		—	—	0.8	
Digital Input Current (MSB)	I_{IH}	High Level, V_{IH} = 5.0V	—	0	0.04	mA
	I_{IL}	Low Level, V_{IL} = 0.8V	—	−0.4	−0.8	
Reference Input Bias Current (Pin 15)	I_{15}		—	−1	−3	μA
Output Current Range	I_{OR}	V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V	0	2.0	4.2	
Output Current	I_O	V_{REF} = 2.000V, R14 = 1000Ω	1.9	1.99	2.1	mA
Output Current	$I_{O(min)}$	All bits low	—	0	4	μA
Output Voltage Compliance ($E_r \leq 0.19\%$ at $T_A = +25°C$)	V_O	I_{REF} = 1mA				
		V_{EE} = −5V	−0.6	—	+0.5	Vdc
		V_{EE} = −10V	−5	—	+0.5	
Reference Current Slew Rate	SRI_{REF}		—	4	—	mA/μs
Output Current Power Supply Sensitivity	$PSSI_{O-}$		—	0.5	2.7	μA/V
Power Supply Current	I_{CC}	All bits low	—	+9	+14	mA
	I_{EE}		—	−7.5	−13	
Power Supply Voltage	V_{CCR}	$T_A = +25°C$	+4.5	+5	+5.5	Vdc
	V_{EER}		−4.5	−15	−16.5	
Power Dissipation	P_d	All bits low				mW
		V_{EE} = −5Vdc	—	82	135	
		V_{EE} = −15Vdc	—	157	265	
		All bits high				
		V_{EE} = −5Vdc	—	70	—	
		V_{EE} = −15Vdc	—	132	—	

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.087 × 0.063 inch, 5481 sq. mils
(2.21 × 1.60 mm, 3.54 sq. mm)

1. N.C.
2. GROUND
3. V_{EE}
4. I_O
5. A1 (MSB)
6. A2
7. A3
8. A4
9. A5
10. A6
11. A7
12. A8 (LSB)
13. V_{CC}
14. $V_{REF}(+)$
15. $V_{REF}(-)$
16. COMP

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at V+ = 5V, V− = 15V, I_{REF} = 2mA, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-1408A-G LIMIT	UNITS
Resolution			8	Bits MIN
Monotonicity			8	Bits MIN
Nonlinearity			±0.19	%FS MAX
Output Voltage Compliance	V_O	Full-Scale Current Change, I_{REF} = 1mA <1/2 LSB V− = −5V	±0.5	V MAX
		V− = −5V	−0.6	V MIN
		V− = −10V	−5	V MIN
Full-Scale Current	I_{FS}	V_{REF} = 2.000V, R_{14}, R_{15} = 1.000kΩ	2, ±0.1	mA MAX
Zero-Scale Current	I_{ZS}	(All Bits Low)	4	µA MAX
Output Current Range	I_{OR}	V− = −5V	2.1	mA MAX
		V− = −15V	4.2	
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2	V MIN
Logic Input Current				
Logic "0"	I_{IL}	Low Level, V_{IL} = −0.8V	±10	µA MAX
Logic "1"	I_{IH}	High Level, V_{IH} = 5V	±10	
Reference Bias Current	I_{15}		−3	µA MAX
Output Current Power Supply Sensitivity	$PSSI_{0-}$		2.7	µA/V MAX
Power Supply Current (All Bits Low)	I+		+14	mA MAX
	I−		−13	
Power Supply Voltage Range	V_{CCR}		+5, ±0.5	V MAX/MIN
	V_{EER}		−16.5, −4.5	
Power Dissipation (All Bits Low)	P_d	V− = 5V	135	mW MAX
		V− = −15V	265	

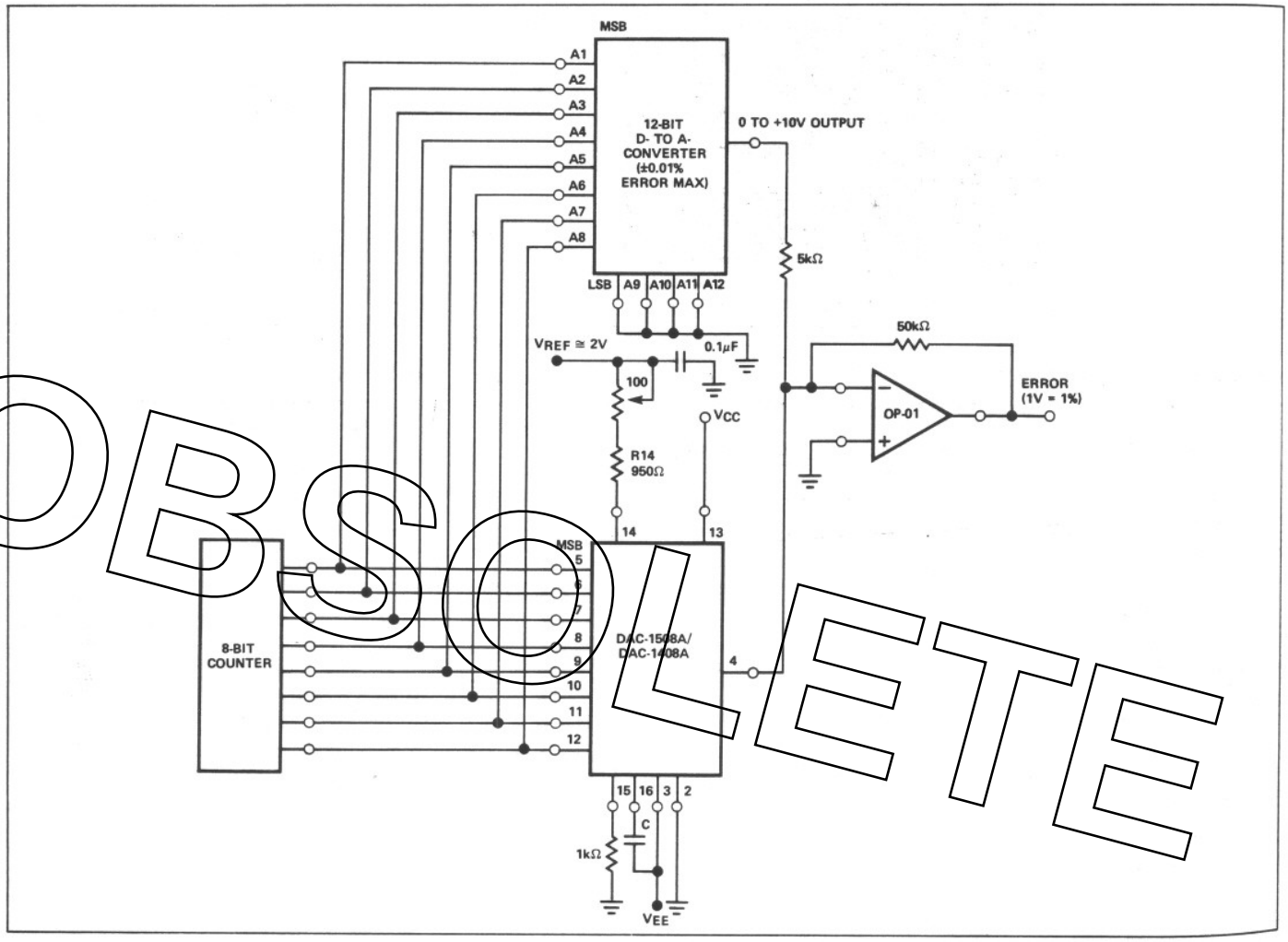
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +5V, V− = −15V, T_A = 25° C, V_{LC} and I_{OUT} connected to ground, and I_{REF} = 2mA, unless otherwise noted. Output characteristics refer to I_{OUT} only.

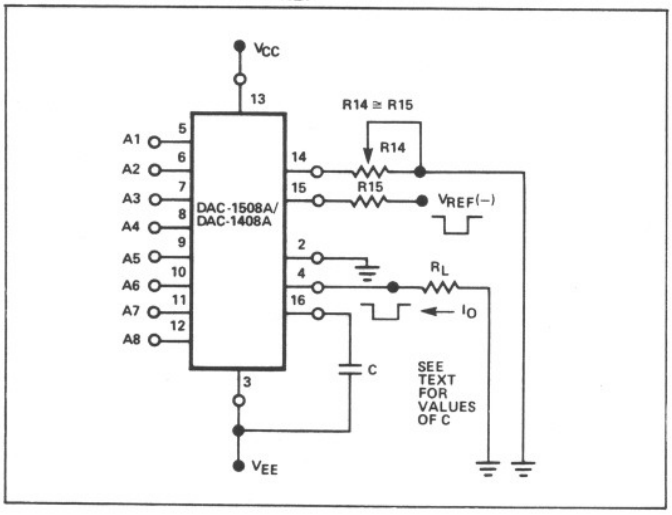
PARAMETER	SYMBOL	CONDITIONS	DAC-1408G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		4	mA/µs
Propagation Delay	t_{PLH}, t_{PHL}	Any Bit	30	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF	250	ns

APPLICATIONS

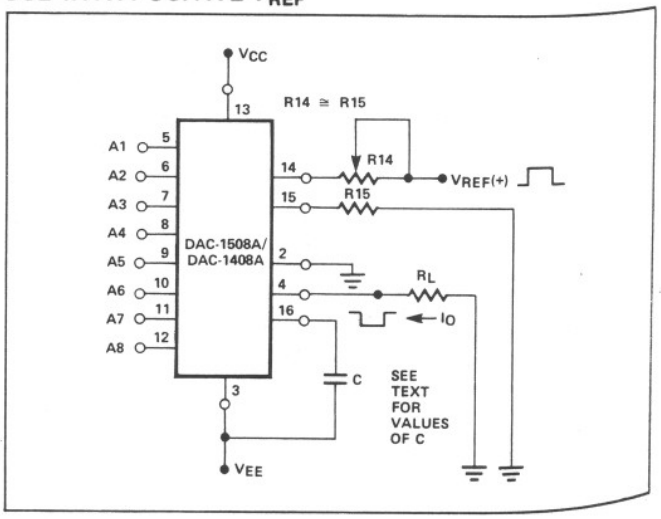
RELATIVE ACCURACY TEST CIRCUIT



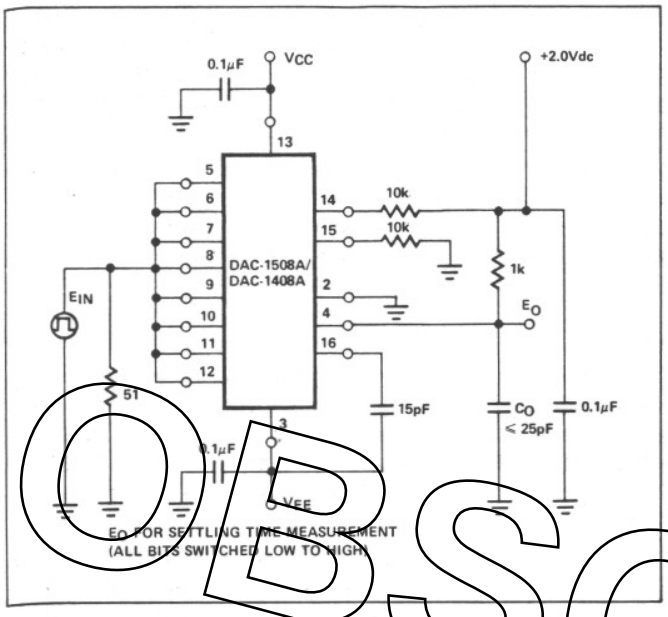
USE WITH NEGATIVE V_{REF}



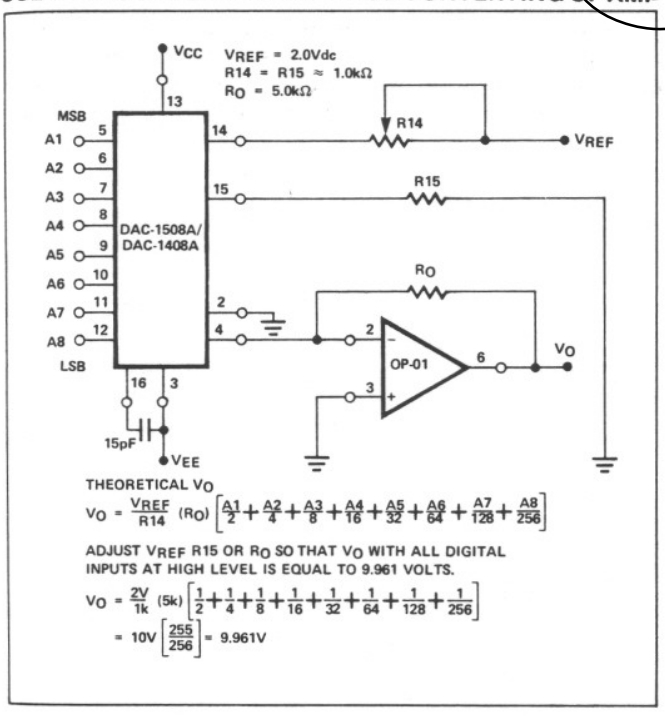
USE WITH POSITIVE V_{REF}



TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

$$V_O = \frac{V_{REF}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

ADJUST V_{REF} R15 OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS.

$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at Pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into Pin 14 regardless of the setup method or reference voltage polarity. Connections for a positive voltage are shown on the preceding page. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on Pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on Pin 4 is restricted to a range of −0.6V to +0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC-1508A-8.

The negative output voltage compliance of the DAC-1508A-8 is extended to −5.0V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992mA and load resistor of 2.5kΩ between Pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. The value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance but a 2.5kΩ load increases "worst case" settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section of Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than −7.0V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC-1508A-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC-1508A-8 has a very low full-scale current drift with temperature.

The DAC-1508A-8/DAC-1408A series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0μA), which is the ladder remainder shunted to ground. The input current to Pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. Testing relative accuracy is accomplished by the circuit labelled "Relative Accuracy Test Circuit". The 12-bit converter is calibrated for a full-scale output current of 1.992mA. This is an optional step since the DAC-1508A-8 accuracy is essentially the same between 1.5 and 2.5mA. Then the DAC-1508A-8 circuit's full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D/A converters may not be used to construct a 16-bit accuracy D/A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076% which is much more accurate than the ±0.19% specification provided by the DAC-1508A-8.

MULTIPLYING ACCURACY

The DAC-1508A-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the additional error contributions are less than 1.6μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC-1508A-8 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a DC reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "ON", which corresponds to a low-to-high transition for all bits. This time is typically 250ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25pF$.

The slowest single switch is the least significant bit. In applications where the D/A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and a minimum scope lead length are all mandatory.