



## 64K × 8 ELECTRICALLY ERASABLE EPROM

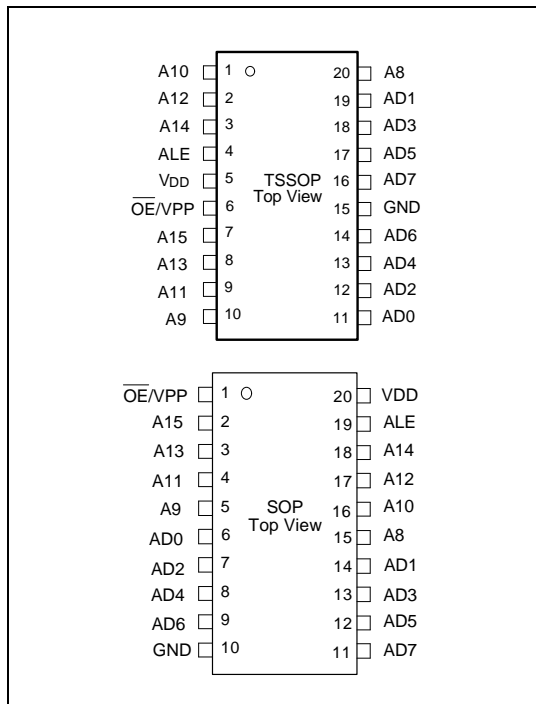
### GENERAL DESCRIPTION

The W27E520 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as 65,536 × 8 bits. It includes latches for the lower 8 address lines to multiplex with the 8 data lines. To cooperate with the MCU, this device could save the external TTL component, also cost and space. It requires only one supply in the range of 4.5V to 5.5V in normal read mode. The W27E520 provides an electrical chip erase function. It will be a great convenient when you need to change/update the contents in the device.

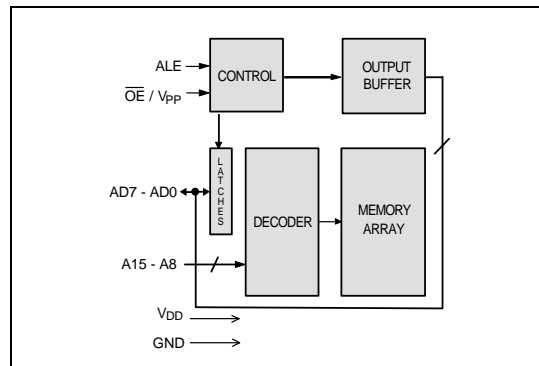
### FEATURES

- High speed access time: 70/90 nS (max.)
- Read operating current: 20 mA (max.)
- Erase/Programming operating current 30 mA (max.)
- Standby current: 100 μA (max.)
- Unregulated battery power supply range, 4.5V to 5.5V
- +13V erase and programming voltage
- High Reliability CMOS Technology
  - 2K V ESD Protection
  - 200 mA Latchup Immunity
- Fully static operation
- All inputs and outputs directly TTL/CMOS compatible
- Three-state outputs
- Available packages: 20-pin TSSOP and 20-pin SOP

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
AD0–AD7	Address/Data Inputs/Outputs
A8–A15	Address Inputs
ALE	Address Latch Enable
OE/VPP	Output Enable, Program/Erase Supply Voltage
VDD	Power Supply
GND	Ground



## FUNCTIONAL DESCRIPTION

### Read Mode

Unlike conventional UVEPROMs, which has  $\overline{CE}$  and  $\overline{OE}$  two control functions, the W27E520 has one  $\overline{OE}/VPP$  and one ALE (address\_latch\_enable) control functions. The ALE makes lower address A[7:0] to be latched in the chip when it goes from high to low, so that the same bus can be used to output data during read mode. i.e. lower address A[7:0] and data bus DQ[7:0] are multiplexed.  $\overline{OE}/VPP$  controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (TACC) is equal to the delay from ALE to output (TCE), and data are available at the outputs TOE after the falling edge of  $\overline{OE}/VPP$ , if TACC and TCE timings are met.

### Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27E520 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

There are two ways to enter Erase mode. One is to raise  $\overline{OE}/VPP$  to VPE (13V), VDD = VDE (6.5V), A9 = VHH (13V), A10 = high A8&A11 = low, and all other address pins include AD[7:0] keep at fixed low or high. Pulsing ALE high starts the erase operation. The other way is somewhat like flash, by programming two consecutive commands into the device and then enter Erase mode. The two commands are loading Data = AA(hex) to Addr. = 5555(hex) and Data = 10(hex) to Addr. = 2AAA(hex). Be careful to note that the ALE pulse widths of these two commands are different: One is 50uS, while the other is 100mS. Please refer to the Smart Erase Algorithm 1 & 2.

### Erase Verify Mode

The device will enter the Erase Verify Mode automatically after Erase Mode. Only power down the device can force the device enter Normal Read Mode again.

### Program Mode

Programming is the only way to change cell data from "1" to "0." The program mode is entered when  $\overline{OE}/VPP$  is raised to VPP (13V), VDD = VDP (6.5V), the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing ALE high starts the programming operation.

### Program Verify Mode

The device will enter the Program Verify Mode automatically after Program Mode. Only power down the device can force the device enter Normal Read Mode again.

### Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When ALE low, erasing or programming of non-target chips is inhibited, so that except for the ALE and  $\overline{OE}/VPP$  pins, the W27E520 may have common inputs.

### Standby Mode

The standby mode significantly reduces VDD current. This mode is entered when ALE and  $\overline{OE}/VPP$  keep high. In standby mode, all outputs are in a high impedance state.



### System Considerations

An EPROM's power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels ( $I_{SB}$ ), active current levels ( $I_{DD}$ ), and transient current peaks produced by the falling and rising edges of ALE. Transient current magnitudes depend on the device output's capacitive and inductive loading. Proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu\text{F}$  ceramic capacitor connected between its VDD and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7  $\mu\text{F}$  electrolytic capacitor should be placed at the array's power supply connection between VDD and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

### TABLE OF OPERATING MODES

( $V_{PP} = 13\text{V}$ ,  $V_{PE} = 13\text{V}$ ,  $V_{HH} = 12\text{V}$ ,  $V_{DP} = 6.5\text{V}$ ,  $V_{DE} = 6.5\text{V}$ ,  $V_{DD} = 5.0\text{V}$ ,  $V_{DI} = 5.0\text{V}$ , X =  $V_{IH}$  or  $V_{IL}$ )

MODE	PIN				
	ALE	$\overline{\text{OE}}/V_{PP}$	OTHER ADDRESS	VDD	AD[7:0]
Address Latch Enable	$V_{IH}$	$V_{IH}$	A1N	VDD	A[7:0]
Read	$V_{IL}$	$V_{IL}$	A1N	VDD	DOUT
Output Disable	$V_{IL}$ $/V_{IH}$	$V_{IH}$	X	VDD	High Z
Standby	$V_{IH}$	$V_{IH}$	X	VDD	A[7:0]
Program	$V_{IH}$	$V_{PP}$	A1N	VDP	DIN
Erase 1	$V_{IH}$	$V_{PE}$	A8&A11 = $V_{IL}$ , A9 = $V_{PE}$ , A10 = $V_{IH}$ , Others = X	VDE	X
Erase 2	$V_{IH}$	$V_{PE}$	First command: Addr. = 5555 (hex)	VDE	AA(hex)
			Second command: Addr. = 2AAA (hex)	VDE	10(hex)
Product Identifier- manufacturer	$V_{IL}$	$V_{IL}$	A8 = $V_{IL}$ , A9 = $V_{HH}$ , Others = X	VDI	DA(Hex)
Product Identifier-device	$V_{IL}$	$V_{IL}$	A8 = $V_{IH}$ , A9 = $V_{HH}$ , Others = X	VDI	1F(Hex)



## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Ambient Temperature with Power Applied	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on all Pins with Respect to Ground Except $\overline{OE}/V_{PP}$ , A9 and VDD Pins	-2.0 to +7.0	V
Voltage on $\overline{OE}/V_{PP}$ Pin with Respect to Ground	-2.0 to +7.0	V
Voltage on A9 Pin with Respect to Ground	-2.0 to +7.0	V
Voltage VDD Pin with Respect to Ground	-2.0 to +14.0	V

Notes:

- Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.
- Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 nS. Maximum output pin voltage is VDD +0.75V DC which may overshoot to +7.0V for pulses of less than 20 nS.

### DC Erase Characteristics

(TA = 25° C ±5° C, VDD = 6.5V ±0.25V)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	VIN = VIL or VIH	-10	-	10	μA
VDD Erase Current	ICP	ALE = VIH, $\overline{OE}/V_{PP} = V_{PE}$ A8 & A11 = VIL, A9 = VPE, A10 = VIH, Others = X	-	-	30	mA
VPP Erase Current	IPP	ALE = VIH, $\overline{OE}/V_{PP} = V_{PE}$ A8 & A11 = VIL, A9 = VPE, A10 = VIH, Others = X	-	-	30	mA
Input Low Voltage	VIL	-	-0.3	-	0.8	V
Input High Voltage	VIH	-	2.4	-	VDD+0.3	V
Output Low Voltage (Verify)	VOL	IOL = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	VOH	IOH = -0.4 mA	2.4	-	-	-
A9 SID Voltage	VHH	VDD = 5V ±10%	11.5	12	12.5	V
A9 Erase Voltage	VPE	-	12.75	13	13.25	V
VPP Erase Voltage	VPE	-	12.75	13	13.25	V
VDD Supply Voltage (Erase & Erase Verify)	VDE	-	6.25	6.5	6.75	V

Note: VDD must be applied simultaneously or before VPP and removed simultaneously or after VPP.



**CAPACITANCE**

(V<sub>DD</sub> = 4.5V to 5.5V, T<sub>A</sub> = 25° C, f = 1 MHz)

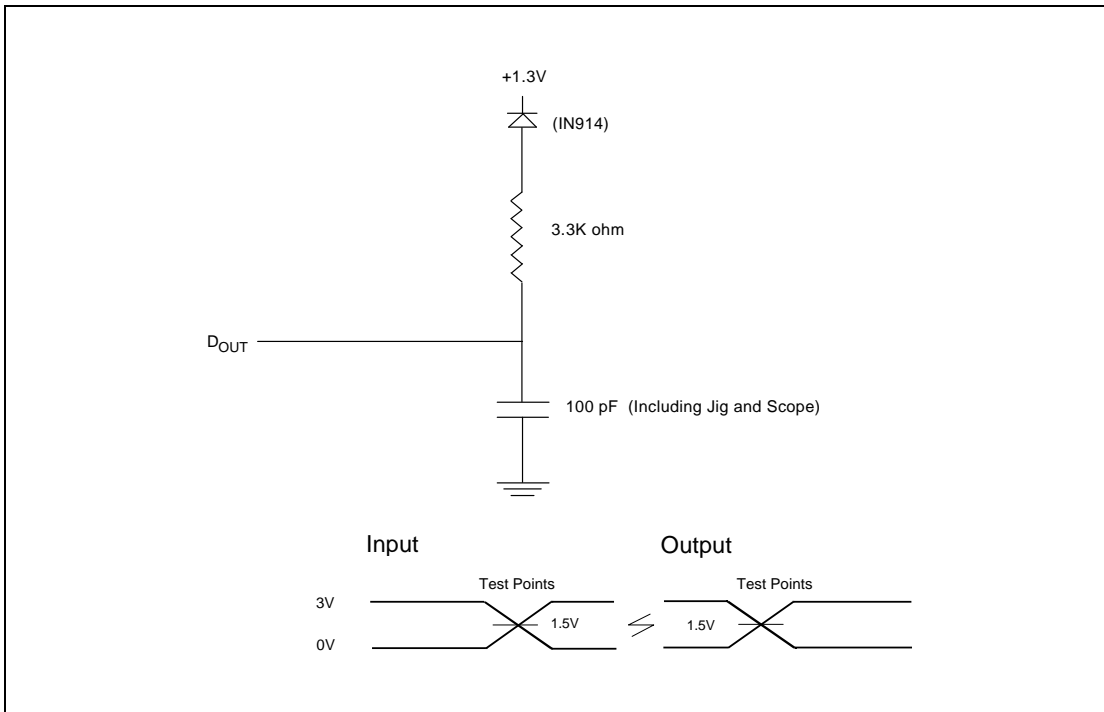
PARAMETER	SYMBOL		MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V	12	pF

**AC CHARACTERISTICS**

**AC Test Conditions**

PARAMETER	CONDITIONS
Input Pulse Levels	0V/3V
Input Rise and Fall Times	10 nS
Input and Output Timing Reference Level	1.5V/1.5V
Output Load	CL = 100 pF, I <sub>OH</sub> /I <sub>OL</sub> = -0.4 mA/2.1 mA

**AC Test Load and Waveforms**





**READ OPERATION DC CHARACTERISTICS**

(V<sub>DD</sub> = 4.5V to 5.5V, T<sub>A</sub> = 0 to 70° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>DD</sub>	-5	-	5	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> = 0V to V <sub>DD</sub>	-5	-	5	μA
Standby V <sub>DD</sub> Current (CMOS input)	I <sub>SB</sub>	ALE = V <sub>DD</sub> ±0.3V, $\overline{OE}/V_{PP}$ = V <sub>DD</sub> ±0.3V All others inputs = GND/ V <sub>DD</sub> ±0.3V	-	-	100	μA
V <sub>DD</sub> Operating Current	I <sub>DD</sub>	ALE = V <sub>IL</sub> , I <sub>OUT</sub> = 0 mA f = 5 MHz	-	-	20	mA
Input Low Voltage	V <sub>IL</sub>	-	-0.6	-	0.8	V
Input High Voltage	V <sub>IH</sub>	-	2.0	-	V <sub>DD</sub> +0.3	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	-	-	0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.4 mA	2.4	-	-	V

**READ OPERATION AC CHARACTERISTICS**

(V<sub>DD</sub> = 4.5V to 5.5V, T<sub>A</sub> = 0 to 70° C)

PARAMETER	SYM.	W27E520-70		W27E520-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address Latch Enable Access Time	T <sub>CE</sub>	-	70	-	90	nS
Address Latch Enable Width	T <sub>ALE</sub>	45	-	45	-	nS
Address Access Time	T <sub>ACC</sub>	-	70	-	90	nS
Address Setup Time	T <sub>AS</sub>	15	-	15	-	nS
Address Hold Time	T <sub>AH</sub>	15	-	15	-	nS
Output Enable Access Time	T <sub>OE</sub>	-	35	-	35	nS
$\overline{OE}/V_{PP}$ High to High-Z Output	T <sub>DF</sub>	-	25	-	25	nS
Output Hold from Address Change	T <sub>OH</sub>	0	-	0	-	nS

Note: V<sub>DD</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.



## DC PROGRAMMING CHARACTERISTICS

(V<sub>DD</sub> = 6.5V ±0.25V, T<sub>A</sub> = 25° C ±5° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-10	-	10	μA
V <sub>DD</sub> Program Current	I <sub>CP</sub>	ALE = V <sub>IH</sub> , $\overline{\text{OE}} / V_{PP} = V_{PP}$	-	-	30	mA
V <sub>PP</sub> Program Current	I <sub>PP</sub>	ALE = V <sub>IH</sub> , $\overline{\text{OE}} / V_{PP} = V_{PP}$	-	-	30	mA
Input Low Voltage	V <sub>IL</sub>	-	-0.3	-	0.8	V
Input High Voltage	V <sub>IH</sub>	-	2.4	-	V <sub>DD</sub> +0.5	V
Output Low Voltage (Verify)	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V <sub>OH</sub>	I <sub>OH</sub> = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	V <sub>HH</sub>	V <sub>DD</sub> = 5V ±10%	11.5	12.0	12.5	V
V <sub>PP</sub> Program Voltage	V <sub>PP</sub>	-	12.75	13.0	13.25	V
V <sub>DD</sub> Supply Voltage (Program)	V <sub>DP</sub>	-	6.25	6.5	6.75	V

## AC PROGRAMMING/ERASE CHARACTERISTICS

(V<sub>DD</sub> = 6.5V ±0.25V, T<sub>A</sub> = 25° C ±5° C)

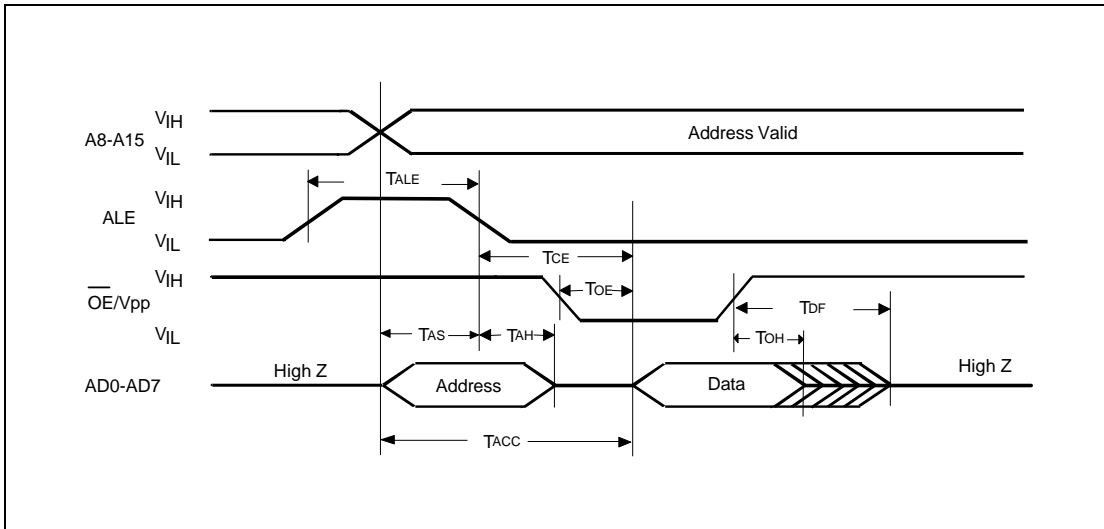
PARAMETER	SYM.	LIMITS			UNIT
		MIN.	TYP.	MAX.	
$\overline{\text{OE}} / V_{PP}$ Pulse Rise Time	TPRT	50	-	-	nS
Address Latch Enable Width	TALE	500	-	-	nS
ALE Program Pulse Width	TPPW	47.5	50	52.5	μS
ALE Erase Pulse Width	TEPW	95	100	105	mS
ALE Erase Pulse Width 1	TEPW1	47.5	50	52.5	μS
ALE Erase Pulse Width 2	TEPW2	95	100	105	mS
Latched Address Setup Time	TLAS	100	-	-	nS
Latched Address Hold Time	TLAH	100	-	-	nS
Address Setup Time	TAS	2.0	-	-	μS
Address Hold Time	TAH	0	-	-	μS
$\overline{\text{OE}} / V_{PP}$ Setup Time	TOES	2.0	-	-	μS
$\overline{\text{OE}} / V_{PP}$ Hold Time	TOEH	2.0	-	-	μS
Data Setup Time	TDS	2.0	-	-	μS
Data Hold Time	TDH	2.0	-	-	μS
Data Valid from $\overline{\text{OE}} / V_{PP}$ Low during Erase Verify	TEOE	-	-	150	nS
Data Valid from $\overline{\text{OE}} / V_{PP}$ Low during Program Verify	TPOE	-	-	150	nS
$\overline{\text{OE}} / V_{PP}$ High to Output High Z	TDFP	0	-	130	nS
$\overline{\text{OE}} / V_{PP}$ High Voltage Delay After ALE Low	TVS	2.0	-	-	μS
$\overline{\text{OE}} / V_{PP}$ Recovery Time	TVR	2.0	-	-	μS

Note: V<sub>DD</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.

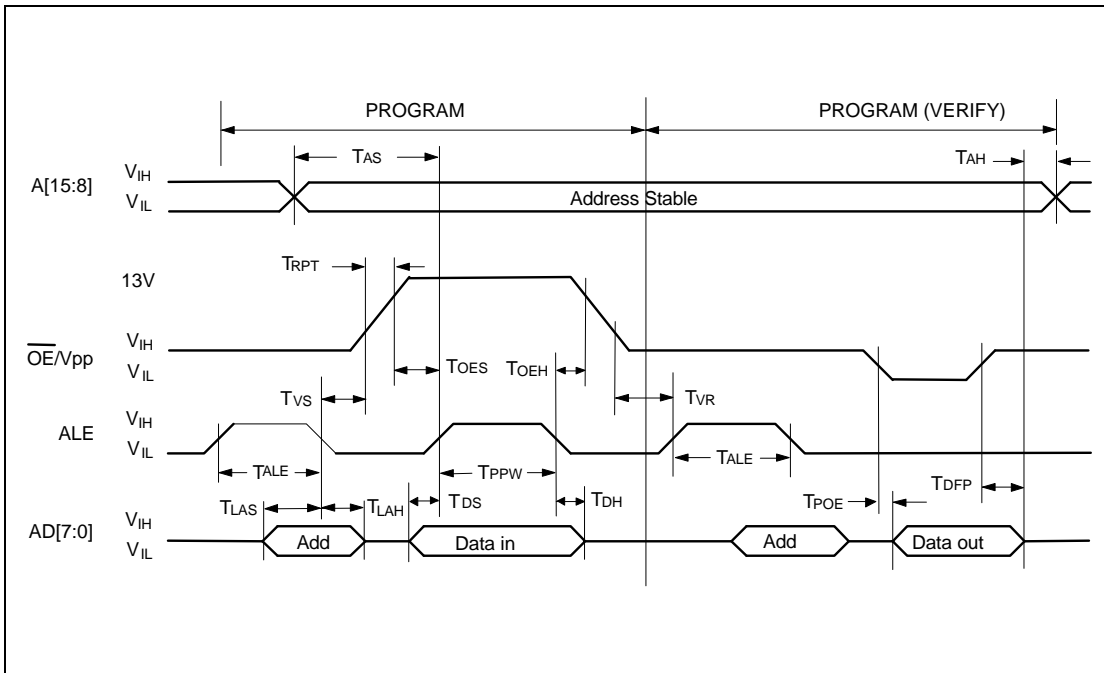
Publication Release Date: September 2000

**TIMING WAVEFORMS**

**AC Read Waveform**



**Programming Waveform**

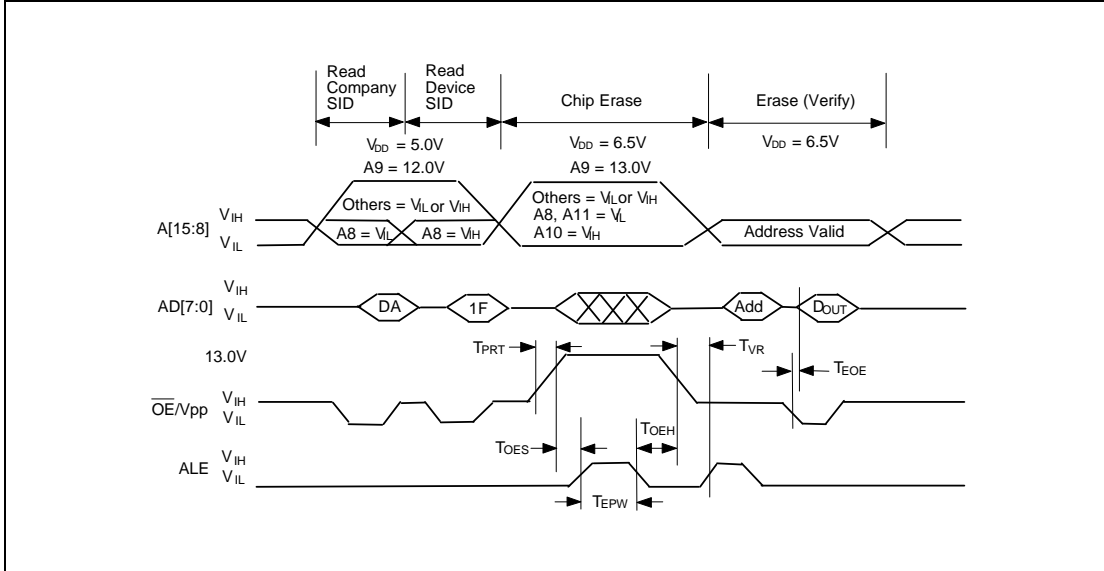




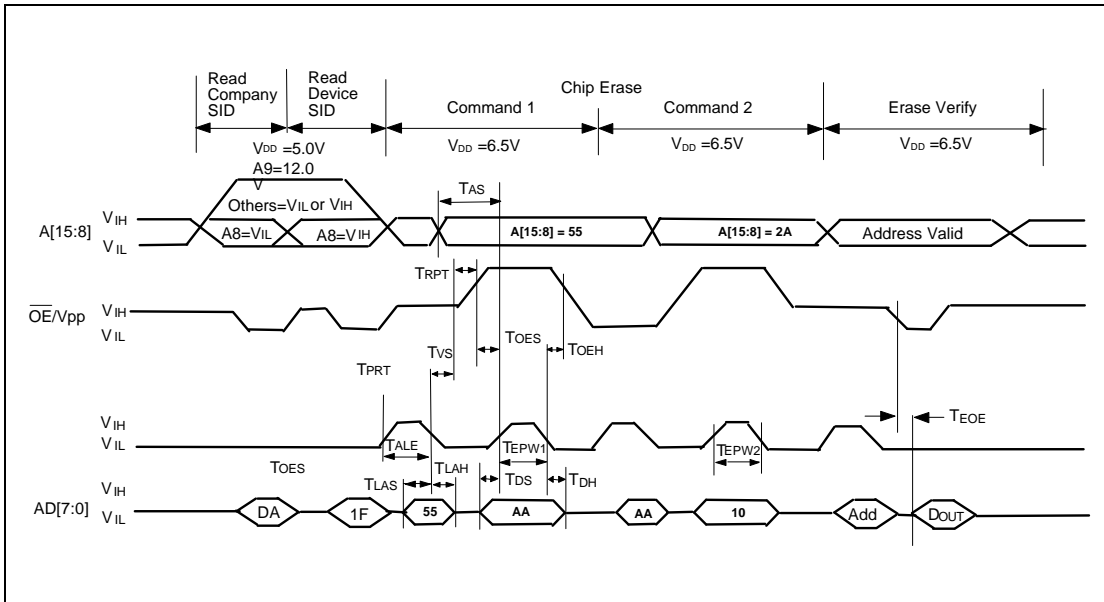


Timing Waveforms, continued

**Erase Waveform 1**

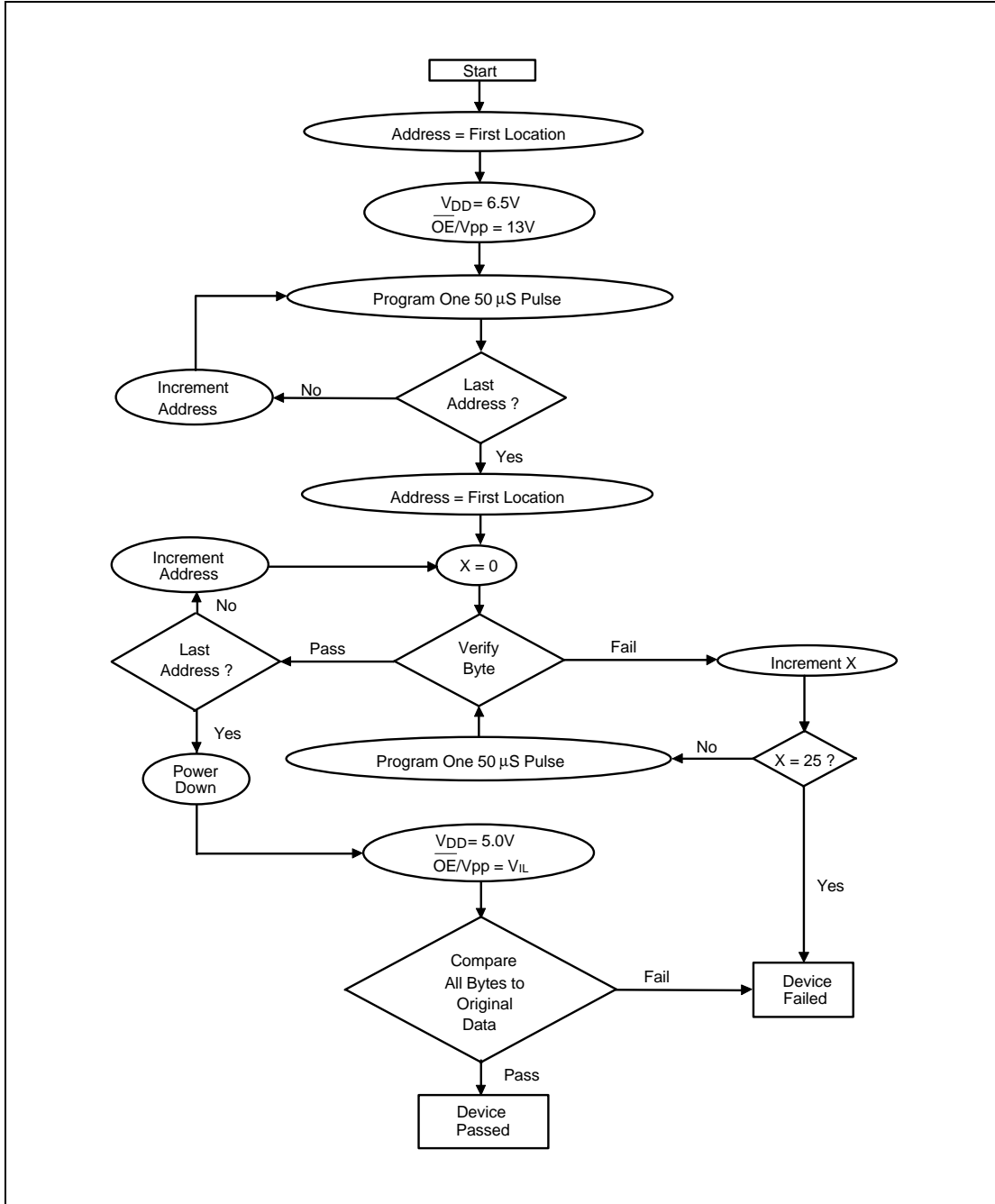


**Erase Waveform 2**

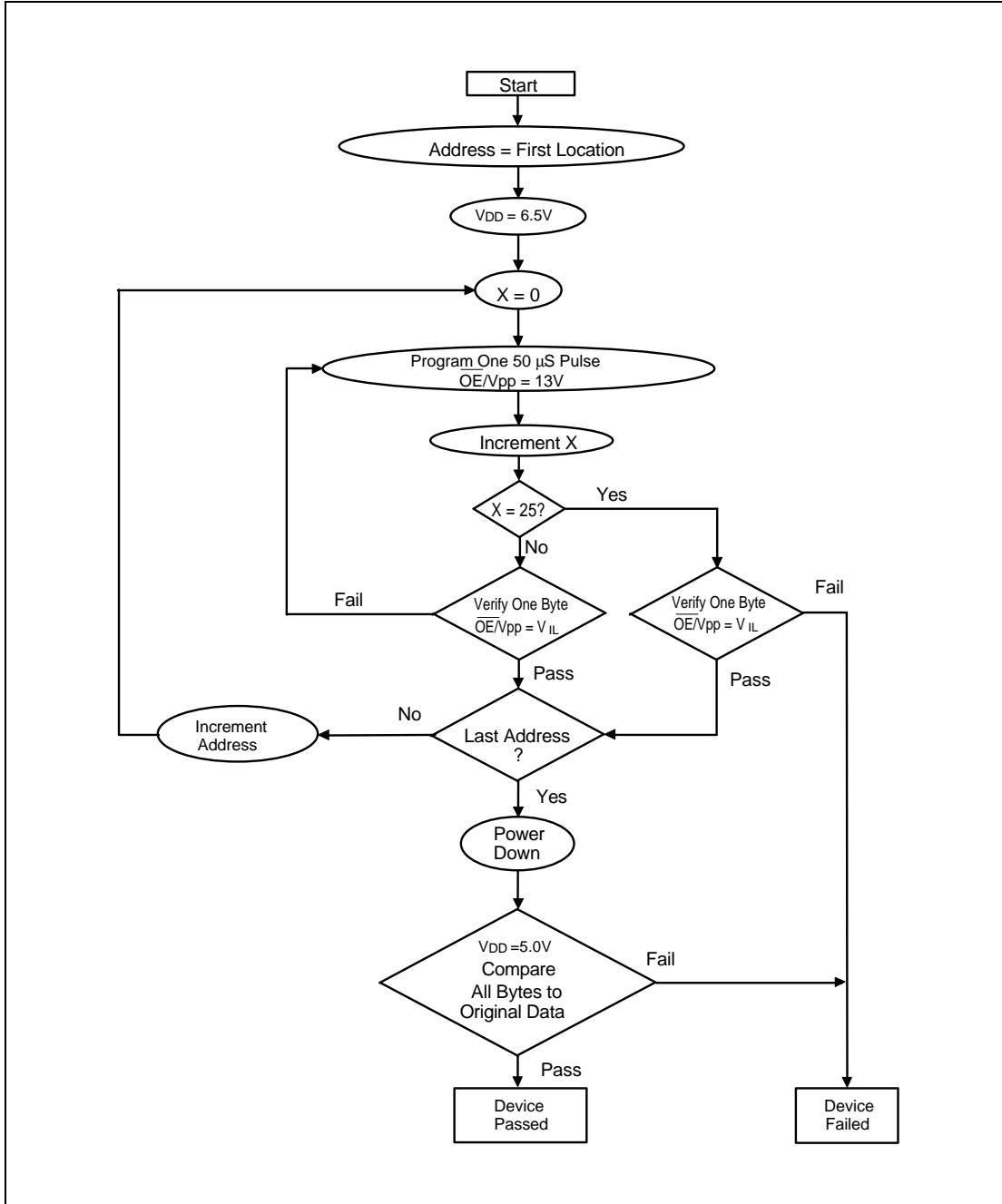


Note: First command Address = 5555(hex) with Data = AA(hex)  
 Second command Address = 2AAA(hex) with Data = 10(hex)

SMART PROGRAMMING ALGORITHM 1

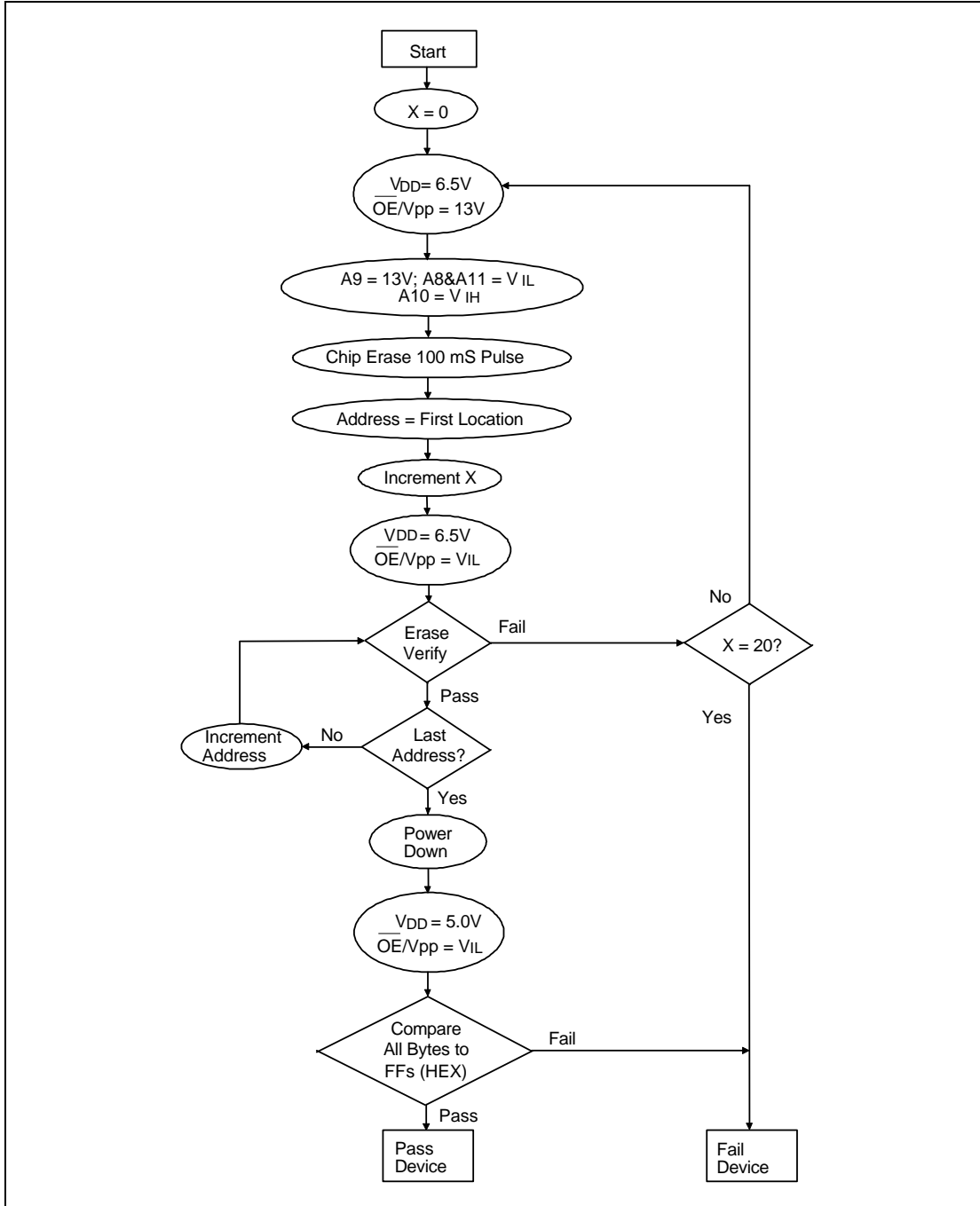


SMART PROGRAMMING ALGORITHM 2

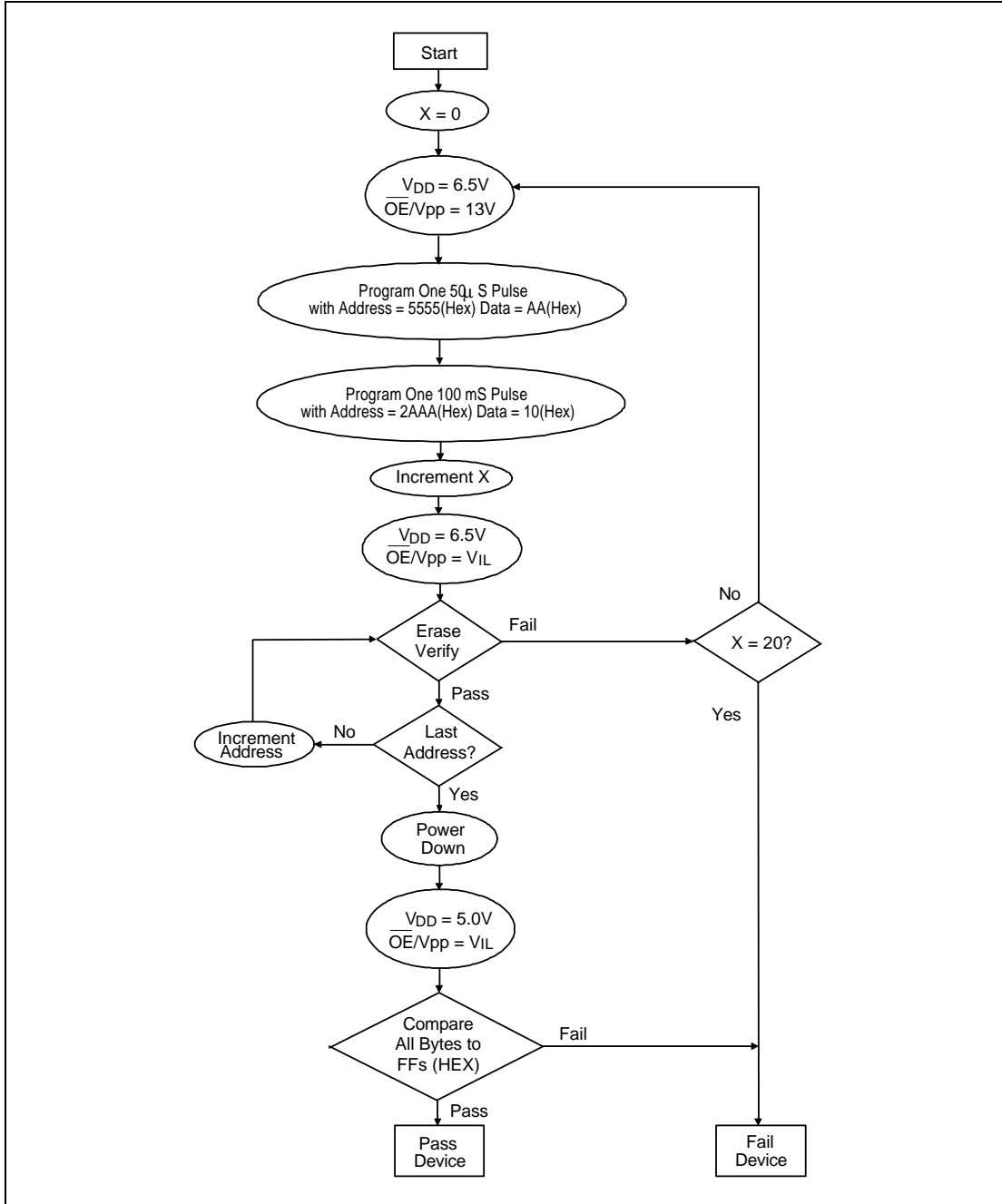




SMART ERASE ALGORITHM 1



SMART ERASE ALGORITHM 2



**ORDERING INFORMATION**

<b>PART NO.</b>	<b>ACCESS TIME (nS)</b>	<b>OPERATING CURRENT MAX. (mA)</b>	<b>STANDBY CURRENT MAX. (μA)</b>	<b>PACKAGE</b>
W27E520W-70*	70	20	100	173mil TSSOP
W27E520W-90*	90	20	100	173mil TSSOP
W27E520S-70*	70	20	100	300mil SOP
W27E520S-90*	90	20	100	300mil SOP

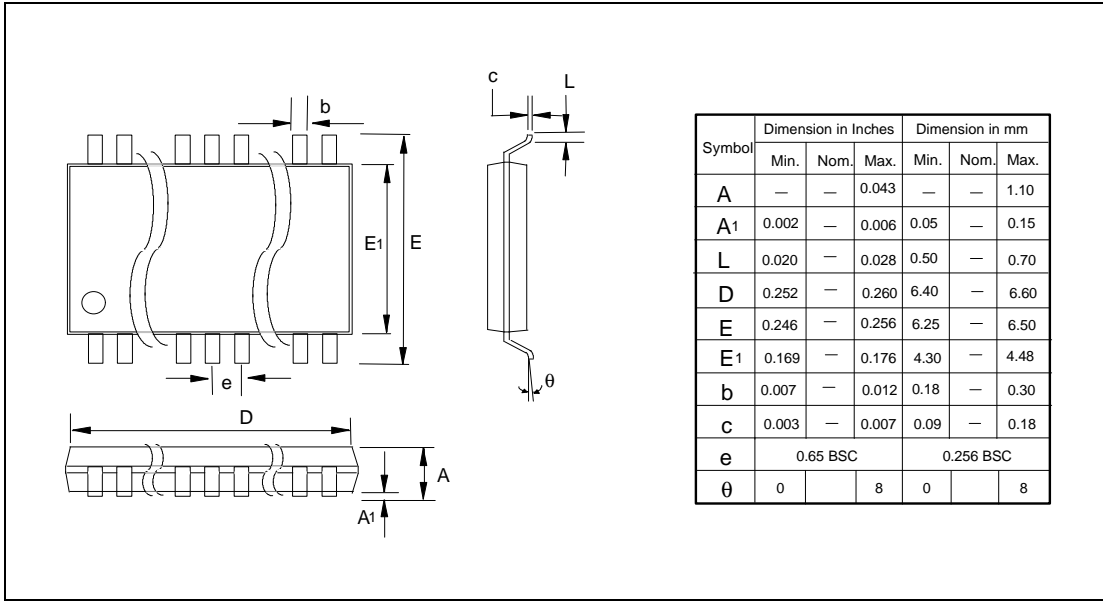
## Notes:

1. The Part No is preliminary and might be changed after project is consoled.
2. Winbond reserves the right to make changes to its products without prior notice.
3. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

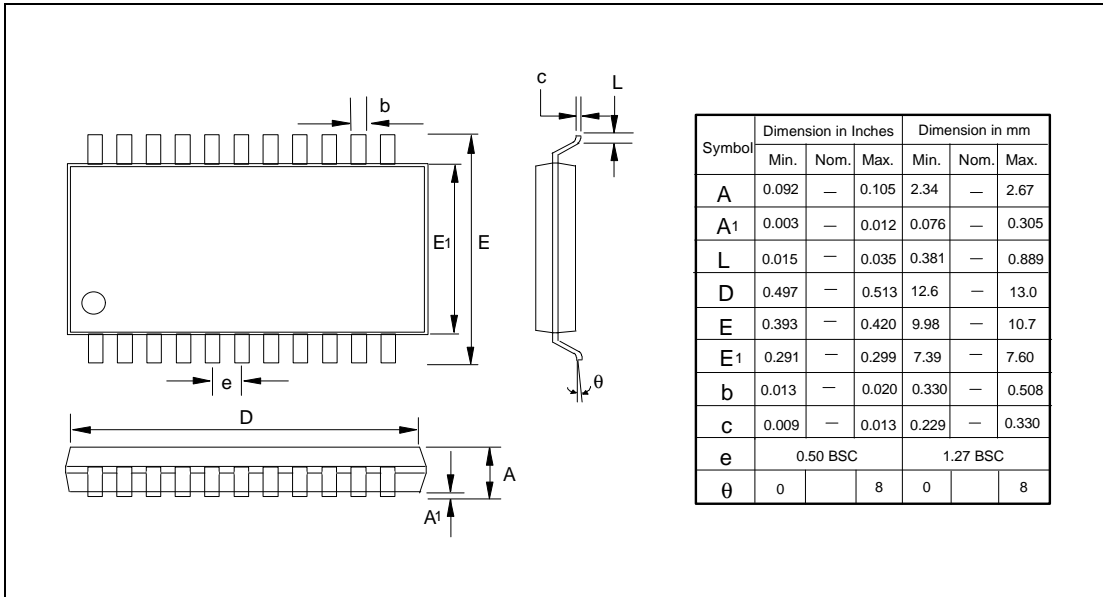


**PACKAGE DIMENSIONS**

**20-pin TSSOP**



**20-pin SOP**



**VERSION HISTORY**

VERSION	DATE	PAGE	DESCRIPTION
A1	Jun. 2000	-	Initial Issued
A2	Sep. 2000	9	Correct Erase Waveform
		3	Modify Address Latch Enable Mode: X -> Ain; Modify Output Disable Mode: VIL -> VIL/VIH; Modify Standby Mode: Ain -> X; Typo Correction
		1	Modify Feature description: LVTTTL -> TTL



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Note: All data and specifications are subject to change without notice.