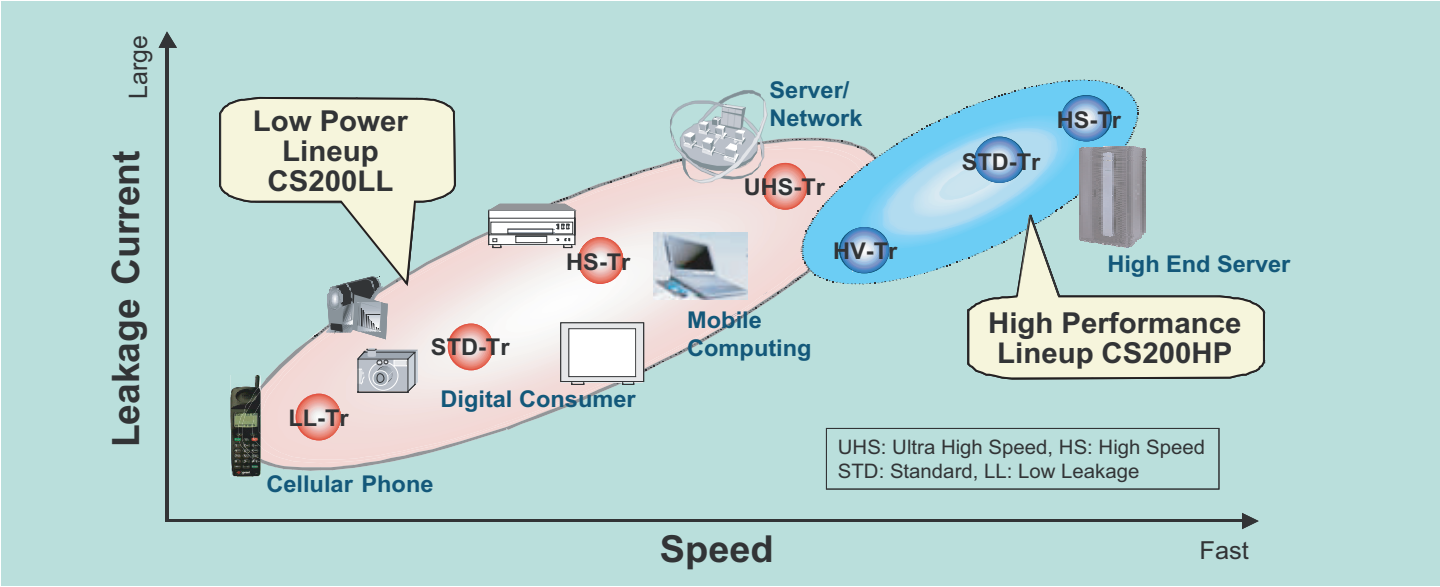
65nm CMOS Standard Cell

CS200 ASIC Series



Features

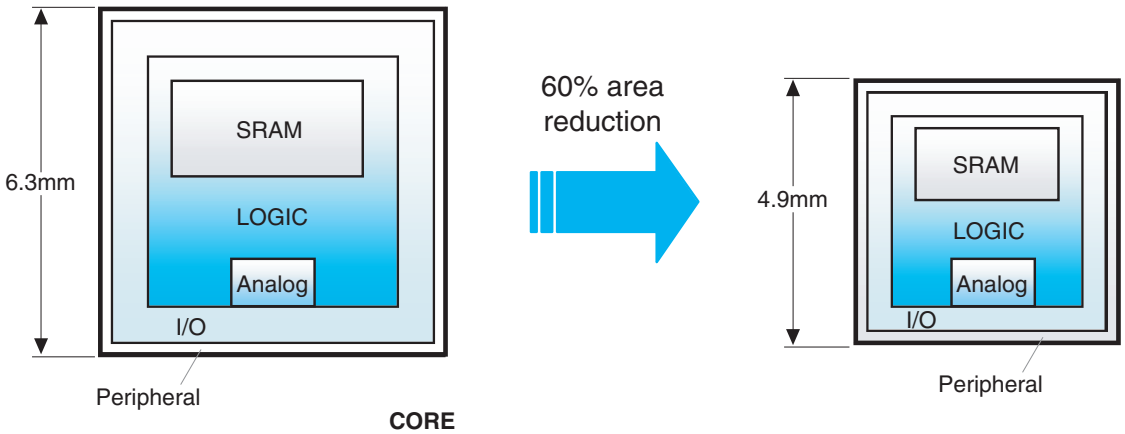
- High integration
  - Transistor of 30–50nm gate length (ITRS road map 65nm)
  - 12-layer fine pitch, copper wiring, and low-K insulating material techniques
  - Maximum 180 million gates, nearly twice that of 90nm technology
  - 50% reduction in SRAM cell size
  - 30% increase in performance over 90nm
- Low power consumption/low leakage current
- I/O with pad structure with fine pad pitch technology for chip size reduction
- High-speed library and low-power library available
  - High speed: CS200HP
  - Low leak: CS200L
- Higher performance, gate propagation delay tpd = 4.4ps (@1.2V, inverter, and F/O = 1, CS200HP)
- Compiled memory macros: 1T and 6T SRAMs, and ROM
- Application specific IPs
  - Computational cores: ARM7, 9, 11, Communication and Digital-AV DSP
  - Mixed signals: Wide range of ADCs and DACs
  - HSIF logics: PCI-Express, XAUI, SATA, DDR, USB, HDMI
- High-speed interface SerDes macros (~10Gbps data rate)
- Wide range of PLLs: standard to high-speed 1.6GHz
- Standard I/Os: LVTTL, SSTL, HSTL, LVDS, P-CML
- Wide supply voltage (0.80V to 1.30V for core)
- Triple Vth Transistor options
- Various packages available (QFP, FBGA, EBGA, PBGA, FC-BGA)
- Design methodology and support
  - Methodology in place to support multi-million-gates hierarchical designs
  - Excellent design center support at Sunnyvale and Dallas
  - Worldwide service organizations for global support

Description

CS200 Series, 65nm standard cells CMOS process technology, addresses the design challenges of the PDA and mobile computing market in low power and multi-functionality. It also addresses the need of ultra high performance design in leading-edge networking, server computing, and in complex telecom equipment applications. 65nm technology is available in 300mm fabrication and supports high volume wafer capacity in multiple manufacturing locations.

65nm CMOS Standard Cell

65nm compared to 90nm of the same design



CORE
- Logic: 4Mgate (Usage ratio 60%)
- Macro: 2Mgate (SRAM: 0.5M-bit, PLL etc.)

Specifications

Memory Macros and Compilers
- 1 RW SRAM in 16K X 40-bit Max. Configuration
- 2 RW SRAM in 4K X 18-bit Max. Configuration

Phase-Lock Loops
- Analog: up to 3.2Ghz
- DLL

I/O: High Speed Interface and Conventional IOs
- 2.5V and 3.3V LVCMOS
- P-CML, LVDS, SSTL, HSTL
- PCI Express, S-ATA, DDR, USB, DDR, HDMI, CDR
- 3.125Gbps XAUI, SFI, SPI

Mix-Signal Macros

ADC
- 8-bit 54MS/s
- 8-bit 110MS/s
- 10-bit 1MS/s
- 10-bit 33MS/s
- 10-bit 1110MS/s
- 12-bit 80MS/s Dual

DAC
- 8-bit 300kS/s
- 8-bit 1MS/s
- 10-bit 300kS/s
- 10-bit 1MS/s
- 10-bit 40MS/s
- 10-bit 54MS/s
- 10-bit 110MS/s

SoC IP Cores

Networking and Communication
- PCI-Express Link & PHY, S-ATA Link & PHY, SPI4, 10/100/1000 Ethernet

Processors and DSP
- ARM7, 9, 11, ARC, Tensilica

Std. Bus Controllers & Bus Bridges
- USB2.0 Device/Host Controller & PHY, PCI controller, SD/CF Card IF, I^2C, UART

Multimedia Access
- HDMI Link & PHY, JPEG, NTSC/PAL, DES/AES Encryption

Memory Controllers
- Mobile DDR, DDR2/3, FCRAM, SDRAM

FUJITSU MICROELECTRONICS AMERICA, INC.

Corporate Headquarters
1250 E. Arques Avenue, M/S 333, Sunnyvale, CA 94085-5401
Tel: (800) 866-8608 Fax: (408) 737-5999
E-mail: inquiry@fma.fujitsu.com Web Site: http://us.fujitsu.com/micro

Printed in the U.S.A. SMS-FS-21293-3/2008