6AM11

Silicon N-Channel/P-Channel Power MOS FET Array

HITACHI

Application

High speed power switching

Features

· Low on-resistance

$$\begin{split} & \text{N-channel:} \;\; R_{\text{DS(on)}} \quad 0.17 \quad \text{, } V_{\text{GS}} = 10 \; \text{V, } I_{\text{D}} = 2.5 \; \text{A} \\ & \text{P-channel:} \;\; R_{\text{DS(on)}} \quad 0.2 \quad \text{, } V_{\text{GS}} = -10 \; \text{V, } I_{\text{D}} = -2.5 \; \text{A} \end{split}$$

• Capable of 4 V gate drive

Low drive current

· High speed switching

• High density mounting

• Suitable for H-bridged motor driver

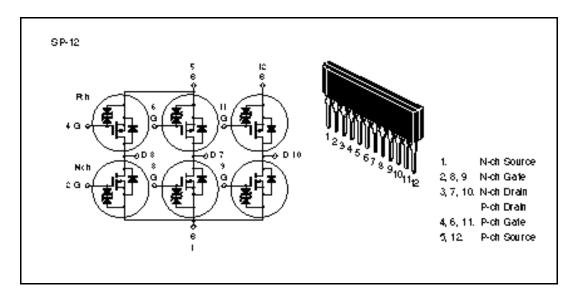
• Discrete packaged devices of same die:

N-channel: 2SK970, 2SK1093 P-channel: 2SJ172, 2SJ175



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Outline



Absolute Maximum Ratings (Ta = 25°C) (1 Unit)

		Ratings		
Item	Symbol	Nch	Pch	Unit
Drain to source voltage	$V_{\scriptscriptstyle DSS}$	60	-60	V
Gate to source voltage	$V_{\rm GSS}$	±20	±20	V
Drain current	I _D	5	- 5	Α
Drain peak current	I _{D(pulse)} *1	20	-20	Α
Body to drain diode reverse drain current	I _{DR}	5	- 5	A
Channel dissipation	Pch (Tc = 25°C)*2	36		W
	Pch*2	4.8		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	-55 to +150		°C

Notes: 1. PW 10 µs, duty cycle 1%

2. 6 Device Operation

Electrical Characteristics (Ta = 25°C) (1 Unit)

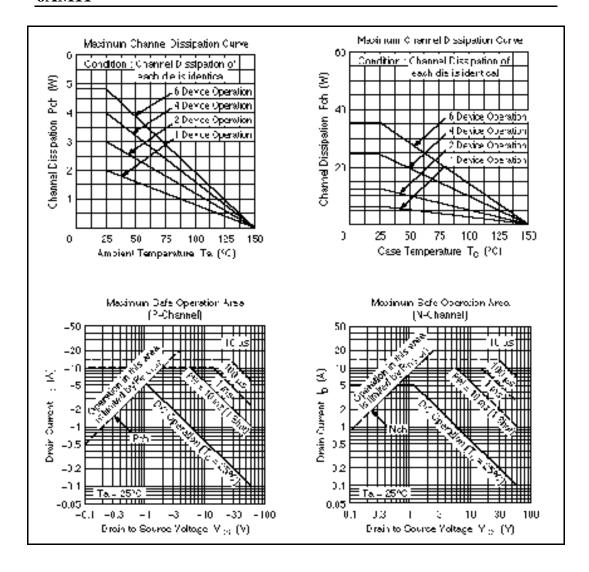
		N cha	annel	el P channel					
Item	Symbol	Min	Тур	Max	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	_	_	-60	_	_	V	$I_{D} = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	_	_	±20	_	_	V	$I_{G} = \pm 100 \ \mu A, \ V_{DS} = 0$
Gate to source leak current	I _{GSS}	_	_	±10	_	_	±10	μΑ	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_	_	250	_	_	-250	μΑ	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	_	2.0	-1.0	_	-2.0	V	$I_{D} = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{\mathrm{DS(on)}}$	_	0.13	0.17	_	0.15	0.2		$I_D = 2.5 \text{ A},$ $V_{GS} = 10 \text{ V}^{*1}$
		_	0.18	0.24	_	0.20	0.27		$I_D = 2.5 \text{ A}, V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	y _{fs}	2.7	4.5	_	2.7	5.0	_	S	$I_D = 2.5 \text{ A},$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	Ciss	_	400	_	_	900	_	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$
Output capacitance	Coss	_	220	_	_	460	_	pF	f = 1 MHz
Reverse transfer capacitance	Crss	_	60	_	_	130	_	pF	
Turn-on delay time	t _{d(on)}	_	5	_	_	8	_	ns	$I_D = 2.5 \text{ A}, V_{GS} = 10 \text{ V},$
Rise time	t _r	_	30	_	_	35	_	ns	R _L = 12
Turn-off delay time	$t_{d(off)}$	_	170	_	_	180	_	ns	-
Fall time	t _f	_	75	_	_	85	_	ns	-
Body to drain diode forward voltage	V_{DF}	_	1.0	_	_	-1.0	_	V	$I_F = 5 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t _{rr}		100	_		170	_	ns	$I_F = 5 \text{ A}, V_{GS} = 0,$ $diF/dt = 50 \text{ A/}\mu\text{s}$

Note: 1. Pulse Test

Polarity of test conditions for P channel device is reversed.

Pch: See characteristic curves of 2SJ172

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