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SGS-THOMSON MICROELECTRONICS

MK48Z08/18/09/19(B) -55/70/10/15/20

S G S-THOMSON 30E D

8 K X 8 ZEROPOWER™ SRAM

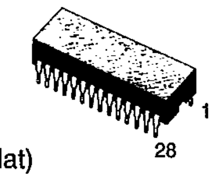
FEATURES

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES
  MK48Z08/09 - 4.50V ≤ V_{PFD} ≤ 4.75
  MK48Z18/19 - 4.20V ≤ V_{PFD} ≤ 4.50 .

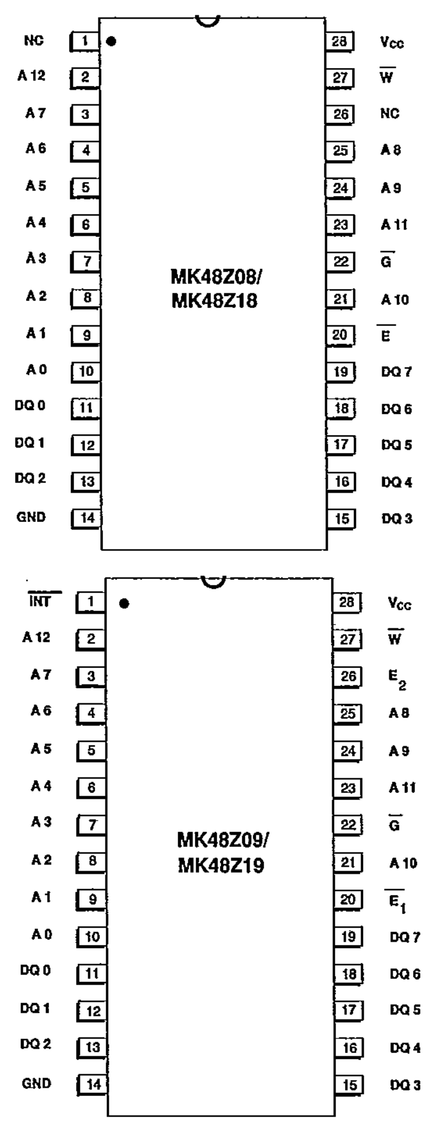
B

DIP-28

(Plastic with BatteryTop Hat)



PIN CONNECTIONS



DESCRIPTION

Part Number	Access Time	R/W Cycle Time
MK48ZXX-55	55 ns	55 ns
MK48ZXX-70	70 ns	70 ns
MK48ZXX-10	100 ns	100 ns
MK48ZXX-15	150 ns	150 ns
MK48ZXX-20	200 ns	200 ns

PIN NAMES

A0-A12	Address Input	Vcc	+5Volts
$\overline{E}$1	Chip Enable	$\overline{W}$	Write Enable
E2	Chip Enable	$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data In/Data Out
NC	No Connection	$\overline{INT}$	Power Fail Interrupt

DESCRIPTION

The MK48Z08/18/09/19 combines an 8K x 8 full CMOS SRAM and a long life lithium carbon monofluoride battery in a single plastic DIP package. The MK48Z08/18/09/19 is a nonvolatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z08/18/09/19 has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

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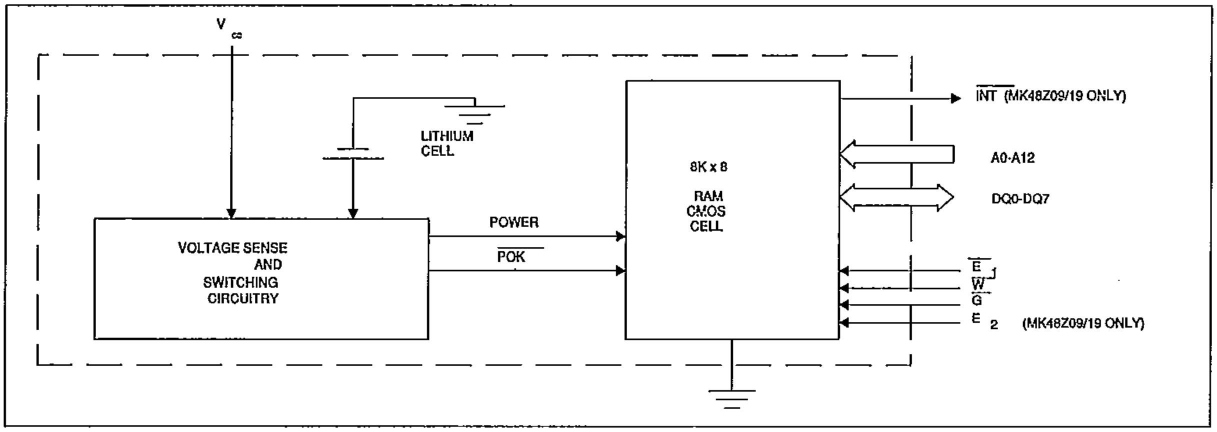
FIGURE 1 : MK48Z08 BLOCK DIAGRAM



TRUTH TABLE (MK48Z08/18)

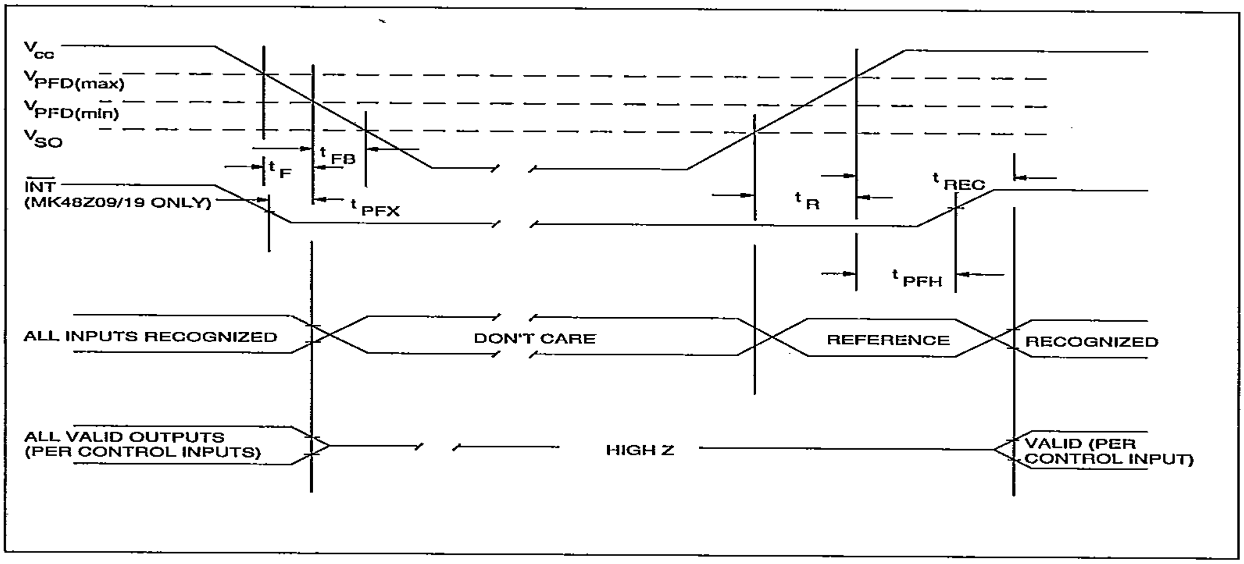
Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc	V_{IH}	X	X	Deselect	High Z	Standby
(Max)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
> Vcc	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
(Min)	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(Min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up

TRUTH TABLE (MK48Z09/19)

Vcc	$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc	V_{IH}	X	X	X	Deselect	High Z	Standby
(Max)	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	DIN	Active
> Vcc	V_{IL}	V_{IH}	V_{IL}	VIH	Read	D_{OUT}	Active
(Min)	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(Min) > V_{SO}	X	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	X	Deselect	High Z	Battery Back-up

NOTE 1 : Refer to Figure 2

FIGURE 2 : POWER DOWN/POWER UP TIMING.



REFERENCE :

Inputs may not be recognized at this time. Caution should be taken to keep $\overline{E}_1$ high or $\overline{E}_2$ low as VCC rises past VSO. **Some system may performs inadvernant write cycles** after V_{CC} rises above normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) ($0°C \le T_A \le +70°C$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs	
t_F	V_{PFD} (Max) to V_{PFD} (Min) Vcc Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	1		µs	
t_{REC}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		ms	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	µs	4

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS) ($0°C \le T_A \le +70°C$)

SYMBOL	PARAMETER	VALUE			UNITS	NOTES
		MIN	TYP	MAX		
V_{PFD}	Power-fail Deselect Voltage (MK48Z08/09)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z18/19)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	11			YEARS	

NOTES :

1. All voltages referenced to GND.

2. V_{PFD} (MAX) to V_{PFD} (MIN) fall time of less than t_F may result in deselection/write protection not occuring until 200 µs after Vcc passes V_{PFD} (MIN). V_{PFD} (MAX) to (MIN) fall times of less than 10 µs may cause corruption of RAM data.

3. V_{PFD} (MIN) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

4. $\overline{INT}$ may go high anytime after Vcc exceeds V_{SO} and is guaranteed to go high t_{PFH} after Vcc exceeds V_{PFD} (MAX).

READ MODE

The MK48Z08/18/09/19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$ is low, and E_2 is high (MK48Z09/19). The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and $\overline{G}$ access times are satisfied.

If Chip Enable or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and $\overline{G}$. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address inputs are changed while Chip Enable and $\overline{G}$ remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

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AC ELECTRICAL CHARACTERISTICS (READ CYCLE) (0°C ≤ T_A ≤ +70°C (Vcc (min) ≤ Vcc ≤ Vcc(max))

SYMBOL	PARAMETER	48ZXX-55/70/10/15/20		48ZXX-55		48ZXX-70		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{E1LQX}	Chip Enable 1 to Q Low-Z	10							
t_{E2HQX}	Chip Enable 2 to Q Low-Z	10							
t_{AXQX}	Output Hold from Address	5							
t_{GLQX}	Ouput Enable 1 to Q Low-Z	5							
t_{AVAV}	Read Cycle Time			55		70			
t_{AVQV}	Address Access Time				55		70	ns	
t_{E1LQV}	Chip Enable 1 Access Time				55		70		
t_{E2HQV}	Chip Enable 2 Access Time				55		70		
t_{GLQV}	Ouput Enable Access Time				55		70		
t_{E1HQZ}	Chip Enable 1 to Q High-Z				20		20		
t_{E2LQZ}	Chip Enable 2 to Q High-Z				20		20		
t_{GHQZ}	Output Disable to QHigh-Z				15		15		

SYMBOL	PARAMETER	48ZXX-10		48ZXX-15		48ZXX-20		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AVAV}	Read Cycle Time	100		150		200			
t_{AVQV}	Address Access Time		100		150		200		
t_{E1LQV}	Chip Enable 1 Access Time		100		150		200		
t_{E2HQV}	Chip Enable 2 Access Time		100		150		200	ns	
t_{GLQV}	Output Enable Access Time		50		75		100		
t_{E1HQZ}	Chip Enable 1 to Q High-Z		50		75		100		
t_{E2LQZ}	Chip Enable 2 to Q High-Z		50		75		80		
t_{GHQZ}	Output Disable to Q High-Z		40		60		80		

FIGURE 3 : READ TIMING N°.1 (ADDRESS ACCESS)

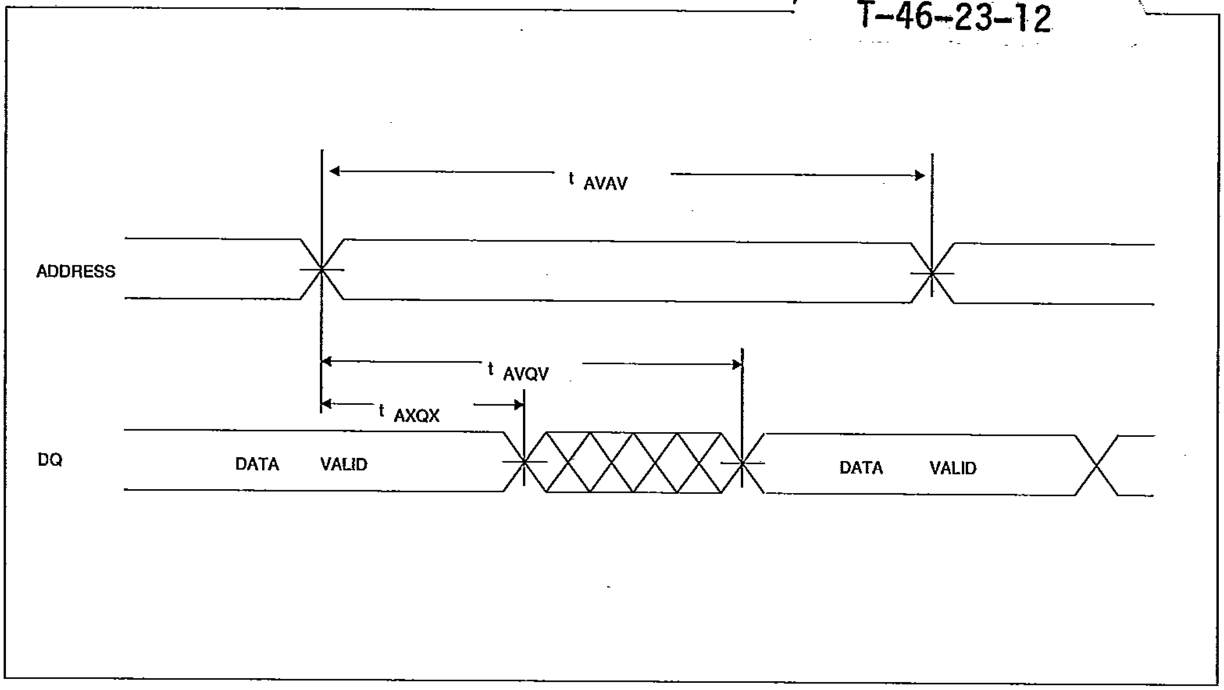
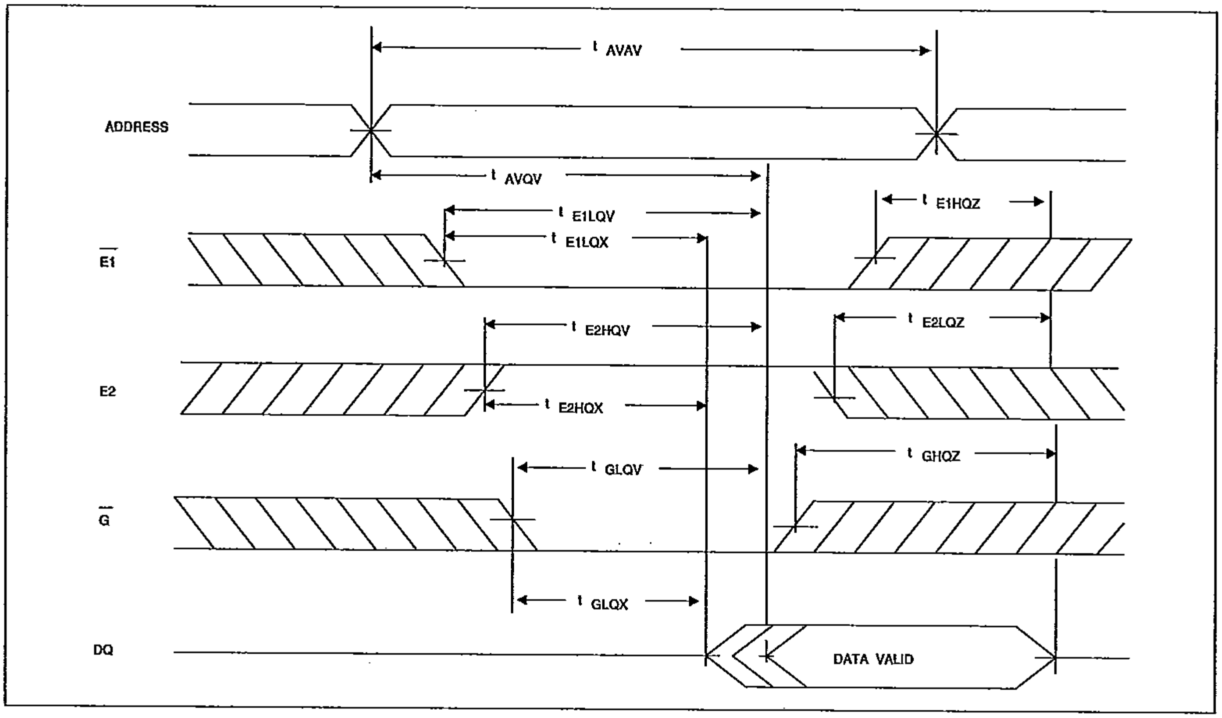


FIGURE 4 : READ TIMING N°.2



WRITE MODE

The MK48Z08/18/09/19 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E_1}$ or rising edge of E_2 (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E_1}$ or the falling edge of E_2 (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E_1}$ or $\overline{W}$ must return high or E_2 low for minimum of t_{E1HAX} or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} prior to the end of write and remain valid for t_{WHDX} afterward. Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

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AC ELECTRICAL CHARACTERISTICS(WRITE CYCLE)(0°C ≤ T_A ≤ +70°C (Vcc (min) ≤ Vcc ≤ Vcc(max))

SYMBOL	PARAMETER	48ZXX-55/70/10/15/20		48ZXX-55		48ZXX-70		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0							
t_{AVE1L}	Address Set-Up Time to ChipEnable Active	0							
t_{AVE2H}		0							
t_{E1HAX}	Write Recovery from Chip Enable (Address Hold Time)	10							2
t_{E2LAX}		10							2
t_{WHDX}	Data Hold Time	5							1,2
t_{AVAV}	Write Cycle Time			55		70		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High			35		50			
t_{WLWH}	Write Pulse Width			35		50			
t_{WHAX}	Address Hold after End of Write			10		10			1
t_{E1LE1H}	Chip Enable Active to End of Write (W High)			35		50			2
t_{E2HE2L}				35		50			2
t_{DVWH}	Data Valid to End of Write			25		40			1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z				30		40		

SYMBOL	PARAMETER	48ZXX-10		48ZXX-15		48ZXX-20		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AVAV}	WriteCycle Time	100		150		200			
t_{AVWH}	Address Valid to $\overline{W}$ High	80		130		180			
t_{WLWH}	Write Pulse Width	80		100		150			
t_{WHAX}	Address Hold after End of Write	10		10		10		ns	1
t_{E1LE1H}	Chip Enable Active to End of Write (W High)	80		130		180			2
t_{E2HE2L}		80		130		180			2
t_{DVWH}	Data Valid to End of Write	50		70		80			1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		50		75		100		

NOTES : **1.** In a $\overline{W}$ Controlled Cycle / **2.** In a $\overline{E_1}$, E2 Controlled Cycle

FIGURE 5 : WRITE CONTROL WRITE CYCLE TIMING

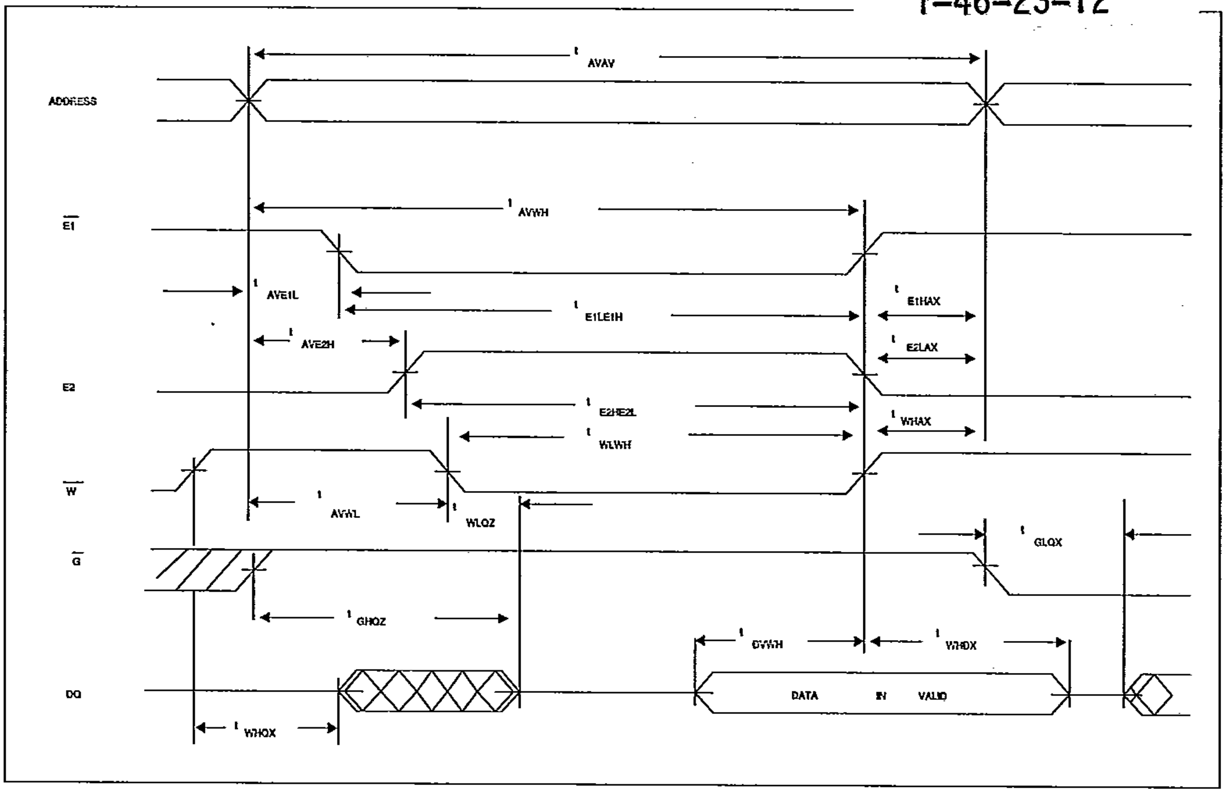
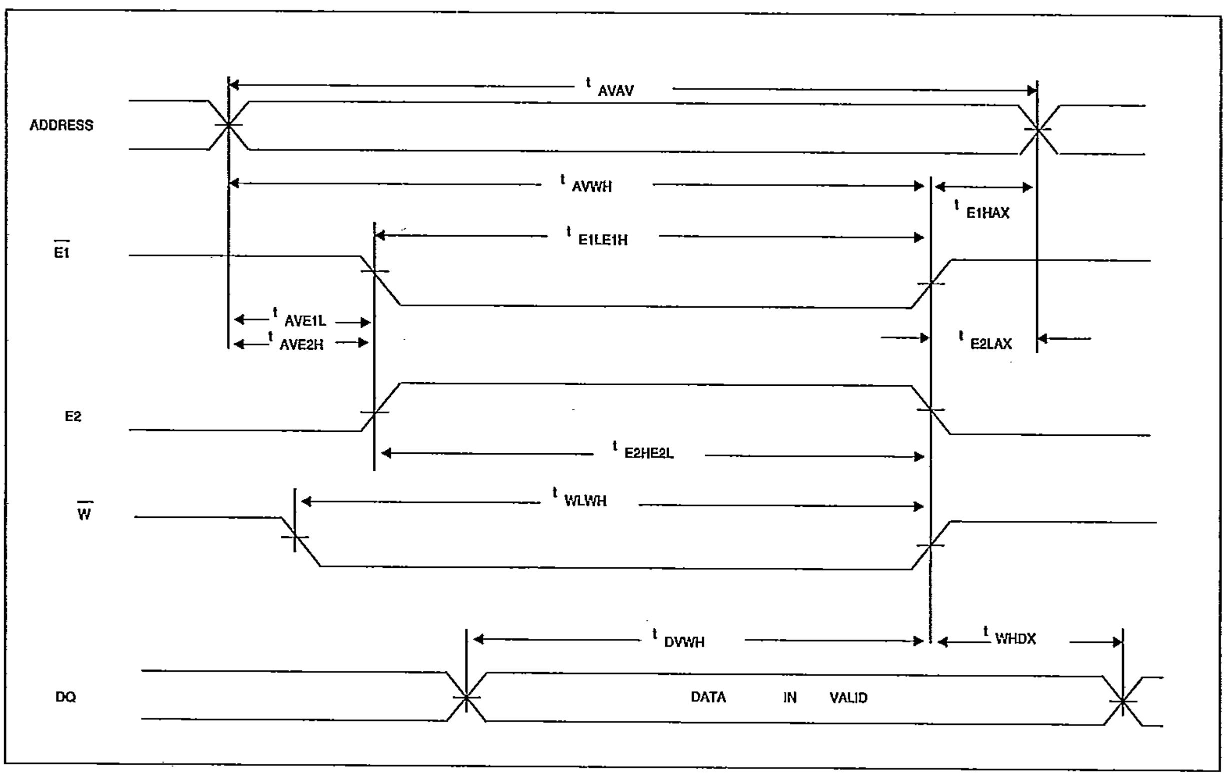


FIGURE 6 : CHIP ENABLE CONTROL WRITE CYCLE TIMING



DATA RETENTION MODE

With V_{CC} applied, the MK48Z08/18/09/19 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48Z08/18/09/19 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E_1}$ high (MK48Z08/18) or E_2 low (MK48Z09/19) as V_{CC} rises past V_{SO} as some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48Z09/19 continuously monitors Vcc. When Vcc fall to the power fail detect trip point of the MK48Z09/19 an interrupt is immediatly generated. An internal clock provides a delay no less than 10µS but no greater than 40µS before automatically deselecting the MK48Z09/19.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48Z08/18/09/19 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

With V_{CC} on, the battery is disconnected from the RAM and aging effects become the determining factor in battery life. With V_{CC} off, leakage currents in the RAM provide the only load on the Battery during battery back-up. For the MK48Z08/18/09/19, the leakage currents are so low that the Back-up System life of the device is simply the Storage Life of the cell. The Storage Life of the cell is a function of temperature.

PREDICTING STORAGE LIFE

Figure 7 illustrates how temperature affects Storage Life of the MK48Z08/18/09/19 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48Z08/18/09/19.

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Storage Life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

A Special Note: The summary presented in Figure 8 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. The are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48Z08/18/09/19 is marked with a five digit manufacturing date code in the form XYYWW. The first digit is the assembly location code (example: 98625= assembled in Muar Malasia, 1986, week 25).

Calculating Predicted Storage Life of the Battery

As Figure 7 indicates, the predicted Storage Life of the battery in the MK48Z08/18/09/19 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 7. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

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Example Predicted Storage Life Calculation

Predicted Storage Life = $1 \div \{ [(TA_1 \div TT) \div SL_1] + [(TA_2 \div TT) \div SL_2] + ... + [(TA_N \div TT) \div SL_N] \}$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + ... + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 7)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48Z08 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

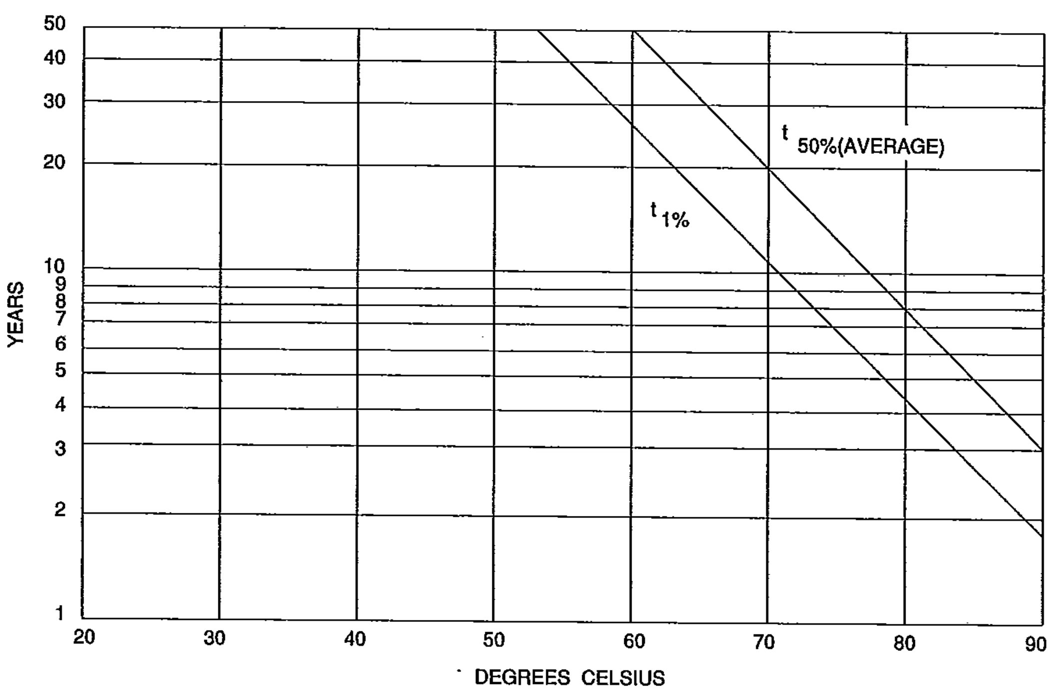
Reading Predicted $t_{1\%}$ values from Figure 7; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

Predicted Typical Storage Life ≥ $1 \div \{ [(8322 \div 8760) \div 41] + [(438 \div 8760) \div 11.4]$

Predicted Typical Storage Life ≥ 36 years

FIGURE 7 : PREDICTED BATTERY STORAGE LIFE VS. TEMP.



ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUE	UNIT
Total Power Dissipation	1.0	W
Output Current per Pin	20	mA
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (Vcc on) Temperature (T_A)	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION
Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vcc	Supply Voltage (MK48Z08/09)	4.75	5.5	V	1
Vcc	Supply Voltage (MK48Z18/19)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS(0°C≤ T_A ≤+70°C) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Icc1	Average Vcc Power Supply Current		80,125	mA	3,6
Icc2	TTL Standby Current ($\overline{E}_1$= V_{IH} or E_2=V_{IL})		3	mA	
Icc3	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	-1	+1	µA	5
I_{OL}	Ouput Leakage Current	-5	+5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5 mA)		0.4	V	

NOTES :

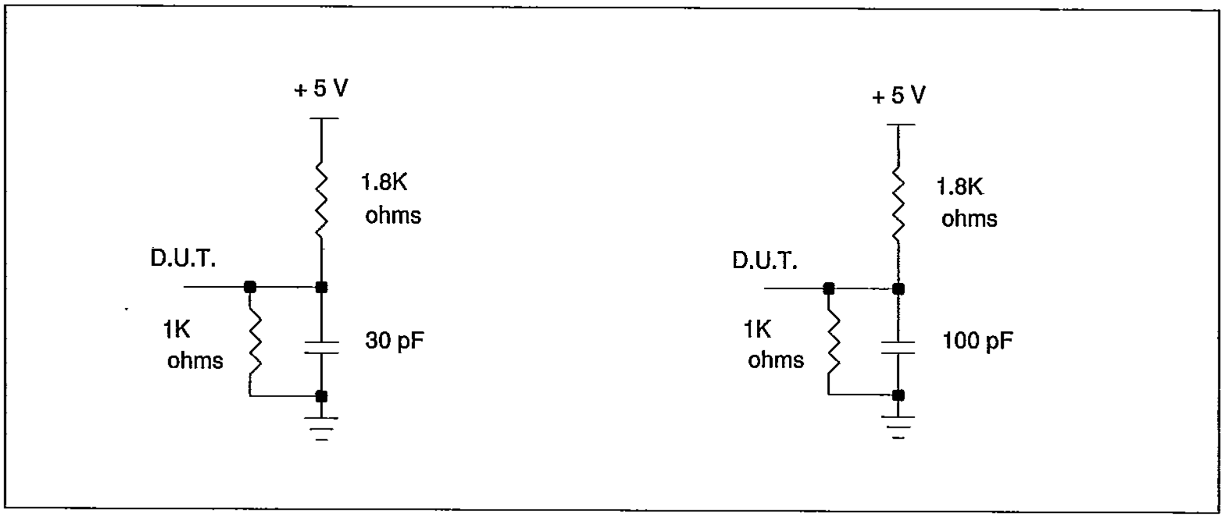
1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V_I ≥ GND and outputs deselected.
6. 80mA@ 100,150,200ns, & 125mA@ 55,70ns

AC TEST CONDITIONS

INPUT LEVELS ______________ 0.0v to 3.0v
TRANSITION TIMES ________ 5ns
INPUT AND OUTPUT TIMING REFERENCE LEVELS ________ 1.5v

FIGURE 8 : OUPUT LOAD DIAGRAM

MK48Z08/18/09/19-55/70 MK48Z08/18/09/19-10/15/20



CAPACITANCE (T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
CI	Capacitance On All Pins (except DQ)	10.0	pF	1
CQ	Capacitance On DQ Pins	10.0	pF	1,2

NOTE :
1. Effective capacitance calculated from the equation C = I Δt/ΔV with ΔV = 3 volts and power supply at 5.0V
2. Measured with outputs deselected.

ORDERING INFORMATION

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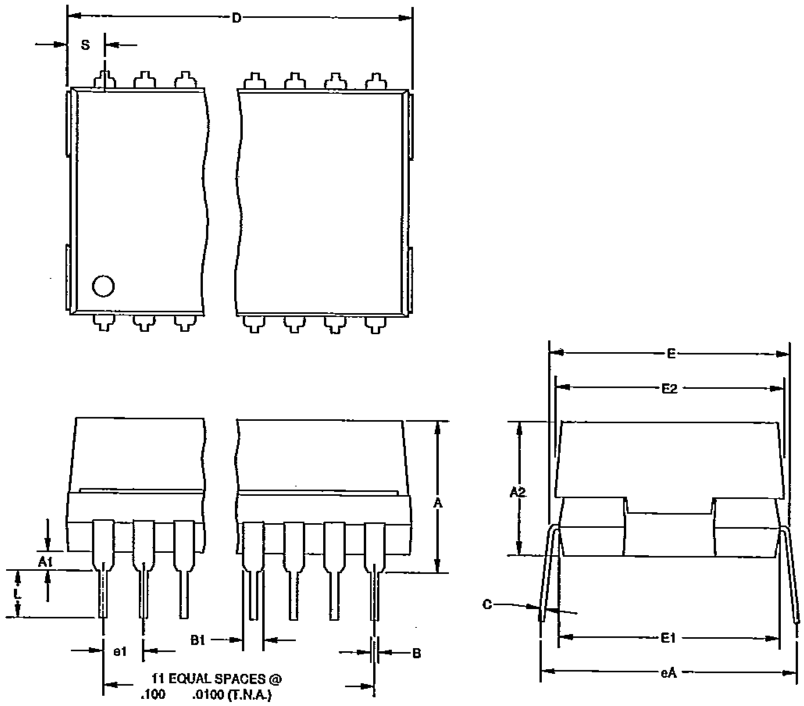
PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE
MK48Z08-B55	55	5V ±10%
MK48Z08-B70	70	5V ±10%
MK48Z08-B10	100	5V ±10%
MK48Z08-B15	150	5V ±10%
MK48Z08-B20	200	5V ±10%
MK48Z18-B55	55	5V +10 -5%
MK48Z18-B70	70	5V +10 -5%
MK48Z18-B12	100	5V +10 -5%
MK48Z18-B15	150	5V +10 -5%
MK48Z18-B20	200	5V +10 -5%
MK48Z09-B55 (PFI)	55	5V ±10%
MK48Z09-B70 (PFI)	70	5V ±10%
MK48Z09-B10 (PFI)	100	5V ±10%
MK48Z09-B12 (PFI)	150	5V ±10%
MK48Z09-B20 (PFI)	200	5V ±10%
MK48Z19-B55 (PFI)	55	5V +10 -5%
MK48Z19-B70 (PFI)	70	5V +10 -5%
MK48Z19-B10 (PFI)	100	5V +10 -5%
MK48Z19-B15 (PFI)	150	5V +10 -5%
MK48Z19-B20 (PFI)	200	5V +10 -5%

FIGURE 9 : PACKAGE MECHANICAL DATA

T-46-23-12



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.495	1
E	.530	.640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.