

# ECH8505 — PNP Epitaxial Planar Silicon Transistor

## Motor Drive Applications

### Features

- Composite type, facilitating high-density mounting.
- Mounting height 0.9mm.
- Halogen free compliance.

### Specifications

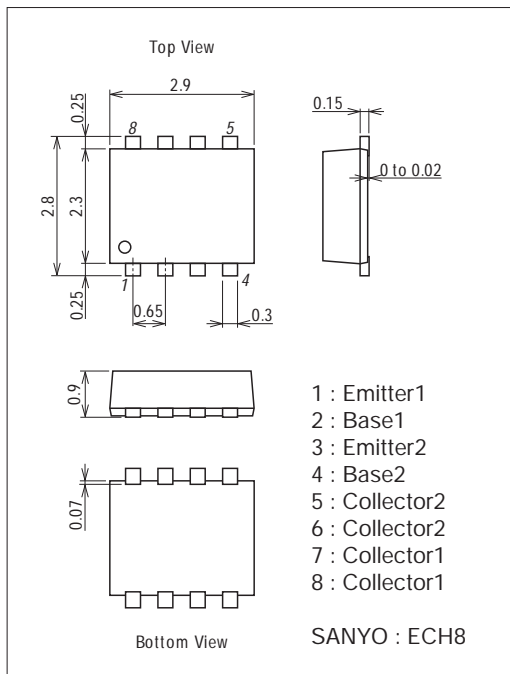
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	VCBO		-180	V
Collector-to-Emitter Voltage	VCEO		-160	V
Emitter-to-Base Voltage	VEBO		-7	V
Collector Current	IC		-1.5	A
Collector Current (Pulse)	ICP		-3	A
Base Current	IB		-300	mA
Collector Dissipation	PC	When mounted on ceramic substrate (900mm <sup>2</sup> ×0.8mm) 1unit	1.3	W
Total Dissipation	PT	When mounted on ceramic substrate (900mm <sup>2</sup> ×0.8mm)	1.6	W
Junction Temperature	TJ		150	°C
Storage Temperature	Tstg		-55 to +150	°C

### Package Dimensions

unit : mm (typ)

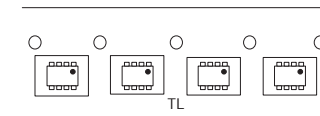
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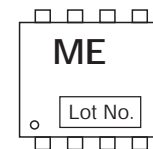
### Product & Package Information

- Package : ECH8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

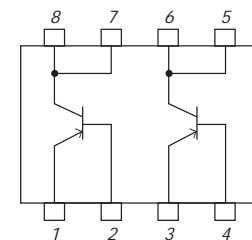
### Taping Type : TL



### Marking



### Electrical Connection

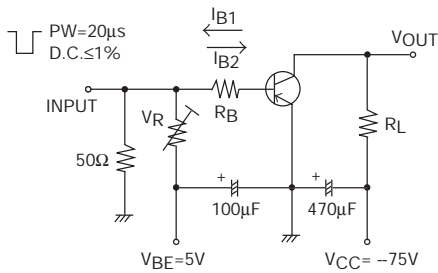


Electrical Characteristics at Ta=25°C

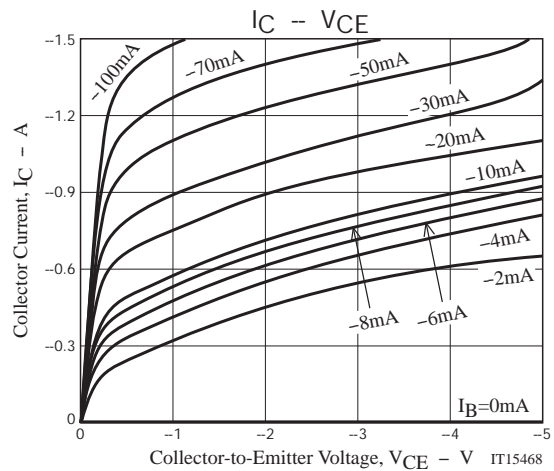
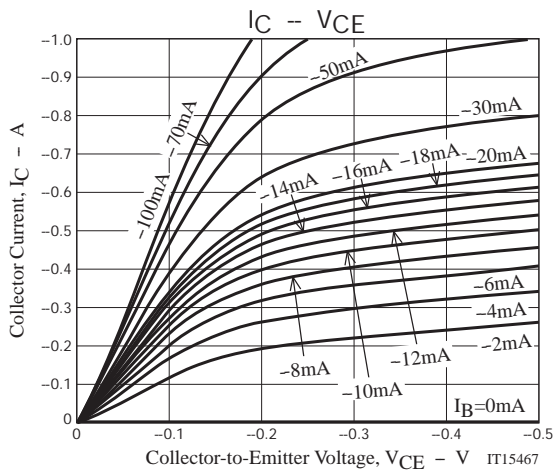
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	$I_{CBO}$	$V_{CB} = -80V, I_E = 0A$			-1	$\mu A$
Emitter Cutoff Current	$I_{EBO}$	$V_{EB} = -4V, I_C = 0A$			-1	$\mu A$
DC Current Gain	$h_{FE}$	$V_{CE} = -5V, I_C = -100mA$	200		560	
Gain-Bandwidth Product	$f_T$	$V_{CE} = -10V, I_C = -100mA$		85		MHz
Output Capacitance	$C_{ob}$	$V_{CB} = -10V, f = 1MHz$		21		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -500mA, I_B = -50mA$		-90	-160	mV
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -500mA, I_B = -50mA$		-0.9	-1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -10\mu A, I_E = 0A$	-180			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -1mA, R_{BE} = \infty$	-160			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -10\mu A, I_C = 0A$	-7			V
Turn-On Time	$t_{on}$	See specified Test Circuit.		25		ns
Storage Time	$t_{stg}$	See specified Test Circuit.		970		ns
Fall Time	$t_f$	See specified Test Circuit.		30		ns

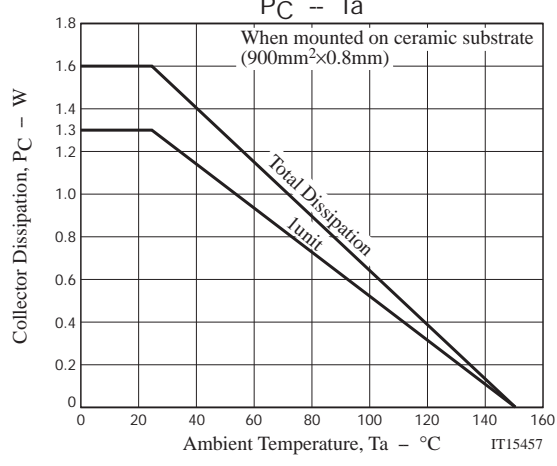
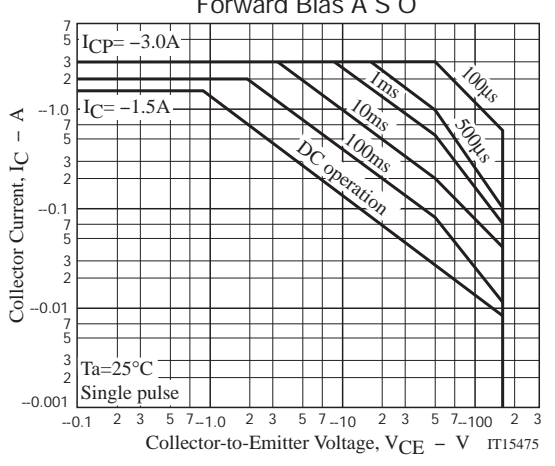
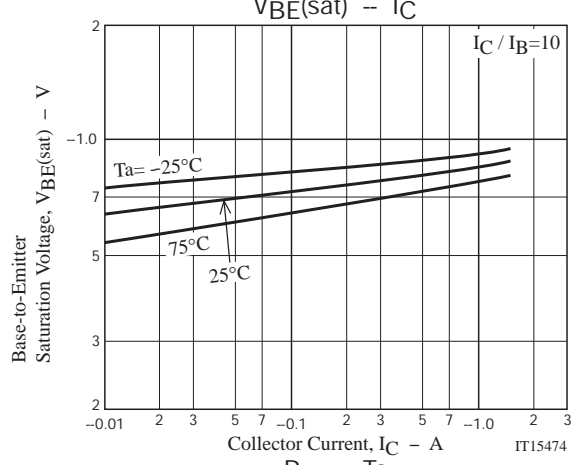
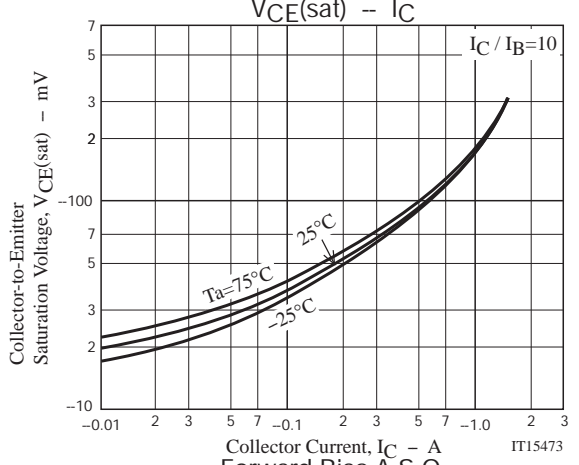
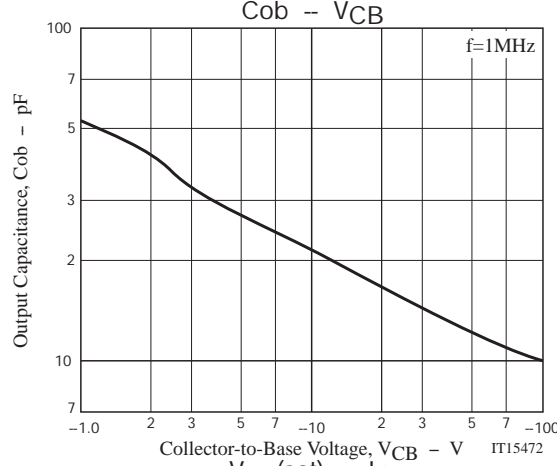
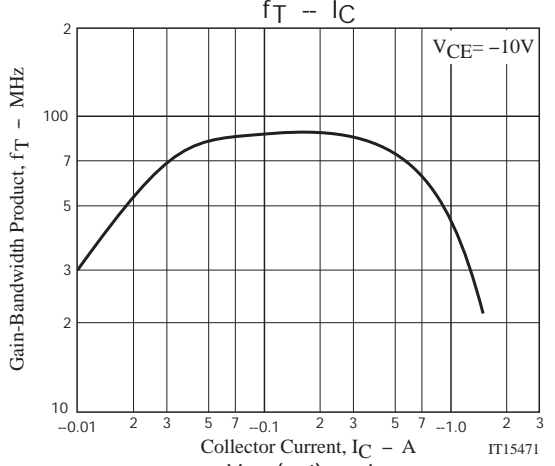
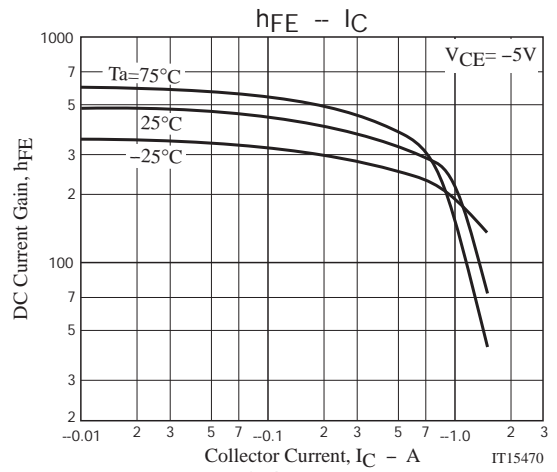
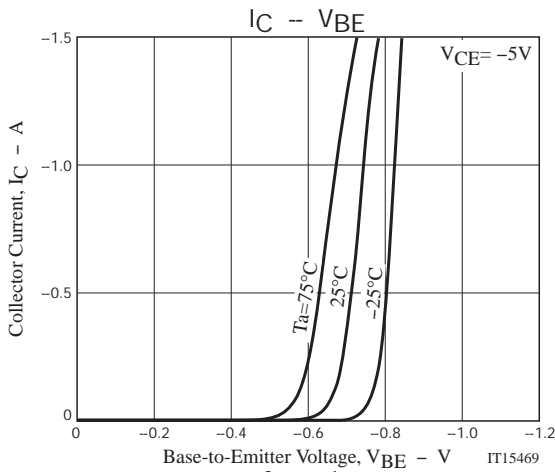
Note) The specifications shown above are for each individual transistor.

Switching Time Test Circuit



$$I_C = -10I_{B1} = 10I_{B2} = -0.7A$$





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