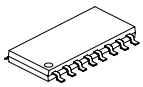
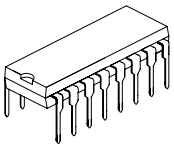
8-Bit Constant Current LED Driver

DESCRIPTION

SD16730 is a special constant current driver for LED display application. The value of constant current can be determined with external resistor. It bases on BICMOS technology and includes an 8-bit shift register. Latch and constant current driver. At the output stage, there are eight regulated current sources which provide 2-80mA constant current for driving LEDs by Bipolar Junction Transistor.



SOP-16-300-1.27



DIP-16-300-2.54

FEATURES

* Output current adjustable through an external resistor
* Serial data in/out
* 8 constant-current output channels
* Output current: 2-80mA
* 20MHz clock frequency
* Current accuracy (All output ON)

Current accuracy		Output current
Between Bits	Between ICs	
<±3%	<±6%	10 to 60mA

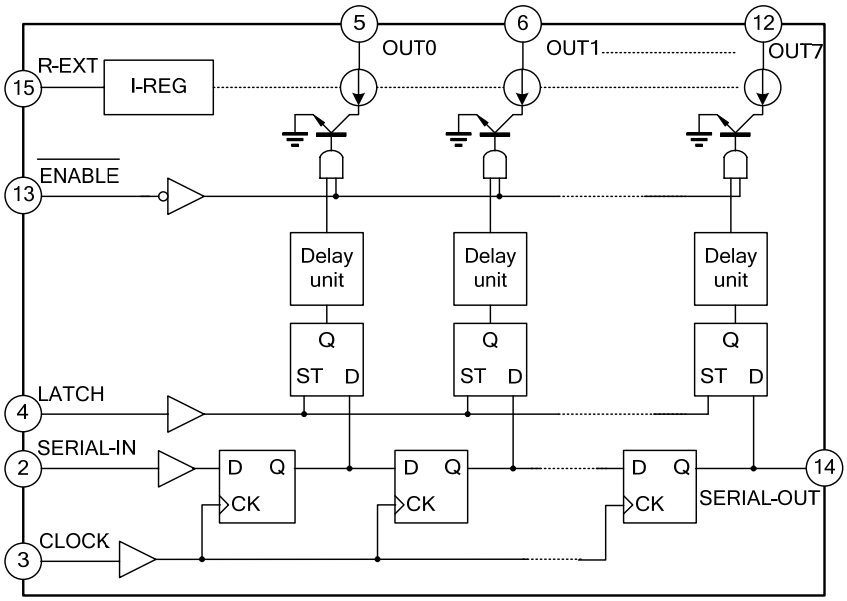
APPLICATIONS

* LED guardrail diode

ORDERING INFORMATION

Device	Package	Seal
SD16730	DIP-16-300-2.54	SD16730
SD16730S	SOP-16-300-1.27	SD16730S

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Tamb=25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Input Voltage	V_{IN}	-0.2~V_{DD}-0.2	V
Output Current	I_{OUT}	90	mA/ch
Output Voltage	V_{OUT}	-0.2~ 17	V
Power Dissipation	P_{D1}	1.25	W
Storage Temperature	T_{stg}	-55~+150	°C
Operating Temperature	T_{opr}	-40 ~ 85	°C

RECOMMENDED OPERATE CONDITION

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	-	3.0	-	5.5	V
Output Voltage	V_{OUT}	-	-	0.7	4.0	V
Output Current	I_{OUT}	-	2	-	80	mA/ch
	I_{OH}	SERIAL-OUT	-	-	1	mA
	I_{OL}	SERIAL-OUT	-	-	-1	mA
Input Voltage	V_{IH}	-	0.74V_{DD}	-	V_{DD}+ 0.15	V
Input Voltage	V_{IL}	-	-0.15	-	0.26V_{DD}	V
Clock Frequency	F_{clk}	Cascade connected	-	-	20	MHz
Setup Time For LATCH	$T_{SU(L)}$	-	50	-	-	nS

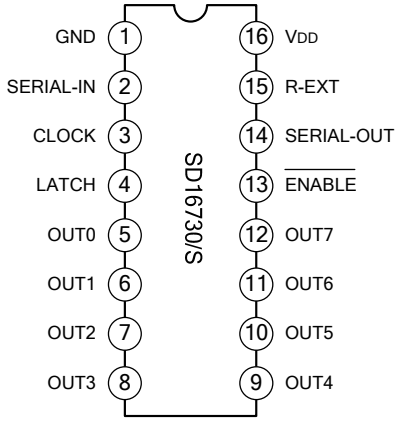
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Hold Time For LATCH	$T_{h(L)}$		50	-	-	nS
CLOCK Pulse Width	t_{CLK}		25	-	-	nS
ENABLE Pulse Width	t_{ENA}	Upper I_{OUT} = 20 mA	175	-	-	nS
		Lower I_{OUT} = 20 mA	130	-	-	nS
Setup Time For CLOCK	$T_{su(C)}$	-	10	-	-	nS
Hold Time For CLOCK	$T_{h(C)}$	-	10	-	-	nS

ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, V_{DD}=3.0V-5.5V unless otherwise specified)

Characteristics	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	-		3.0	-	5.5	V
Output Current	I_{OUT1}	V_{DD}=3.3V V_{OUT}=0.4V	R_{EXT}=490Ω	31.96	36.20	40.54	mA
	I_{OUT2}	V_{DD}=5.0V V_{OUT}=0.4V		31.59	35.90	40.02	mA
	I_{OUT3}	V_{DD}=3.3V V_{OUT}=0.7V	R_{EXT}=250Ω	63.63	72.30	80.97	mA
	I_{OUT4}	V_{DD}=5.0V V_{OUT}=0.7V		62.75	71.30	79.95	mA
Output Leakage Current	Iok	V_{OUT}=15.0V		-	-	1	uA
Output Current (Bit to Bit)	△Iout1	V_{OUT}>0.4V	R_{EXT}=490Ω	-	±1	±3	%
	△Iout2	V_{OUT}>0.4V	R_{EXT}=250Ω				
Output Voltage (SOUT)	V_{OH}	I_{OH}=-1.0 mA, V_{DD}=3.3 V		3	-	-	V
		I_{OH}=-1.0 mA, V_{DD}=5.0 V		4.7	-	-	V
	V_{OL}	I_{OL}=1.0 mA, V_{DD}=3.3 V		-	-	0.3	V
		I_{OL}=1.0 mA, V_{DD}=5.0 V		-	-	0.3	V
Output Current Regulation	%/V_{DD}	V_{DD}:3.0V—5.0V		-	-1	-5	%
Pull-down Resistor	$R_{IN(down)}$	-		115	230	460	kΩ
Pull-up Resistor	$R_{IN(up)}$	-		115	230	460	kΩ
Supply Current OFF	I_{OFF}	V_{out}=15.0V, OPEN		-	0.1	0.5	mA
		V_{out}=15.0V,R_{EXT}=490Ω		1	3.5	5	mA
		V_{out}=15.0V,R_{EXT}=250Ω		4	6	9	mA
Supply Current ON	I_{ON}	V_{OUT}=0.7V,R_{EXT}=490Ω		-	5.5	15	mA
		V_{OUT}=0.7V,R_{EXT}=250Ω		-	10.5	25	mA
	I_{ON}	V_{OUT}=0.7V,T_{amb}=-40°C, R_{EXT}=490Ω		-	-	20	mA
		V_{OUT}=0.7V,T_{amb}=-40°C , R_{EXT}=250Ω		-	-	40	mA
Propagation Delay Time (“L” to “H”)	T_{pLH1}	CLK— $\overline{OUTn}$, LATCH= “H”, $\overline{ENABLE}$ =“L”		-	140	300	nS
	T_{pLH2}	LATCH— $\overline{OUTn}$, $\overline{ENABLE}$ =“L”		-	140	300	nS
	T_{pLH3}	$\overline{ENABLE}$ — $\overline{OUTn}$, LATCH =“H”		-	140	300	nS
	T_{pLH4}	CLK—SERIAL OUT		3	6	-	nS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Propagation Delay Time ("H" to "L")	T_{pHL1}	CLK— $\overline{OUTn}$, LATCH = "H", $\overline{ENABLE}$ ="L"	-	170	340	nS
	T_{pHL2}	LATCH— $\overline{OUTn}$, $\overline{ENABLE}$ ="L"	-	170	340	nS
	T_{pHL3}	$\overline{ENABLE}$ — $\overline{OUTn}$, LATCH ="H"	-	170	340	nS
	T_{pHL4}	CLK—SERIAL OUT	4	7	-	nS
Output Rise Time	t_{or}	-	40	85	150	nS
Output Fall Time	t_{of}	-	40	70	150	nS
Maximum CLOCK Rise Time	t_r	-	-	-	5	uS
Maximum CLOCK Fall Time	t_f	-	-	-	5	uS

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	GND	--	Ground terminal
2	SERIAL-IN	I	Input terminal of a data shift register
3	CLOCK	I	Input terminal of a clock shift register
4	LATCH	I	Input terminal of a data strobe
5 ~ 12	$\overline{OUT0}$ ~ $\overline{OUT7}$	O	Output terminals
13	$\overline{ENABLE}$	I	Input terminal of output enable (low active)
14	SERIAL-OUT	O	output terminal of a data shift register
15	R-EXT	I	Input terminal of an external resistor
16	VDD	--	Supply voltage terminal

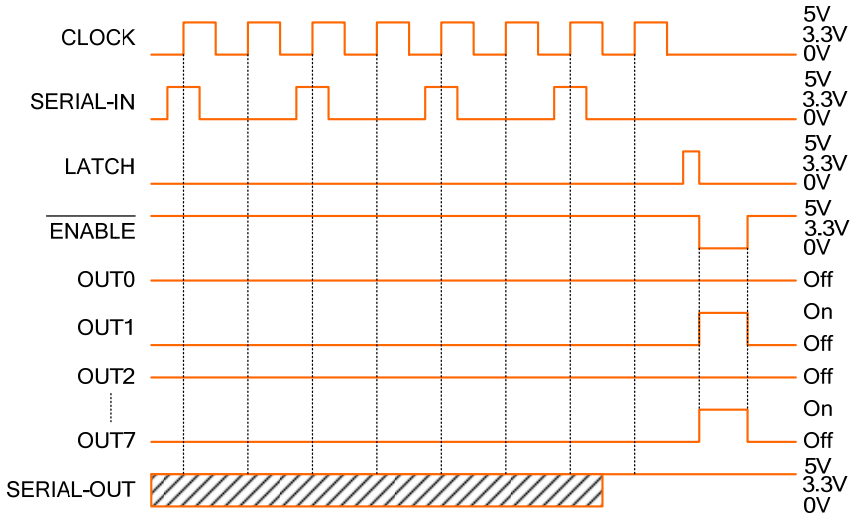
FUNCTION DESCRIPTION

In LED display application, SD16730 can maintain the current nearly no variations among different channels or chips. The maximum current variation range is ±3% between channels and ±6% between chips.

This device has only one ground pin shared by signal, output sink current, and power ground. It is advisable to pattern the ground layout with minimized inductance so that the switching noise induced by the input signals and the output sink current would not cause chip malfunction. To prevent drivers' outputs from damaging by

overshoot stresses, it is also advisable not to turn off the drivers and scan transistors simultaneously.
In order to obtain an ideal constant current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage from the character table. Even under the same output current condition, the minimum output voltage required for each part is different.
The resistor should be placed as close as possible to the R-EXT terminal to avoid the noise influence.

TIMING DIAGRAM



Note: The latches circuit holds data when LATCH terminal goes low voltage.

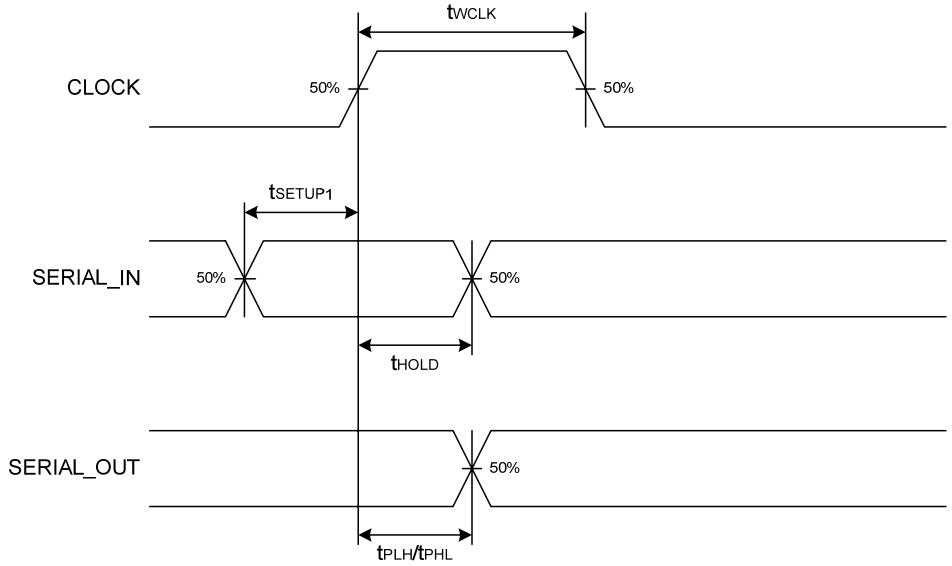
When LATCH terminal is a high voltage, latch circuit does not hold data, and it passes from the input to the output.

When $\overline{\text{ENABLE}}$ terminal is a low voltage, output terminals respond to the data, and on and off does.

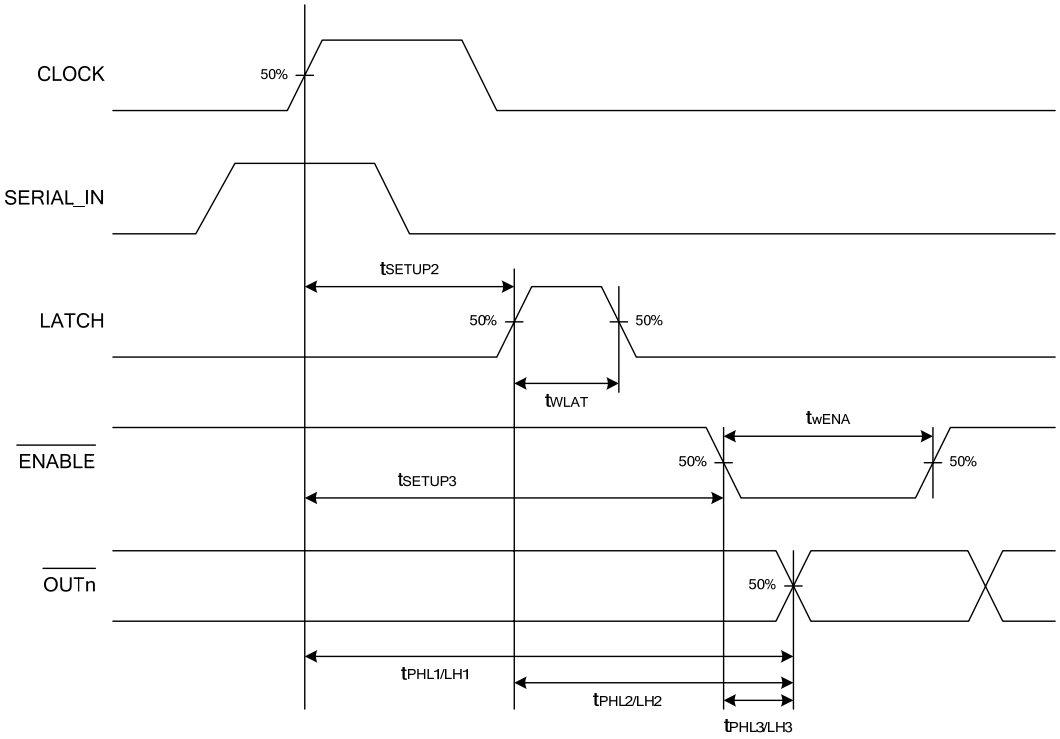
When $\overline{\text{ENABLE}}$ terminal is a high voltage, it closes with the output terminal regardless of the data.

TIMING WAVEFORM

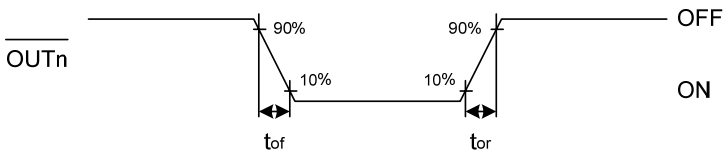
1. Clock, serial-in, serial-out



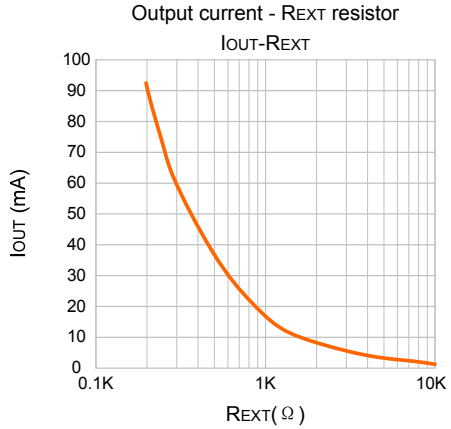
2. Clock, serial-in, LATCH, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$



3. $\overline{\text{OUTn}}$



ELECTRICAL CHARACTERISTICS CURVE



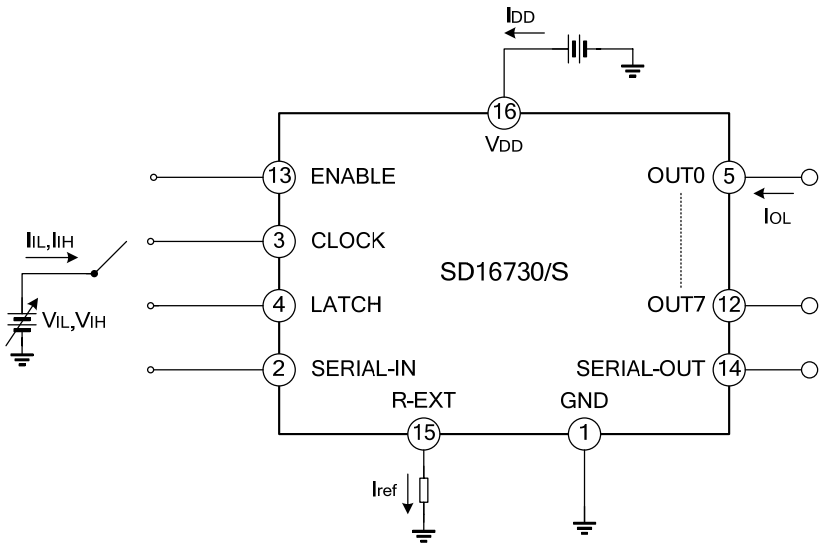
The calculation formula is as follows:

$I_{OUT} = (V_{R\text{-}EXT} / R_{EXT}) \times 16$; $V_{R\text{-}EXT} = 1.185V$

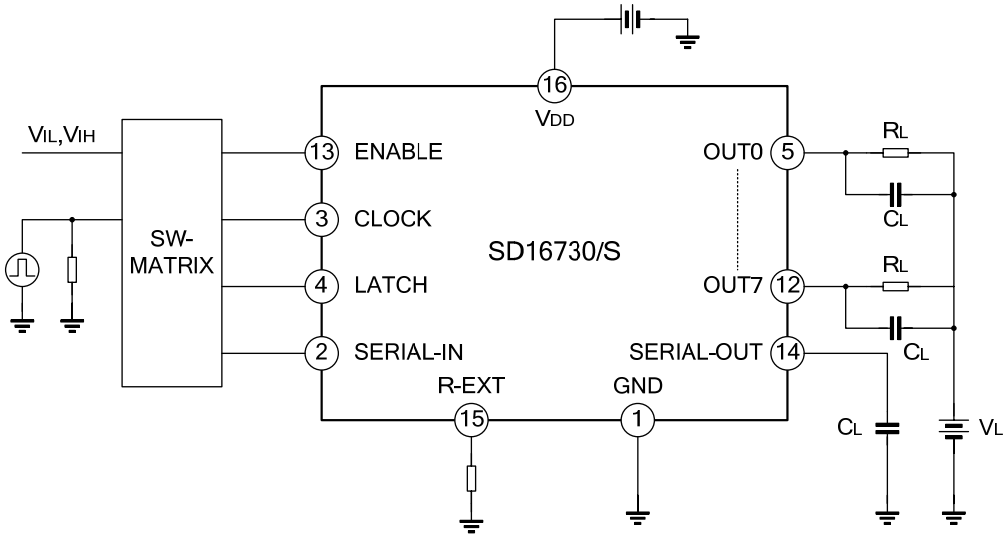
Where, $V_{R\text{-}EXT}$ is voltage on R-EXT port, REXT is the external resistance of R-EXT Port.

TEST CIRCUIT

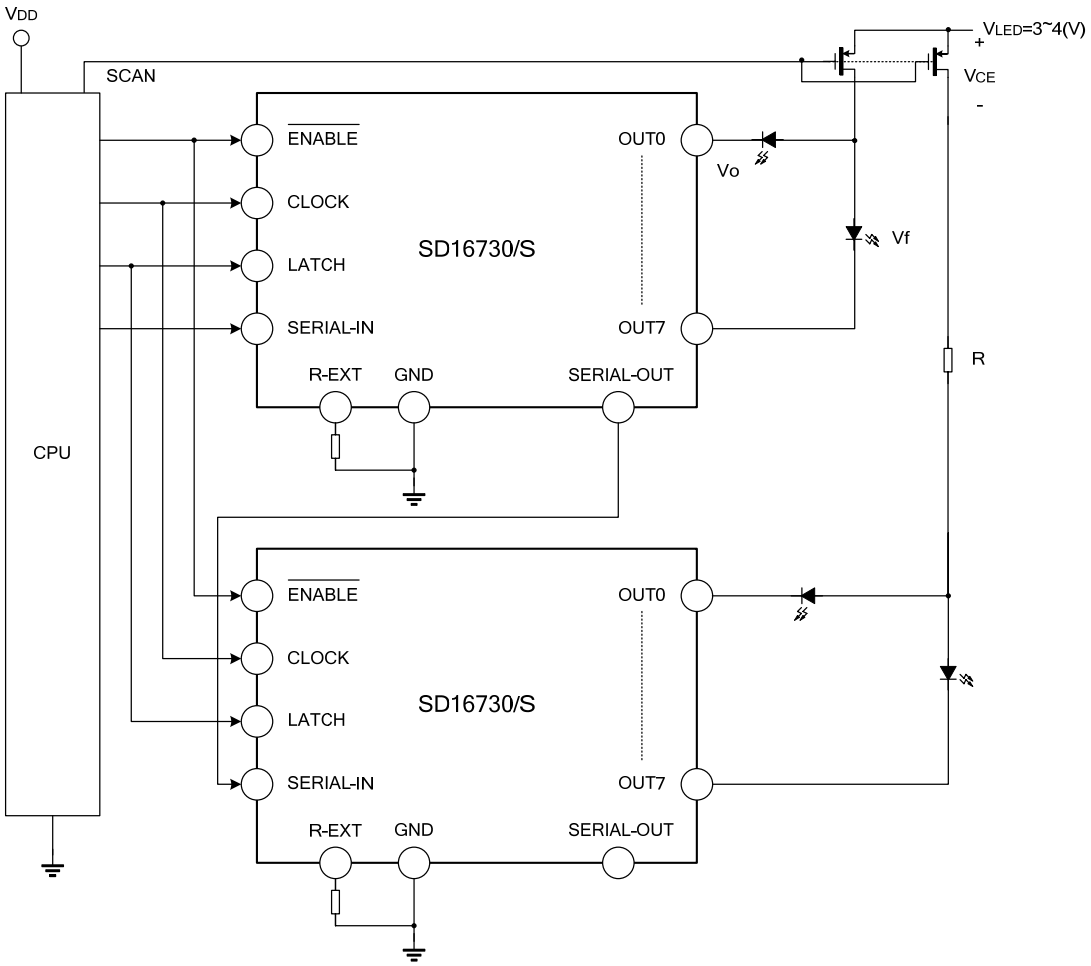
DC CHARACTERISTIC



AC CHARACTERISTIC



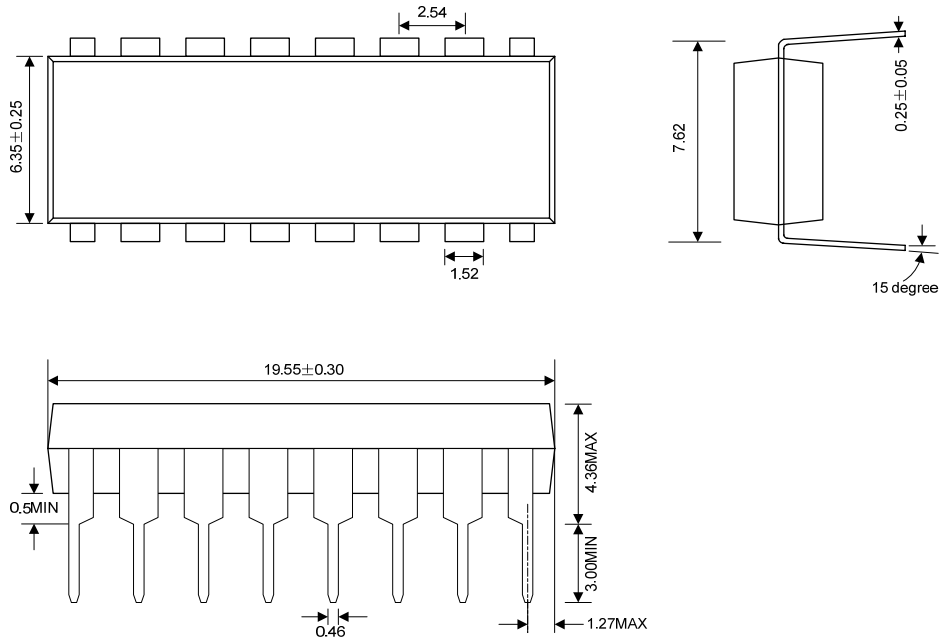
TYPICAL APPLICATION CIRCUIT



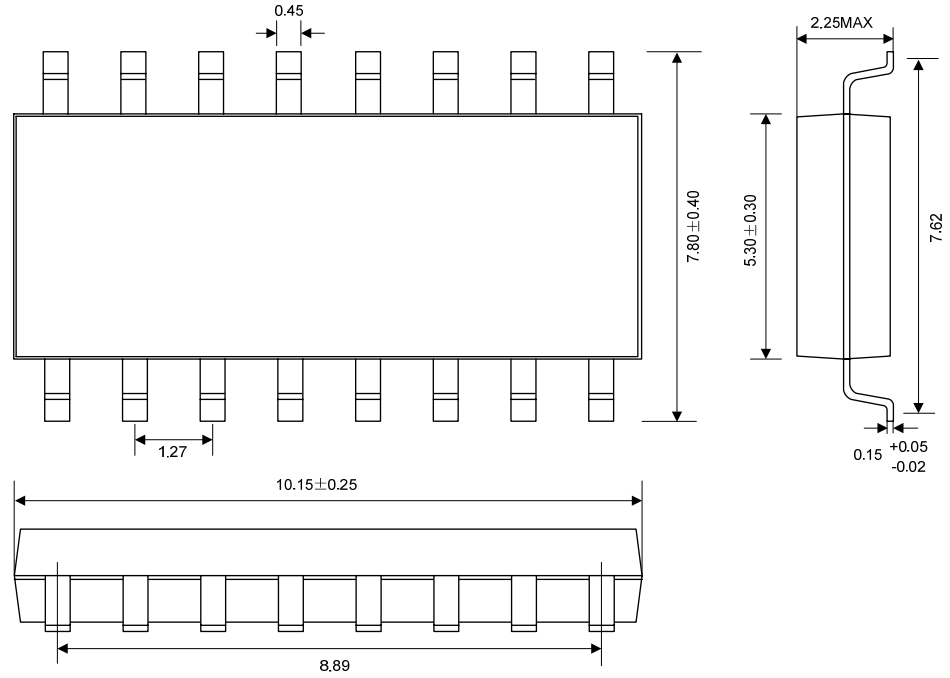
Note: The circuit and parameters are reference only, please set the parameters of the real application circuit based on the real test.

PACKAGE OUTLINE

DIP-16-300-2.54 UNIT: mm



SOP-16-300-1.27 UNIT: mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Note：Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers.

Attachment

Revision History

Data	REV	Description	Page
2008.06.23	1.0	Original	
2008.11.16	1.1	Modify the “RECOMMENDED OPERATE CONDITION” and ”ELECTRICAL CHARACTERISTICS”	