

OKI Semiconductor

MSC23132D/DL-xxBS8/DS8

1,048,576-word x 32-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The MSC23132D/DL-xxBS8/DS8 is a fully decoded, 1,048,576-word x 32-bit CMOS dynamic random access memory module composed of eight 4Mb DRAMs in SOJ packages mounted with eight decoupling capacitors on a 72-pin glass epoxy single-inline package. This module supports any application where high density and large capacity of storage memory are required. The MSC23132DL (the low-power version) is specially designed for lower-power applications.

FEATURES

- 1,048,576-word x 32-bit organization
- 72-pin socket insertable module
 - MSC23132D/DL-xxBS8 : Gold tab
 - MSC23132D/DL-xxDS8 : Solder tab
- Single +5V supply \pm 10% tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 1024cycles/16ms (1024cycles/128ms: L-version)
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Fast page mode capability
- Multi-bit test mode capability

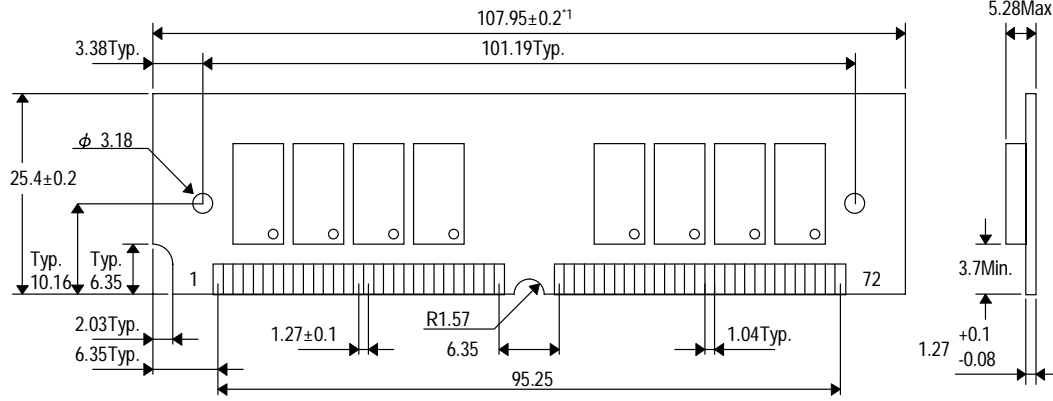
PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}		Operating(Max.)	Standby(Max.)
MSC23132D/DL-60BS8/DS8	60ns	30ns	15ns	110ns	3960mW	44mW/
MSC23132D/DL-70BS8/DS8	70ns	35ns	20ns	130ns	3520mW	8.8mW(L-version)

MODULE OUTLINE

MSC23132D/DL-xxBS8/DS8

(Unit : mm)



*1 The common size difference of the board width 12.5mm of its height is specified as ±0.2.
The value above 12.5mm is specified as ±0.5.

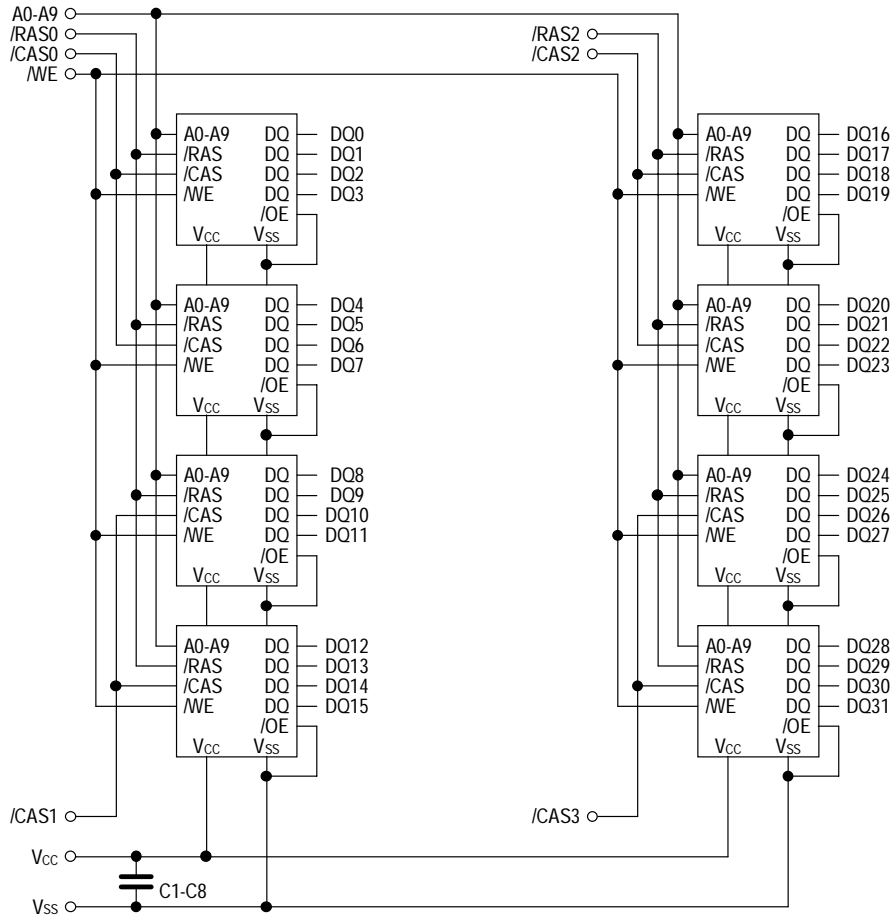
PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	/CAS0	58	DQ28
5	DQ17	23	DQ21	41	/CAS2	59	V _{CC}
6	DQ2	24	DQ6	42	/CAS3	60	DQ29
7	DQ18	25	DQ22	43	/CAS1	61	DQ13
8	DQ3	26	DQ7	44	/RAS0	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	/WE	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	/RAS2	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

Presence Detect Pins

Pin No.	Pin Name	MSC23132D/DL -60BS8/DS8	MSC23132D/DL -70BS8/DS8
67	PD1	V _{SS}	V _{SS}
68	PD2	V _{SS}	V _{SS}
69	PD3	NC	V _{SS}
70	PD4	NC	NC

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Ta = 25°C)

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1.0 to +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D	8	W
Operating Temperature	T _{OPR}	0 to +70	°C
Storage Temperature	T _{STG}	-40 to +125	°C

Recommended Operating Conditions

(Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	6.5	V
Input Low Voltage	V _{IL}	-1.0	-	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C _{IN1}	-	57	pF
Input Capacitance (/WE)	C _{IN2}	-	65	pF
Input Capacitance (/RAS0, /RAS2)	C _{IN3}	-	35	pF
Input Capacitance (/CAS0- /CAS3)	C _{IN4}	-	20	pF
I/O Capacitance (DQ0 - DQ31)	C _{DQ}	-	13	pF

Note: Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0°C to +70°C)

Parameter	Symbol	Condition	MSC23132D/DL -60BS8/DS8		MSC23132D/DL -70BS8/DS8		Unit	Note	
			Min.	Max.	Min.	Max.			
Input Leakage Current	I _{LI}	0V ≤ V _{IN} ≤ 6.5V: All other pins not under test = 0V	-80	80	-80	80	μA		
Output Leakage Current	I _{LO}	Data out is disable 0V ≤ V _{OUT} ≤ 5.5V	-10	10	-10	10	μA		
Output High Voltage	V _{OH}	I _{OH} = -5.0mA	2.4	V _{CC}	2.4	V _{CC}	V		
Output Low Voltage	V _{OL}	I _{OL} = 4.2mA	0	0.4	0	0.4	V		
Average Power Supply Current (Operating)	I _{CC1}	/RAS cycling, /CAS cycling, t _{RC} = min.	-	720	-	640	mA	1, 2	
Power supply current (Standby)	I _{CC2}	/RAS = V _{IH} /CAS = V _{IH}	TTL	-	16	-	16	mA	1
			MOS	-	8	-	8	mA	1
				-	1.6	-	1.6	mA	1, 5
Average Power Supply Current (/RAS only refresh)	I _{CC3}	/RAS cycling, /CAS = V _{IH} , t _{RC} = min.	-	720	-	640	mA	1, 2	
Average Power Supply Current (/CAS before /RAS refresh)	I _{CC6}	t _{RC} = min.	-	720	-	640	mA	1, 2	
Average Power Supply Current (Fast Page Mode)	I _{CC7}	/RAS = V _{IL} , /CAS cycling, t _{PC} = min.	-	560	-	480	mA	1, 3	
Average Power Supply Current (Battery Backup)	I _{CC10}	t _{RC} = 125μs, /CAS before /RAS cycling	-	2.4	-	2.4	mA	1, 4, 5	

- Notes:
1. I_{CC} is dependent on output loading and cycles rates. Specified values are obtained with the output open.
 2. Address can be changed once or less while /RAS = V_{IL}.
 3. Address can be changed once or less while /CAS = V_{IH}.
 4. V_{CC} - 0.2V ≤ V_{IH} ≤ 6.5V, - 1.0V ≤ V_{IL} ≤ 0.2V.
 5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C) Note: 1, 2, 3, 9, 10

Parameter	Symbol	MSC23132D/DL -60BS8/DS8		MSC23132D/DL -70BS8/DS8		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	-	130	-	ns	
Fast Page Mode Cycle Time	t _{PC}	40	-	45	-	ns	
Access Time from /RAS	t _{RAC}	-	60	-	70	ns	4, 5, 6
Access Time from /CAS	t _{CAC}	-	15	-	20	ns	4, 5
Access Time from Column Address	t _{AA}	-	30	-	35	ns	4, 6
Access Time from /CAS Precharge	t _{CPA}	-	35	-	40	ns	4
Output Low Impedance Time from /CAS	t _{CLZ}	0	-	0	-	ns	4
/CAS to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	ns	7
Transition Time	t _T	3	50	3	50	ns	3
Refresh Period	t _{REF}	-	16	-	16	ms	
Refresh Period (L-version)	t _{REF}	-	128	-	128	ms	
/RAS Precharge Time	t _{RP}	40	-	50	-	ns	
/RAS Pulse Width	t _{RAS}	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	100K	70	100K	ns	
/RAS Hold Time	t _{RSH}	15	-	20	-	ns	
/CAS Precharge Time (Fast Page Mode)	t _{CP}	10	-	10	-	ns	
/CAS Pulse Width	t _{CAS}	15	10K	20	10K	ns	
/CAS Hold Time	t _{CSH}	60	-	70	-	ns	
/CAS to /RAS Precharge Time	t _{CRP}	5	-	5	-	ns	
/RAS Hold Time from /CAS Precharge	t _{RHCP}	35	-	40	-	ns	
/RAS to /CAS Delay Time	t _{RCD}	20	45	20	50	ns	5
/RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	ns	6
Row Address Set-up Time	t _{ASR}	0	-	0	-	ns	
Row Address Hold Time	t _{RAH}	10	-	10	-	ns	
Column Address Set-up Time	t _{ASC}	0	-	0	-	ns	
Column Address Hold Time	t _{CAH}	15	-	15	-	ns	
Column Address Hold Time from /RAS	t _{AR}	50	-	55	-	ns	
Column Address to /RAS Lead Time	t _{RAL}	30	-	35	-	ns	
Read Command Set-up Time	t _{RCS}	0	-	0	-	ns	
Read Command Hold Time	t _{RCH}	0	-	0	-	ns	8
Read Command Hold Time referenced to /RAS	t _{RRH}	0	-	0	-	ns	8

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C) Note: 1, 2, 3, 9, 10

Parameter	Symbol	MSC23132D/DL -60BS8/DS8		MSC23132D/DL -70BS8/DS8		Unit	Note
		Min.	Max.	Min.	Max.		
Write Command Set-up Time	t _{WCS}	0	-	0	-	ns	
Write Command Hold Time	t _{WCH}	10	-	10	-	ns	
Write Command Hold Time from /RAS	t _{WCR}	45	-	50	-	ns	
Write Command Pulse Width	t _{WP}	10	-	10	-	ns	
Write Command to /RAS Lead Time	t _{RWL}	15	-	20	-	ns	
Write Command to /CAS Lead Time	t _{CWL}	15	-	20	-	ns	
Data-in Set-up Time	t _{DS}	0	-	0	-	ns	
Data-in Hold Time	t _{DH}	15	-	15	-	ns	
Data-in Hold Time from /RAS	t _{DHR}	50	-	55	-	ns	
/CAS Active Delay Time from /RAS Precharge	t _{RPC}	10	-	10	-	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	t _{CSR}	5	-	5	-	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	t _{CHR}	10	-	10	-	ns	
/WE to /RAS Precharge Time (/CAS before /RAS)	t _{WRP}	10	-	10	-	ns	
/WE Hold Time from /RAS (/CAS before /RAS)	t _{WRH}	10	-	10	-	ns	
/RAS to /WE Set-up Time (Test Mode)	t _{WTS}	10	-	10	-	ns	
/RAS to /WE Hold Time (Test Mode)	t _{WTH}	10	-	10	-	ns	

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
 2. The AC characteristics assumes $t_T = 5$ ns.
 3. $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ are reference levels for measuring input timing signals. Transition time (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2TTL loads and 100pF.
 5. Operation within the $t_{RCD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RCD}(\text{Max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{Max.})$ limit, then the access time is controlled by t_{CAC} .
 6. Operation within the $t_{RAD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RAD}(\text{Max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{Max.})$ limit, then the access time is controlled by t_{AA} .
 7. $t_{OFF}(\text{Max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by a /RAS only refresh or /CAS before /RAS refresh cycle.
 10. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.