OKI semiconductor

MSC23109D-xxBS/DS3

1,048,576 Word By 9 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC23109D-xxBS/DS3 is a fully decoded, 1,048,576 word X 9 bit CMOS dynamic random access memory composed of two 4-Mb DRAMs (1Mx4) in SOJ and one 1Mb DRAM (1Mx1) in SOJ. The mounting of three SOJs together with three decoupling capacitors on a 30-pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required.

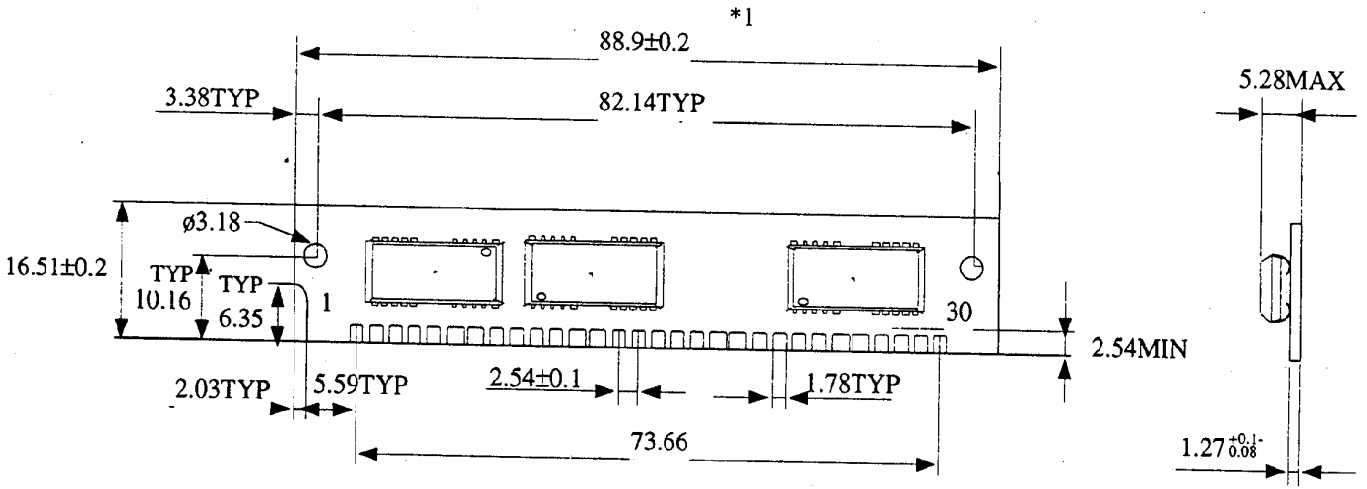
FEATURES

- 1,048,576 word X 9 bit organization
- 30-pin socket insertable module
  MSC23109D-xxBS3 : Gold tab
  MSC23109D-xxDS3 : Solder tab
- Single +5 V supply ±10 % tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 1024 cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$ only refresh capability

FAMILY ORGANIZATION

FAMILY	ACCESS TIME (Max)			Cycle Time	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	(Min)	Operating (Max)	Standby (Max)
MSC23109D-60BS/DS3	60ns	30ns	15ns	120ns	1375mW	16.5mW
MSC23109D-70BS/DS3	70ns	35ns	20ns	130ns	1210mW	

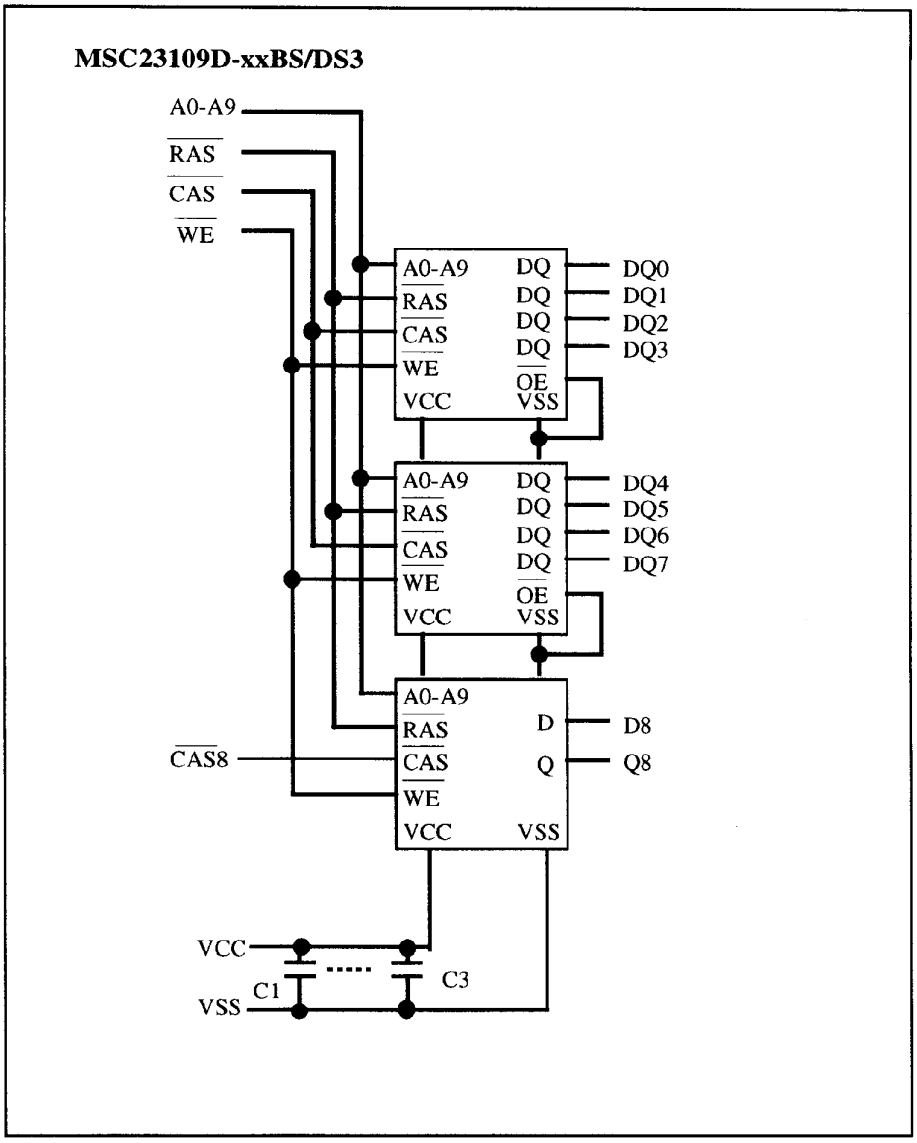
MSC23109D-xxBS/DS3



*1 The common size difference of the board width 12.5mm of its height is specified as ±0.2. The value above 12.5mm is specified as ±0.5.

FUNCTIONAL BLOCK DIAGRAM

MSC23109D-xxBS/DS3



PIN CONFIGURATION

MSC23109D-xxBS/DS3

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	Vss
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS8}$
9	Vss	19	NC	29	D8
10	DQ2	20	DQ5	30	Vcc

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 1.0 ~ + 7.0	V
Voltage Vcc supply relative to Vss	V_{CC}	- 1.0 ~ + 7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	3	W
Operating temperature	T_{OPR}	- 0 ~ + 70	℃
Storage temperature	T_{STG}	- 40 ~ + 125	℃

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted within the limits as specified in this data sheet. Exposure to absolute maximum rating conditions for extended period may affect device reliabity.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYPE	MAX	UNIT	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0 ℃ ~ + 70 ℃
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	-	6.5	V	
Input low voltage	V_{IL}	-1.0	-	0.8	V	

CAPACITANCE

Parameter	Symbol	Typ.	MAX	Unit
Input Capacitance(A0-A9)	C_{IN1}		25	pF
Input Capacitance($\overline{RAS}$,$\overline{WE}$)	C_{IN2}		28	pF
Input Capacitance($\overline{CAS}$)	C_{IN3}		20	pF
I/O Capacitance(DQ0-DQ7)	C_{DO}		13	pF
Input Capacitance($\overline{CAS8}$)	C_{IN4}		13	pF
Input Capacitance(D8)	C_{IN5}		12	pF
Output Capacitance(Q8)	C_{OUT}		13	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS
(Vcc = 5V± 10%, Ta = 0 ~ +70 °C)

Parameter	Symbol	Condition	MSC23109D-60BS/DS3		MSC23109D-70BS/DS3		Unit	Note
			Min	Max	Min	Max		
Input Leakage Current	I_{LI}	$0V \le V_{in} \le 6.5V$: All other pins not under test = 0V	-30	30	-30	30	µA	
Output Leakage Current	I_{LO}	DQ is disable $0V \le V_{out} \le 5.5V$	-10	10	-10	10	µA	
Output High Voltage	V_{OH}	I_{OH} = -5.0mA	2.4	Vcc	2.4	Vcc	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$ cycling t_{RC}=min	-	250	-	220	mA	1,2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	-	6	-	6	mA	1
		$\overline{RAS}$,$\overline{CAS}$ ≥ V_{CC}-0.2V	-	3	-	3	mA	1
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ =V_{IL} t_{RC}=min	-	250	-	220	mA	1,2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	-	250	-	220	mA	1,2
Average power supply current (Fast page)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	-	205	-	175	mA	1,3

NOTE: 1. Icc is dependent on output loading and cycles rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC CHARACTERISTIC

(Vcc = 5V±10%, Ta = 0 ~70 °C)

NOTE 1,2,3

Parameter	Symbol	MSC23109D-60BS/DS3		MSC23109D-70BS/DS3		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	120	-	130	-	ns	
Fast page mode cycle time	t_{PC}	40	-	45	-	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	-	15	-	20	ns	4,5
Access time from column address	t_{AA}	-	30	-	35	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	ns	4
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0	-	0	-	ns	4
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns	7
Transition time	t_T	3	50	3	50	ns	3
Refresh period	t_{REF}	-	16	-	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	50	-	50	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	-	20	-	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	-	10	-	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	-	70	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	6
Row address set-up time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	50	-	55	-	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	ns	

AC CHARACTERISTICS (Continued)
(Vcc = 5V±10%, Ta = 0 ~70 °C)

Parameter	Symbol	MSC23109D-60BS/DS3		MSC23109D-70BS/DS3		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	-	0	-	ns	8
Write command set-up time	t_{WCS}	0	-	0	-	ns	
Write command hold time	t_{WCH}	10	-	15	-	ns	
WRite command hold time from $\overline{RAS}$	t_{WCR}	50	-	55	-	ns	
Write command pulse width	t_{WP}	10	-	15	-	ns	
WRite command to $\overline{RAS}$ lead time	t_{RWL}	15	-	20	-	ns	
WRite command to $\overline{CAS}$ lead time	t_{CWL}	15	-	20	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	ns	
Data-in hold time	t_{DH}	15	-	15	-	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	50	-	55	-	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	-	10	-	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	-	30	-	ns	

NOTES:
1) An initial pause of 200 µs is required after power-up followed by aminimum of 8 initializatin cycles (examples: $\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
2) The AC measurements assume the transition time (t_T) = 5 ns.
3) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.
4) Measured by using an eqivalent load circuit of 2 TTL loads and 100 pF.
5) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD}(max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
6) Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD}(max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
7) The t_{OFF} (max.) spec. defines at which time the output data achieves a high impedance state and is not referenced to output voltage levels.
8) Either the t_{RRH} or the t_{RCH} spec. must be satisfied for proper read cycle.