# PRELIMINARY

Notice: These are not a final specification. Some parametric limits are subject to change.

# M50933-XXXFP
# M50934-XXXFP

## SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## DESCRIPTION

The M50933-XXXFP and the M50934-XXXFP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 80-pin plastic molded QFP. These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

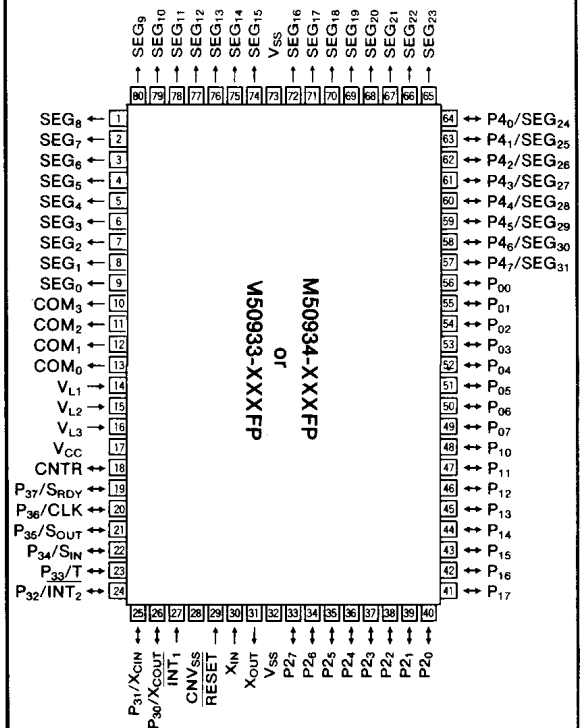
These microcomputers are also suitable for applications which require controlling LCDs.

The differences between M50933-XXXFP and the M50934-XXXFP are noted below.

| Type name | ROM size | RAM size |
|---|---|---|
| M50933-XXXFP | 6144 bytes | 192 bytes |
| M50934-XXXFP | 8192 bytes | 256 bytes |

The differences between the M50933-XXXFP, M50934-XXXFP and the M50932-XXXFP are some electrical characteristics and the fact that these microcomputers work only in the single-chip mode. Other functions are explained in the M50932-XXXFP's section in detail.

## PIN CONFIGURATION (TOP VIEW)




Outline 80P6

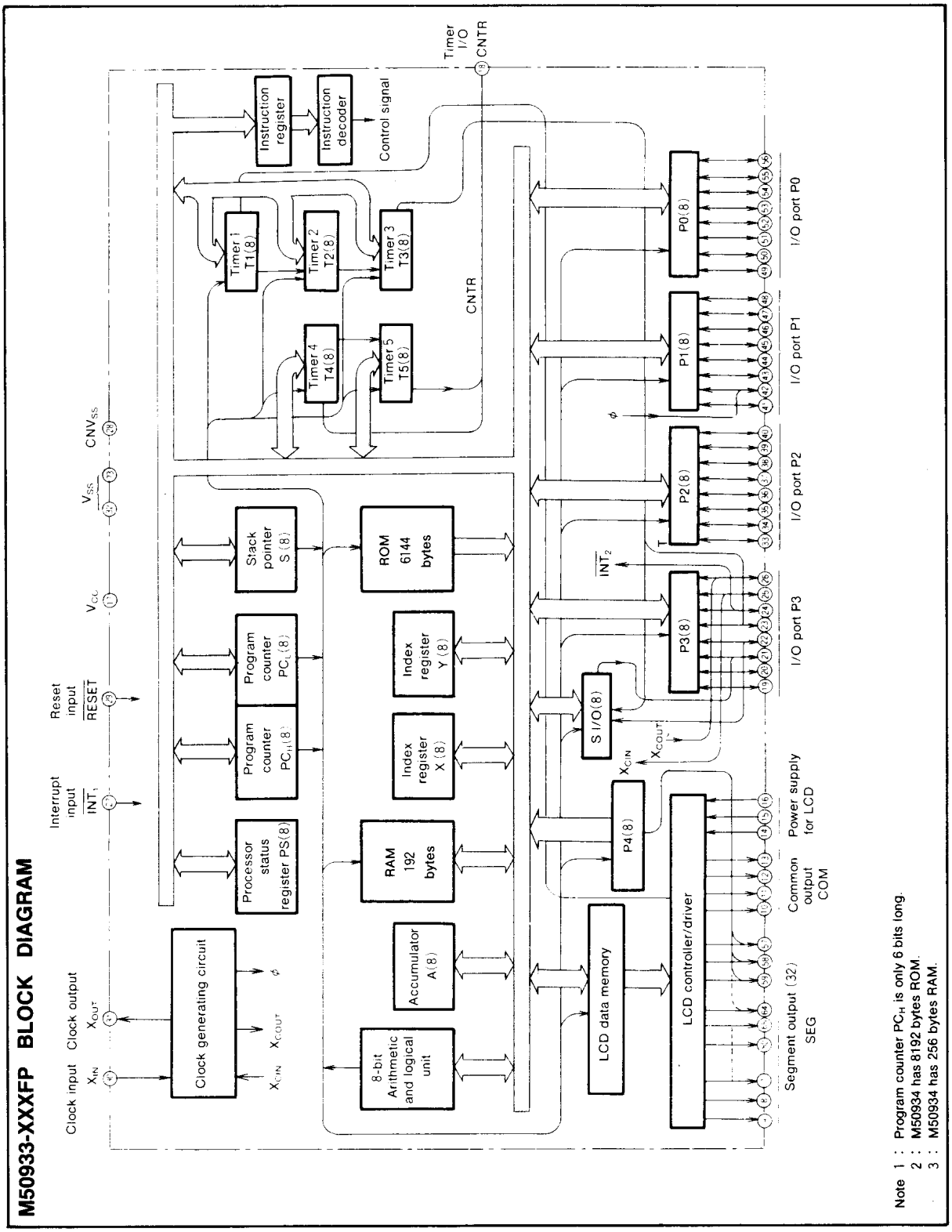
## FEATURES

- Number of basic instructions ..... 69
- Instruction execution time
  ..... 2$\mu$s (minimum instructions at 4MHz frequency)
- Single power supply
  f($X_{IN}$)=4MHz ..... 3.8~5.5V
  f($X_{IN}$)=2MHz ..... 2.7V $\leqq V_{CC} \leqq$ 5.5V(Typ.)
- Power dissipation
  normal operation mode (at 4MHz frequency)
  ..... 15mW($V_{CC}$=5V, Typ.)
  low-speed operation mode (at 32kHz frequency for clock function) ..... 225$\mu$W ($V_{CC}$=5V, Typ.)
  stop mode(at 25℃) ..... 5$\mu$W ($V_{CC}$=5V, Max.)
- RAM retention voltage (stop mode)
  ..... 2.0V $\leqq V_{RAM} \leqq$ 5.5V
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- 16-bit timer ..... 1 (Two 8-bit timers make one set)
- Programmable I/O ports
  (Ports P0, P1, P2, P3) ..... 32
- Input port (Port P4) ..... 8
- Serial I/O (8-bit) ..... 1
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
  segment output ..... 32
  common output ..... 4
- Two clock generator circuits
  (One is for main clock, the other is for clock function)

## APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment
Telephone

## M50933-XXXFP BLOCK DIAGRAM




Note 1 : Program counter $PC_H$ is only 6 bits long.
2 : M50934 has 8192 bytes ROM.
3 : M50934 has 256 bytes RAM.

## FUNCTIONS OF M50933-XXXFP

| Parameter | | | Functions |
|---|---|---|---|
| Number of basic instructions | | | 69 |
| Instruction execution time | | | 2$\mu$s (minimum instructions, at 4MHz frequency). |
| Clock frequency | | | 4.3MHz |
| Memory size | ROM | | 6144 bytes (8192 bytes for M50934-XXXFP) |
| | RAM | | 192 bytes (256 bytes for M50934-XXXFP) |
| | RAM for display LCD | | 16 bytes |
| Input/Output ports | P0, P1, P2, P3 | I/O | 8-bit×4 |
| | P4 | Input | 8-bit×1 (Port P4 are in common with SEG) |
| | SEG | LCD output | 32-bit×1 |
| | COM | LCD output | 4-bit×1 |
| Serial I/O | | | 8-bit×1 |
| Timers | | | 8-bit timer×3 (2 when serial I/O is used) |
| | | | 16-bit timer×1 (combination of two 8-bit timers) |
| LCD controller/driver | Bias | | 1/2, 1/3 bias selectable |
| | Duty ratio | | 1/2, 1/3, 1/4 duty selectable |
| | Common output | | 4 |
| | Segment output | | 32 ($SEG_{24}$~$SEG_{31}$ are in common with port P4) |
| Subroutine nesting | | | 64 (max.) |
| Interrupt | | | Two external interrupts, Three timer interrupts (or two timer, one serial I/O) |
| Clock generating circuit | | | Two built-in circuits (ceramic or quartz crystal oscillator ) |
| Supply voltage | | | 2.7~5.5V (RAM retention voltage at clock stop is 2~5.5V) |
| Power dissipation | At high-speed operation $V_{CC}$=5V | | 15mW (at clock frequency $X_{IN}$=4MHz, typ.) |
| | At low-speed operation $V_{CC}$=5V | | 225$\mu$W (at clock frequency $X_{CIN}$=32kHz, typ.) |
| | At STOP mode | | 5$\mu$W (at clock stop, max.) |
| Input/Output characteristics | Input/Output voltage | | 5V |
| | Output current | | $I_{OH}$=−2mA ($V_{OH}$=3V) |
| | | | $I_{OL}$=10mA ($V_{OL}$=2V) |
| | | | Pull-up current : Min. −30$\mu$A, max. −140$\mu$A, typ −70$\mu$A ($V_{CC}$=5V input voltage 0V) |
| Operating temperature range | | | −10~70℃ |
| Device structure | | | CMOS silicon gate |
| Package | | | 80-pin plastic molded QFP |

## PIN DESCRIPTION

| Pin | Name | Input/ Output | Functions |
|---|---|---|---|
| $V_{CC}$, $V_{SS}$ | Supply voltage | | Power supply inputs 5V±10% to $V_{CC}$, and 0V to $V_{SS}$. |
| $CNV_{SS}$ | $CNV_{SS}$ | | This is usually connect to $V_{SS}$. |
| $\overline{RESET}$ | Reset input | Input | To enter the reset state, the reset input pin must be kept at a "L" for more than 2$\mu$s (under normal $V_{CC}$ conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time. |
| $X_{IN}$ | Clock input | Input | These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the $X_{IN}$ and $X_{OUT}$ pins. If an external clock is used, the clock source should be connected the $X_{IN}$ pin and the $X_{OUT}$ pin should be left open. |
| $X_{OUT}$ | Clock output | Output | |
| $\overline{INT_1}$ | Interrupt input | Input | This is the highest order interrupt input pin. |
| $P0_0$~$P0_7$ | I/O port P0 | I/O | Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output. |
| $P1_0$~$P1_7$ | I/O port P1 | I/O | Port P1 is an 8-bit I/O port and has basically the same functions as port P0. |
| $P2_0$~$P2_7$ | I/O port P2 | I/O | Port P2 is an 8-bit I/O port and has basically the same functions as port P0. |
| $P3_0$~$P3_7$ | I/O port P3 | I/O | Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, $S_{OUT}$, and $S_{IN}$ pins, respectively. Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT_2}$ pin, $X_{CIN}$ and $X_{COUT}$ pins, respectively. |
| $P4_0$~$P4_7$ | Input port P4 | I/O | Port P4 is an 8-bit input port and can be used as segment output pins. |
| $V_{L1}$~$V_{L3}$ | Voltage input for LCD | Input | These are voltage input pins for LCD. Supply voltage as $0V \leqq V_{L1} \leqq V_{L2} \leqq V_{L3} \leqq V_{CC}$. $0V$~$V_{L3}$ is supplied to LCD. |
| $COM_0$~ $COM_3$ | Common output | Output | These are LCD common output pins. At 1/2 duty, $COM_2$ and $COM_3$ pins are not used. At 1/3 duty, $COM_3$ is not used. |
| $SEG_0$~ $SEG_{23}$ | Segment output | Output | These are LCD segment output pins. |
| CNTR | Timer I/O | I/O | This is an output pin for the timer 4 and 5. |

## BASIC FUNCTION BLOCKS

### MEMORY

A memory map for the M50933-XXXFP is shown in Figure 1. Address $2800_{16}$ to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 4096 bytes (Addresses $2000_{16}$ to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 8192 bytes for M50934-XXXFP). Addresses $3F00_{16}$ to $3FFF_{16}$ are a special address area (special page). By using the special page addressing mode of JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $3FF4_{16}$ to $3FFF_{16}$ are vector addresses used for the reset and interrupts (See interrupts chapter).

Addresses $0000_{16}$ to $00FF_{16}$ are the zero page address area. By using zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses $0000_{16}$ to $007F_{16}$ and $0100_{16}$ to $013F_{16}$ are assigned for the built-in RAM which consists of 192 bytes (Addresses $0000_{16}$ to $007F_{16}$ and $0100_{16}$ to $017F_{16}$ are assigned for the built-in RAM which consists of 256 bytes for M50934-XXXFP). This RAM except the area in the page 1 is used as the stack during subroutine calls and interrupts, in addition to data storage.

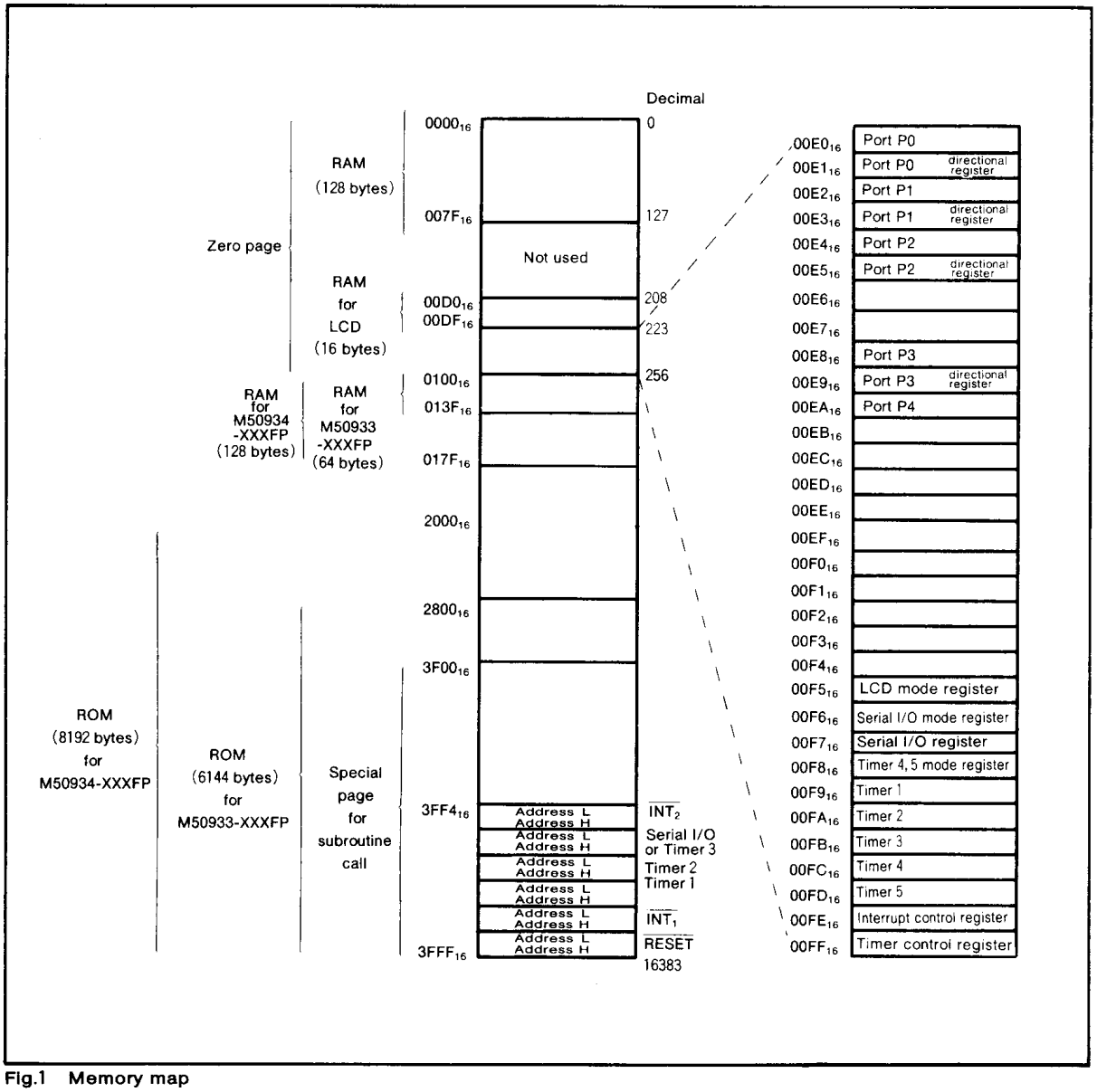



Fig.1 Memory map

## PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of the these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address $00F8_{16}$) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC,CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) When LCD turn-on bit (bit 3 of address $00F5_{16}$) of the LCD mode register is "1", don't stop the timers or count source for timers.

(7) The serial I/O counter must be initialized (write to $00F7_{16}$) after switching the transfer clock source.

(8) When using an external clock as the transfer clock source, the serial I/O counter must be initialized while the external clock is at "H" level.

(9) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.

(10) When using pins $P3_0$ and $P3_1$ as clock I/O pins, the pull-up option must not be used.

(11) Notes on controlling the clock generation circuit

① When system clock is changed $X_{IN}/4$ to $X_{CIN}/2$, set $LM_7$ to "1" after oscillation is stable by the software in side of clock $X_C$.

② When system clock is changed $X_{CIN}/2$ to $X_{IN}/4$, set $LM_7$ to "0" after oscillation is stable by the software in side of clock X.

③ When $SM_5$ is "0" or when $LM_7$ is "0" and $SM_6$ is "0", $LM_6$ is automatically set to "0" by the hardware.

④ When system clock selection bit (bit 7 of address $00F5_{16}$) of the LCD mode register is "1", don't set $SM_5$ to "0".

⑤ In single-chip mode, the $X_{OUT}$ pin uses as $X_{OUT}$ output except setting value of $LM_5$.

⑥ The other than single-chip mode and the input voltage for $\overline{RESET}$ pin is 10V, $X_{OUT}$ pin uses as SYNC output except setting value of $LM_5$.

(12) Bit 1 and 0 of the timer control register must be set to [00] because M50933 and M50934 work only in single-chip mode. Also, bit 5 of the LCD mode register must not to be set to "1".

## DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation from

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port $P3_5/S_{OUT}$ output format
- CNTR pin pull-up transistor

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Output transistor are "off" | −0.3∼7 | V |
| $V_I$ | Supply voltage for LCD $V_{L1}$∼$V_{L3}$ | | −0.3∼$V_{CC}$+0.3 | V |
| $V_I$ | Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $X_{IN}$ | | −0.3∼$V_{CC}$+0.3 | V |
| $V_I$ | Input voltage $\overline{INT_1}$, $CNV_{SS}$ | | −0.3∼7 | V |
| $V_I$ | Input voltage $\overline{RESET}$, CNTR | | −0.3∼13 | V |
| $V_O$ | Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $COM_0$∼$COM_3$, $SEG_0$∼$SEG_{31}$, $X_{OUT}$ | | −0.3∼$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage CNTR | | −0.3∼7 | V |
| $P_d$ | Power dissipation | $T_a$ = 25℃ | 300 | mW |
| $T_{opr}$ | Operating temperature | | −10∼70 | ℃ |
| $T_{stg}$ | Strage temperature | | −40∼125 | ℃ |

## RECOMMENDED OPERATING CONDITIONS ($V_{CC}$=2.7∼5.5V, $V_{SS}$=0V, $T_a$=−10∼70℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage (Note 1) | f($X_{IN}$)=4.3MHz | 3.8 | | 5.5 | V |
| | | f($X_{IN}$)=2MHz | 2.7 | | 5.5 | |
| $V_{SS}$ | Supply voltage | | | 0 | | V |
| $V_{IH}$ | "H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note3), $P4_0$∼$P4_7$, $\overline{RESET}$, $X_{IN}$, $CNV_{SS}$ | | 0.7$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4) $\overline{INT_1}$, CNTR | | 0.74$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note 3), $P4_0$∼$P4_7$, $CNV_{SS}$ | | 0 | | 0.3$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4) $\overline{INT_1}$, CNTR | | 0 | | 0.26$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $\overline{RESET}$ | | 0 | | 0.12$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $X_{IN}$ | | 0 | | 0.16$V_{CC}$ | V |
| $I_{OH}$ | "H" output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ (Note 5), $X_{OUT}$ | | | | −2 | mA |
| $I_{OL(peak)}$ | "L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, $X_{OUT}$ (Note 6) | | | | 10 | mA |
| $I_{OL(avg)}$ | "L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, $X_{OUT}$ (Note 7) | | | | 5 | mA |
| f($X_{IN}$) | Clock oscillating frequency (Note 8) | $V_{CC}$=3.8∼5.5V | 64 | | 4300 | kHz |
| | | $V_{CC}$=2.7∼5.5V | 64 | | 2000 | |
| f($X_{CIN}$) | Clock oscillating frequency for clock function (Note 8) | | 32 | | 50 | kHz |

Note 1 : When only maintaining the RAM data, minimum value of $V_{CC}$ is 2V.
2 : When using port $P3_1$ as $X_{CIN}$, $0.85V_{CC} \leqq V_{IH} \leqq V_{CC}$, $0 \leqq V_{IL} \leqq 0.15V_{CC}$ for port $P3_1$.
3 : In this case of using port $P3_6$ as normal input.
4 : In this case of using port $P3_6$ as CLK input.
Especially when the input oscillation frequency is more than 50kHz, recommend the following :
$0.8V_{CC} \leqq V_{IH} \leqq V_{CC}$, $0 \leqq V_{IL} \leqq 0.2V_{CC}$
5 : The total of $I_{OH}$ of port P0, P1, P2, P3 and $X_{OUT}$ should be 35mA max.
6 : The total of $I_{OL}$ (peak) of port P0, P1, P2, P3 should be 55mA max, and the total of $I_{OL}$ (peak) of port P3, CNTR, and $X_{OUT}$ should be 45mA max.
7 : $I_{OL}$ (avg) is the average current in 100ms.
8 : When changing the contents of the most significant bit at address $00F5_{16}$, f($X_{IN}$) needs the following range : f($X_{IN}$) > 3f($X_{CIN}$).

## ELECTRICAL CHARACTERICS ($V_{SS}$= 0 V, $T_a$=−10~70℃, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | "H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$(Note 9)(Note10) | $V_{CC}$=5V, $I_{OH}$=−2mA | | 3 | | | V |
| | | $V_{CC}$=3V, $I_{OH}$=−0.7mA | | 2 | | | |
| $V_{OH}$ | "H" output voltage $X_{OUT}$ | $V_{CC}$=5V, $I_{OH}$=−1.5mA | | 3 | | | V |
| | | $V_{CC}$=3V, $I_{OH}$=−0.3mA | | 2 | | | |
| $V_{OL}$ | "L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$(Note10), CNTR | $V_{CC}$=5V, $I_{OL}$=10mA | | | | 2 | V |
| | | $V_{CC}$=3V, $I_{OL}$=0.3mA | | | | 1 | |
| $V_{OL}$ | "L" output voltage $X_{OUT}$ | $V_{CC}$=5V, $I_{OL}$=1.5mA | | | | 2 | V |
| | | $V_{CC}$=3V, $I_{OL}$=0.3mA | | | | 1 | |
| $V_{T+}-V_{T-}$ | Hysteresis $\overline{INT_1}$, CNTR | $V_{CC}$=5V | | 0.25 | | 1 | V |
| | | $V_{CC}$=3V | | 0.15 | | 0.7 | |
| $V_{T+}-V_{T-}$ | Hysteresis $P3_6$ | When used as CLK input | $V_{CC}$=5V | | 0.5 | | V |
| | | | $V_{CC}$=3V | | 0.4 | | |
| $V_{T+}-V_{T-}$ | Hysteresis $P3_1$ | When used as $X_{CIN}$ input | $V_{CC}$=5V | | 0.7 | | V |
| | | | $V_{CC}$=3V | | 0.5 | | |
| $V_{T+}-V_{T-}$ | Hysteresis $P2_0$~$P2_7$, $P3_2$ | $V_{CC}$=5V | | | 0.5 | | V |
| | | $V_{CC}$=3V | | | 0.4 | | |
| $V_{T+}-V_{T-}$ | Hysteresis $\overline{RESET}$ | $V_{CC}$=5V | | | 0.5 | 0.7 | V |
| | | $V_{CC}$=3V | | | 0.35 | | |
| $V_{T+}-V_{T-}$ | Hysteresis $X_{IN}$ | $V_{CC}$=5V | | | 0.5 | | V |
| | | $V_{CC}$=3V | | | 0.35 | | |
| $I_{IL}$ | "L" input current $P4_0$~$P4_7$ (except reset state) {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR} without pull-up Tr. $\overline{INT_1}$, $\overline{RESET}$, $X_{IN}$ | $V_{CC}$=5V, $V_I$=0V | | | | −5 | μA |
| | | $V_{CC}$=3V, $V_I$=0V | | | | −4 | |
| $I_{IL}$ | "L" input current {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR} with pull-up Tr. | $V_{CC}$=5V, $V_I$=0V | | −30 | −70 | −140 | μA |
| | | $V_{CC}$=3V, $V_I$=0V | | −6 | −25 | −45 | |
| $I_{IL}$ | "L" input current $P4_0$~$P4_7$ (at reset state) | $V_{CC}$=5V, $V_{L3}$=5V, $V_I$=0V | | −30 | | −140 | μA |
| | | $V_{CC}$=3V, $V_{L3}$=3V, $V_I$=0V | | −6 | | −45 | |
| $I_{IH}$ | "H" input current $P4_0$~$P4_7$ (except reset state) $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR, $\overline{INT_1}$, $\overline{RESET}$, $X_{IN}$ | $V_{CC}$=5V, $V_I$=5V | | | | 5 | μA |
| | | $V_{CC}$=3V, $V_I$=3V | | | | 4 | |
| $I_{IH}$ | "H" input current $P4_0$~$P4_7$ (at reset state) | $V_{CC}$=5V, $V_{L3}$=5V, $V_I$=5V | | | | 5 | μA |
| | | $V_{CC}$=3V, $V_{L3}$=3V, $V_I$=3V | | | | 4 | |
| $R_{COM}$ | Output impedance $COM_0$~$COM_3$ | $V_{L1}$=$V_{CC}$/3, $V_{L2}$=2$V_{L1}$, $V_{L3}$=$V_{CC}$, Other COM, SEG pins are opend. | $V_{CC}$=5V | 30 | 200 | 2000 | Ω |
| | | | $V_{CC}$=3V | 70 | 500 | 4000 | |
| $R_S$ | Output impedance $SEG_0$~$SEG_{31}$ | | $V_{CC}$=5V | | 2 | | kΩ |
| | | | $V_{CC}$=3V | | 3 | | |
| $I_{CC}$ | Supply current (at operation) | Output pin are opened. $\overline{RESET}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, and $P3_0$~$P3_7$ are connected to $V_{CC}$. Except the above pins are connected to $V_{SS}$. However, $X_{IN}$ and $X_{CIN}$ are input signal according to the conditions. | f($X_{IN}$)=4MHz, $V_{CC}$=5V | | 3 | 6 | mA |
| | | | f($X_{IN}$)=1MHz, $V_{CC}$=3V | | 0.4 | 0.8 | |
| | | | $T_a$=25℃, $X_{IN}$=0V, f($X_{CIN}$)=32.8kHz at low power mode ($LM_6$=1) $V_{CC}$=5V | | 45 | 85 | μA |
| | | | $T_a$=25℃, $X_{IN}$=0V, f($X_{CIN}$)=32.8kHz at low power mode ($LM_6$=1) $V_{CC}$=3V | | 18 | 26 | |
| $I_{CC}$ | Supply current (at wait state) | | f($X_{IN}$)=4MHz, $V_{CC}$=5V | | 1 | 2 | mA |
| | | | f($X_{IN}$)=1MHz, $V_{CC}$=3V | | 0.2 | 0.6 | |
| | | | $T_a$=25℃, $X_{IN}$=0V, f($X_{CIN}$)=32.8kHz at low power mode ($LM_6$=1) $V_{CC}$=5V | | 20 | 60 | μA |
| | | | $T_a$=25℃, $X_{IN}$=0V, f($X_{CIN}$)=32.8kHz at low power mode ($LM_6$=1) $V_{CC}$=3V | | 4 | 12 | |
| $I_{CC}$ | Supply current | | f($X_{IN}$)=0, f($X_{CIN}$)=0, $V_{CC}$=5V $T_a$=25℃ | | 0.1 | 1 | μA |
| | | | f($X_{IN}$)=0, f($X_{CIN}$)=0, $V_{CC}$=5V $T_a$=70℃ | | | 10 | |
| $V_{RAM}$ | RAM retention voltage | f($X_{IN}$)=0, f($X_{CIN}$)=0 | | 2 | | 5.5 | V |

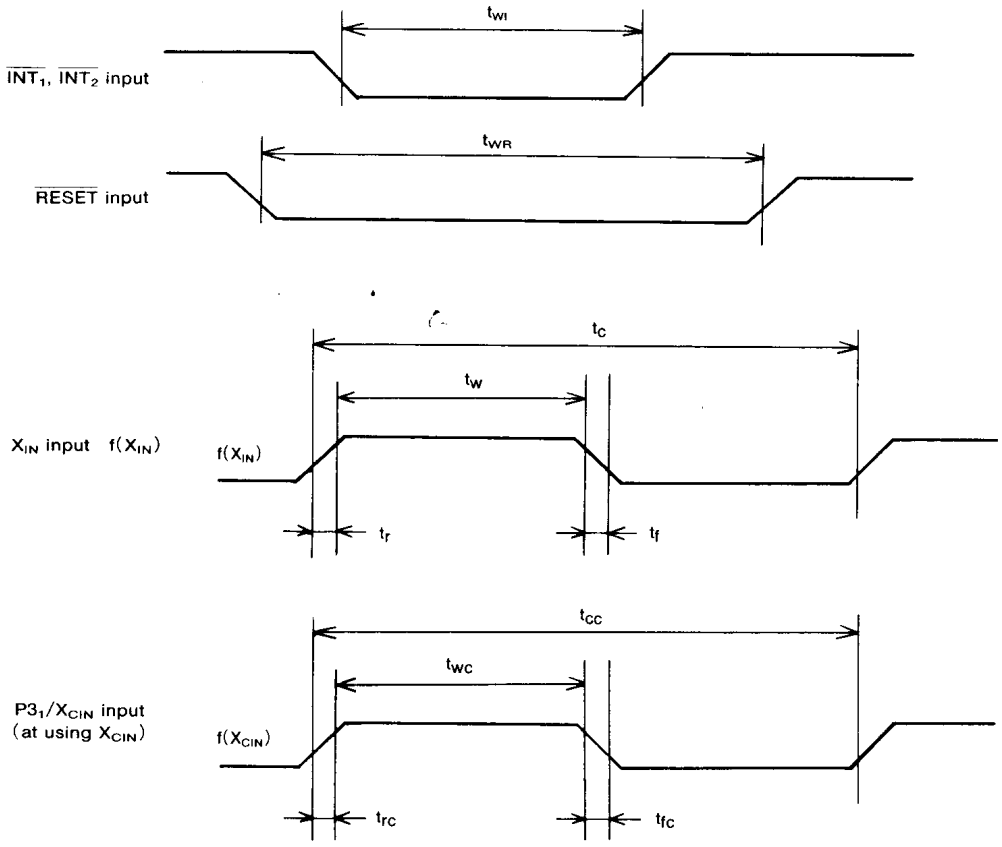
Note 9 : Except when the output type of $P3_5$ is N-channel open drain (mask option).
10 : If $P3_0$ is used as $X_{COUT}$, capability of load driving is lower than the above.

## TIMING REQUIREMENTS

### Memory expanding mode and microprocessor mode ($V_{CC}$=5V±10%, $V_{SS}$=0 V, $T_a$=25℃)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{WI}$ | $\overline{INT_1}$, $\overline{INT_2}$ external clock input pulse width | | 1 | | | μs |
| | | $V_{CC}$=2.7V | 4 | | | |
| $t_{WR}$ | $\overline{RESET}$ external clock input pulse width (Note 13) | | 2 | | | μs |
| | | $V_{CC}$=2.7V | 8 | | | |
| $t_C$ | External clock input cycle time ($X_{IN}$ pin) | | 250 | | | ns |
| $t_W$ | External clock input pulse width ($X_{IN}$ pin) | | 75 | | | ns |
| $t_r$ | External clock rising edge time ($X_{IN}$ pin) | | | | 25 | ns |
| $t_f$ | External clock falling edge time ($X_{IN}$ pin) | | | | 25 | ns |
| $t_{CC}$ | External clock input cycle time ($P3_1/X_{CIN}$ pin, $X_{CIN}$) | | 20 | | | μs |
| $t_{WC}$ | External clock input pulse width ($P3_1/X_{CIN}$ pin, $X_{CIN}$) | | 5 | | | μs |
| $t_{rc}$ | External clock rising edge time ($P3_1/X_{CIN}$ pin, $X_{CIN}$) | | | | 6.2 | μs |
| $t_{fc}$ | External clock falling edge time ($P3_1/X_{CIN}$ pin, $X_{CIN}$) | | | | 6.2 | μs |

Note 13 : Hold $\overline{RESET}$ to "L" level while eight or more rise pulses are input from $X_{IN}$.



# M37412M4-XXXFP

## SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## DESCRIPTION

The M37412M4-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic molded QFP.

This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

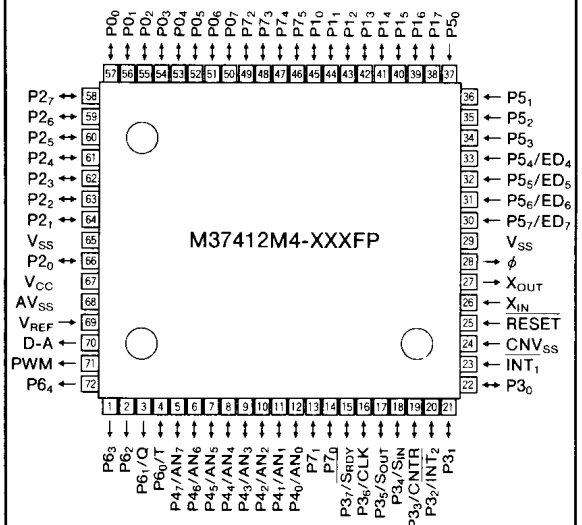
## FEATURES

- Number of basic instructions ..... 69
- Memory size ROM ..... 8192 bytes
  RAM ..... 160 bytes
- Instruction execution time
  ..... 2$\mu$s (minimum instruction, at 4MHz frequency)
- Single power supply ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 4MHz frequency) ..... 15mW
- Subroutine nesting ..... 80 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer ..... 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4, P7) ..... 46
- Input port (Port P5) ..... 8
- Output port (Port P6) ..... 5
- Serial I/O (8-bit) ..... 1
- 8-bit A-D converter ..... 1
- 5-bit D-A converter ..... 1
- 8-bit PWM function ..... 1
- Watchdog timer ..... 1

## APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

## PIN CONFIGURATION (TOP VIEW)




Outline 72P6