Step-up PWM DC/DC Converter

FEATURES

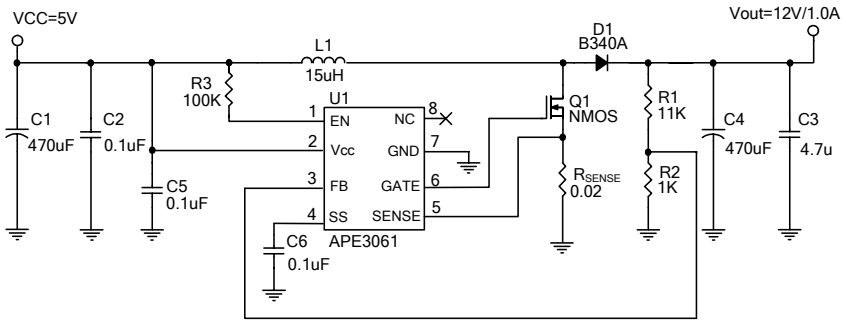
- **Input Voltage : 3.0V to 24V**
- **Output voltage: Define by N-channel MOS**
- **Duty ratio: 0% to 85% PWM control**
- **Oscillation frequency: 500KHz (±20%)**
- **Soft-start time is programmed by outside capacitor**
- **Current Limit is setting by outside resistance**
- **Thermal shutdown protection**
- **Enable/shutdown function**
- **External SW N-channel MOS.**
- **SOP-8L Pb-Free Package.**

DESCRIPTION

The APE3061 is high efficient PWM step-up controller. Designed to drive an external N-channel MOSFET, Output voltage is programmable with 1.0V of standard voltage supply internal, and using externally connected components, output voltage (FB) can be set up at will.

The APE3061 can be operated at switching frequencies of 500kHz allowing for easy filtering and low noise, the size of the external components can be reduced. An enable function and thermal shutdown functions are built inside. The soft-start time can be programmed by outside capacitor; the function prevents overshoot at startup.

TYPICAL APPLICATION



VOUT = VFB x (1+R1/R2) , VFB = 1.0V, R2= 1K~3K
C4 capacitor ESR suggest 30m ~ 100mΩ

PACKAGE ORDERING INFORMATION

APE3061X

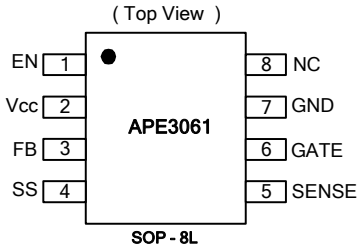
Package Type
M : SOP-8L

ABSOLUTE MAXIMUM RATINGS

VCC Pin Voltage (V_{CC})	VSS - 0.3V to VSS + 26V
Feedback Pin Voltage(V_{FB})	VSS - 0.3V to 12V
EN Voltage (V_{EN})	VSS - 0.3V to VCC
SENSE Voltage (V_{SENSE})	VSS - 0.3V to VCC
SS Pin Voltage (V_{SS})	VSS - 0.3V to VCC
Gate Pin Voltage (V_{GATE})	VSS - 0.3V to VCC
Power Dissipation (P_D)	nternally limited
Storage Temperature Range (T_{ST})	-40 to +150°C
Operating Junction Temperature Range (T_{OPJ})	-20 to +125°C
Operating Supply Voltage (V_{OP})	+3V to +24V
Thermal Resistance from Junction to Case(Rth_{JC})	40°C/W
Thermal Resistance from Junction to Ambient(Rth_{JA})	120°C/W

Note. Rth_{JA} is measured with the PCB copper area of approximately 1 in2 (Multi-layer).

PACKAGE INFORMATION



ELECTRICAL SPECIFICATIONS

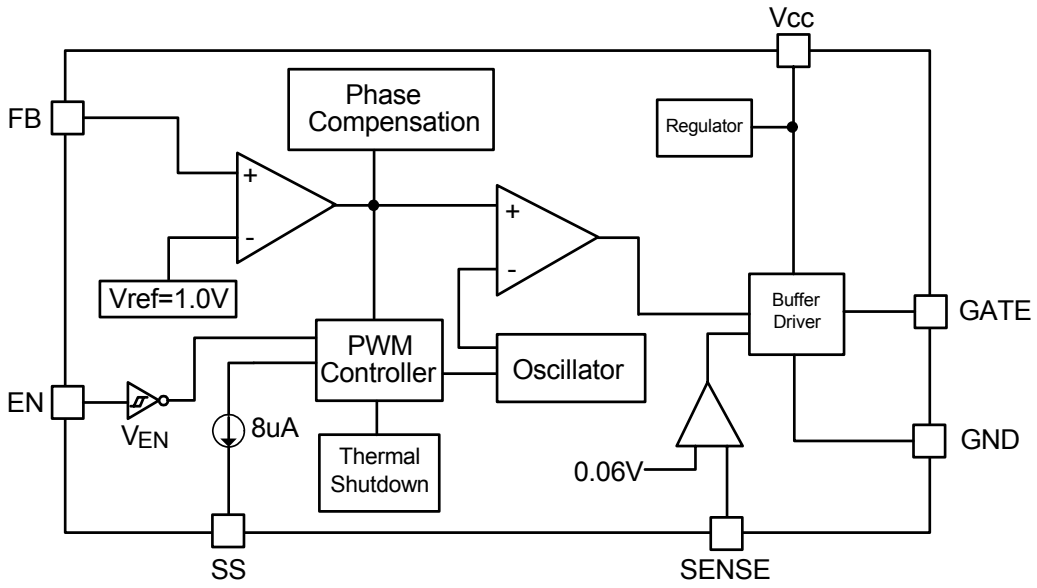
(V_{IN}=5V, V_{OUT}=12V, T_A=25℃, unless otherwise specified)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage	V_{FB}	I_{OUT}=0.1A	0.975	1	1.025	V
Quiescent Current	I_{CCQ}	V_{FB}=1.5V force driver off	-	4	6	mA
Feedback Bias Current	I_{FB}	I_{OUT}=0.1A	-	0.1	0.5	uA
Shutdown Supply Current	I_{SD}	V_{EN} =0V	-	1	10	uA
Oscillation Frequency	F_{OSC}	SW pin	400	500	600	KHz
Sense Voltage	V_{SENSE}		0.05	0.06	0.07	V
Soft Start Current	I_{SS}	V_{SS}=0V	-	8	-	uA
EN Pin Logic Input Threshold Voltage	V_{SH}	High (regulator ON)	2	-	-	V
	V_{SL}	Low (regulator OFF)	-	-	0.8	
EN Pin Input Current	I_{SH}	V_{EN}=2.5V (ON)	-	20	-	uA
	I_{SL}	V_{EN}=0.3V (OFF)	-	-1	-	uA
LX Rise Time	T_{LXR}	C_{LX}=1000pF	-	60	-	ns
LX Fall Time	T_{LXF}	C_{LX}=1000pF	-	60	-	
Efficiency	EFFI	V_{CC}=5V, V_{OUT}=12V, I_{OUT}=1A	-	91	-	%
Maximum Duty Cycle	DC_{MAX}	V_{FB}=0V	-	85	-	%
Minimum Duty Cycle	DC_{MIN}	V_{FB}=1.5V	-	0	-	
Thermal Shutdown Temp	TSD		-	145	-	℃

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPITON
SS	Soft-Start pin
SENSE	Current Limit Sense Voltage
GATE	Gate drive for external N-channel MOSFET.
VCC	VCC supply pin
GND	Ground Pin
FB	Feedback Pin
EN	Shutdown Pin
	H : Normal operation
	L : Shutdown
NC	No connection

BLOCK DIAGRAM



BLOCK DIAGRAM

PWM Control

The APE3061 is high efficient PWM step-up controller. In controllers of the APE3061, the pulse width varies in a range from 0 to 85%, according to the load current. The ripple voltage produced by the switching can easily be removed through a filter because the switching frequency remains constant. Therefore, APE3061 provide a low-ripple power over broad ranges of input voltage and load current.

APPLICATION INFORMATION

Setting the Output Voltage

Application circuit item shows the basic application circuit with APE3061 adjustable output version. The external resistor sets the output voltage according to the following equation:

$$V_{OUT}=1V \times (1+R1/R2)$$

Table 1 Resistor select for output voltage setting

V_{OUT}	R2	R1
12V	1K	11K
15V	1.5K	21K
18V	1K	17K
24V	1.3K	30K

Current Limiting Setting

The current limit threshold is setting by the external resistor (RSENSE) connecting from SENSE pin to GND (refer the application circuit). The internal current limit compared voltage is 60mV. When the SENSE voltage is larger than 60mV, an over-current condition is triggered. Please refer to the formula for setting the minimum current limit value:

$$I_{SW(MAX)} = 60m / RSENSE$$

Note: ISW(MAX) is the maximum N-MOSFET current

Inductor Selection

For most designs, Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = [V_{IN} \times (V_{OUT} - V_{IN})] / (V_{OUT} \times \Delta I_L \times f_{IX})$$

Where is inductor Ripple Current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 15% of the maximum input current 3A, ΔIL=0.45A.

Table 2 Inductor select for output voltage setting (V_{CC}=5V)

V_{OUT}	9V	12V	15V	18V
L1 Value	18uH	15uH	10uH	10uH

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (3A+0.25A).

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used.

The capacitor voltage rating should be at least 1.5 times greater than the input voltage, and often much higher voltage ratings are needed to satisfy.

APPLICATION INFORMATION

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. A low ESR capacitor sized for maximum RMS current must be used. The low ESR requirements needed for low output ripple voltage.

The capacitor voltage rating should be at least 1.5 times greater than the input voltage, and often much higher voltage ratings are needed to satisfy.

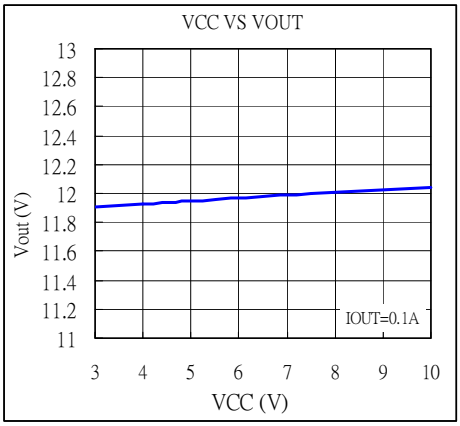
The ESR range of output capacitor is 30m~100mΩ at switch current more than 1.5A. Add a 4.7uF output bypass capacitor in order to reduce output ripple effectively.

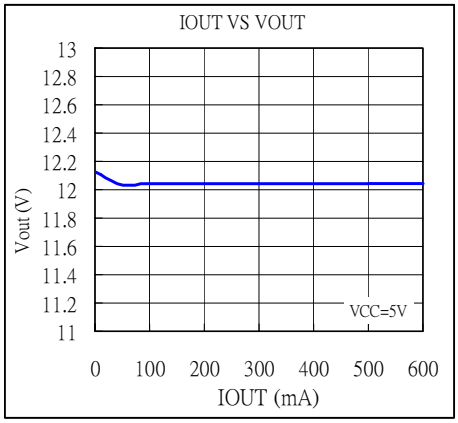
Layout Guidance

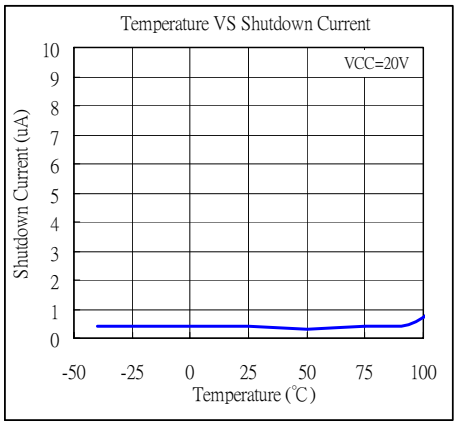
When laying out the PC board, the following suggestions should be taken to ensure proper operation of the APE3061. These items are also illustrated graphically in below.

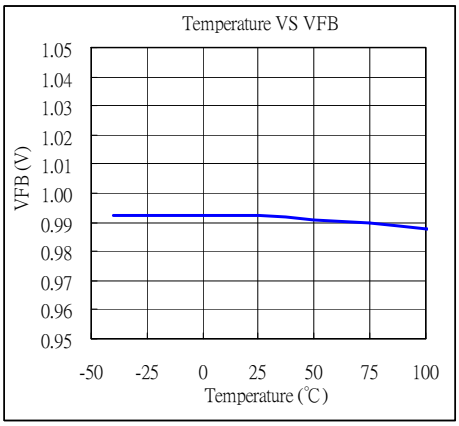
1. The power traces, including the NMOS Drain & Source trace, the inductor and the C1 trace should be kept short, direct and wide to allow large current flow.
2. The ground area for RSENSE and C1 must be closed and C2 closed VCC pin of APE3061 to get good stability.
3. Keep the switching node, away from the sensitive FB node.
4. Do not trace signal line under inductor.

TYPICAL PERFORMANCE CHARACTERISTICS



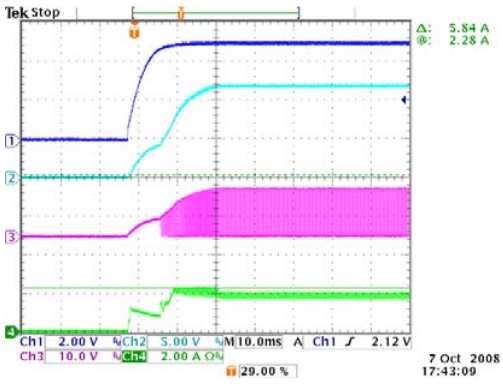






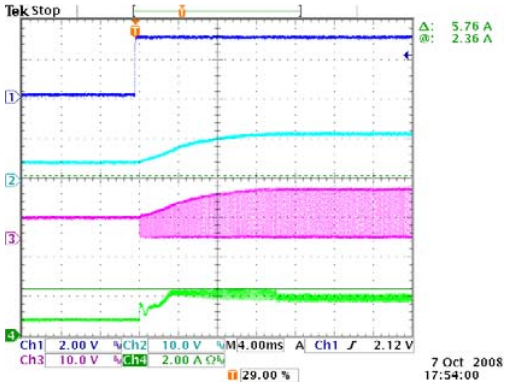
Power-ON Wave

(VCC=5V, Vout=12V, Load=0.7A, SS=0.1uF)

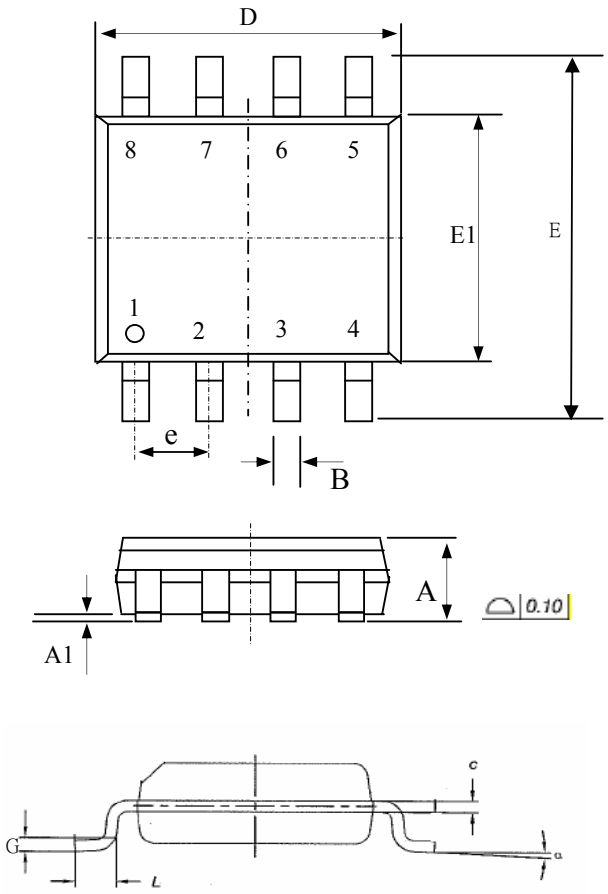


Enable-ON Wave

(VCC=5V, Vout=12V, Load=0.7A, SS=0.1uF)



Package Outline : SOP-8L

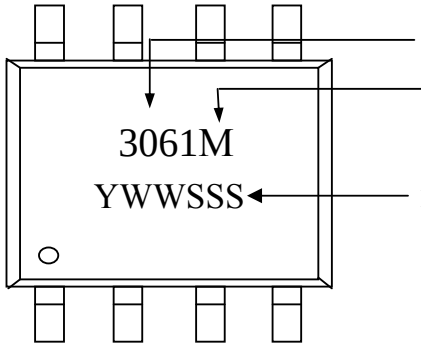


		Millimeters	
SYMBOLS	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
c	0.19	0.22	0.25
D	4.80	4.90	5.00
E	5.80	6.15	6.50
E1	3.80	3.90	4.00
e	1.27 TYP		
G	0.254 TYP		
L	0.38	—	0.90
α	0.00	4.00	8.00

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Part Marking Information & Packing : SOP-8L



Part Number

Package Code

Date Code (YWWSSS)

Y：Last Digit Of The Year

WW：Week

SSS：Sequence