TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM9434

20V P-Channel MOSFET

SOP-8

Pin Definition:
1. Source
2. Source
3. Source
4. Gate
5, 6, 7, 8. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
-20	40 @ V_{GS} = -4.5V	-6.4
	60 @ V_{GS} = -2.5V	-5.1

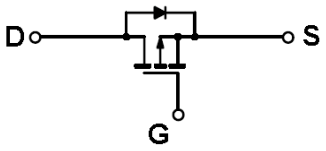
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM9434CS RL	SOP-8	T&R

Absolute Maximum Rating (Ta = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current		I_D	-6.4	A
Pulsed Drain Current		I_{DM}	±10	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	-2.5	A
Maximum Power Dissipation	Ta = 25 °C	P_D	2.5	W
	Ta = 70 °C		1.6	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JC}$	30	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	50	°C/W

Notes:

a. Surface Mounted on 1” x 1” FR4 Board.

b. Pulse width limited by maximum junction temperature

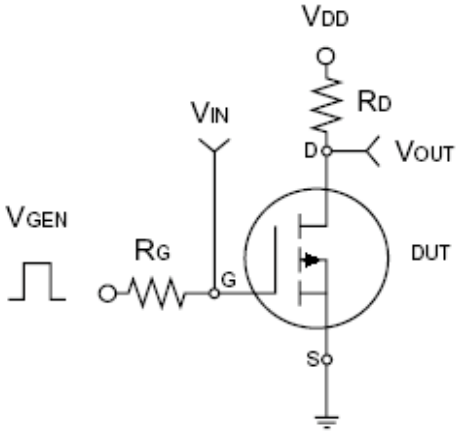
TSM9434

20V P-Channel MOSFET

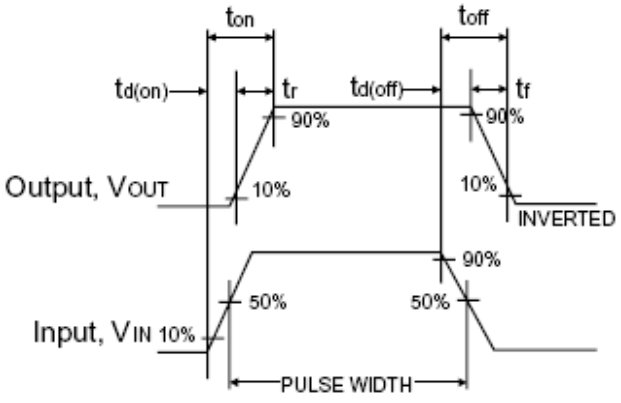
Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = - 250uA	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = - 250uA	$V_{GS(TH)}$	-0.4	--	-1.0	V
Zero Gate Voltage Drain Current	V_{DS} = -16V, V_{GS} = 0V	I_{DSS}	--	--	-1.0	uA
Gate Body Leakage	V_{GS} = ±8V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
On-State Drain Current	V_{DS} ≤-5V, V_{GS} = -4.5V	$I_{D(ON)}$	-10	--	--	A
Drain-Source On-State Resistance	V_{GS} = -4.5V, I_D = -6.4A	$R_{DS(ON)}$	--	31	40	mΩ
	V_{GS} = -2.5V, I_D = -5.1A		--	45	60	
Forward Transconductance	V_{DS} = -9V, I_D = -6.4A	g_{fs}	--	14	--	S
Diode Forward Voltage	I_S = -2.5A, V_{GS} = 0V	V_{SD}	--	- 0.9	-1.2	V
Dynamic[b]						
Total Gate Charge	V_{DS} = -10V, I_D = -6.4A, V_{GS} = -4.5V	Q_g	--	12.5	19	nC
Gate-Source Charge		Q_{gs}	--	1.7	--	
Gate-Drain Charge		Q_{gd}	--	3.3	--	
Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1020	--	pF
Output Capacitance		C_{oss}	--	191	--	
Reverse Transfer Capacitance		C_{rss}	--	140	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = -10V, R_L = 10Ω, I_D = -1A, V_{GEN} = -4.5V, R_G = 6Ω	$t_{d(on)}$	--	25	40	nS
Turn-On Rise Time		t_r	--	43	65	
Turn-Off Delay Time		$t_{d(off)}$	--	71	110	
Turn-Off Fall Time		t_f	--	48	75	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



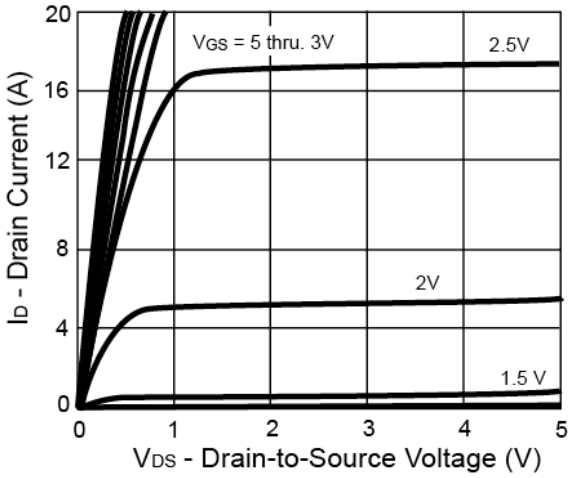
Switching Test Circuit



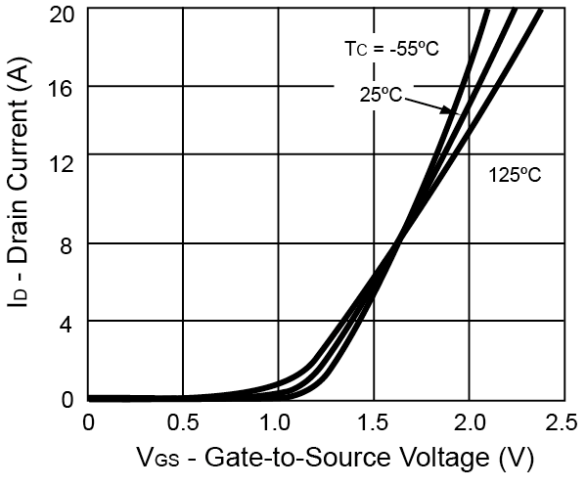
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

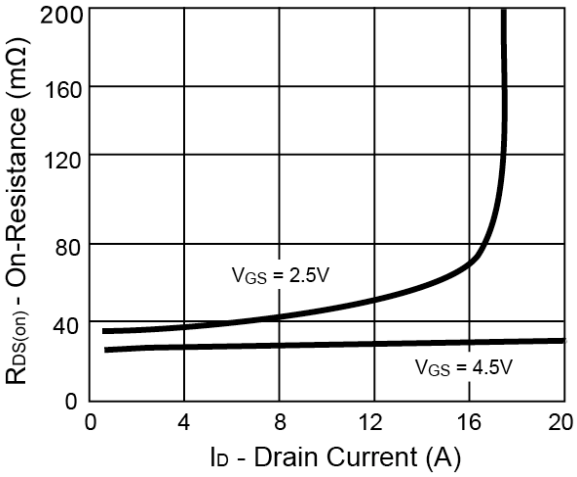
Output Characteristics



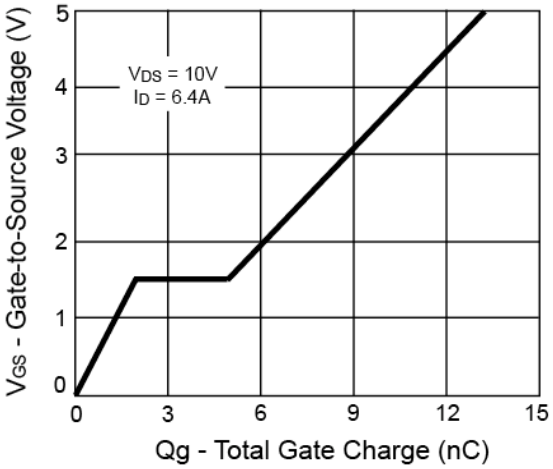
Transfer Characteristics



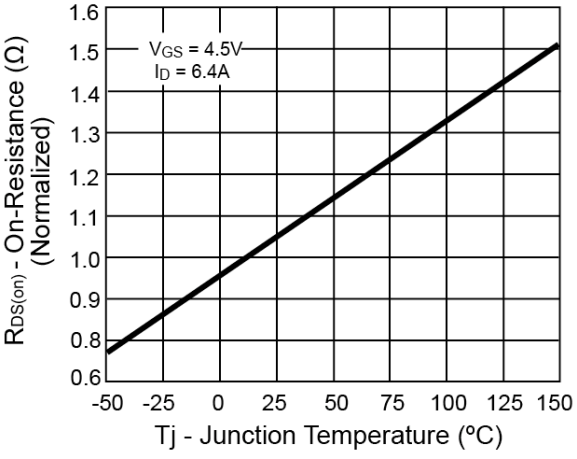
On-Resistance vs. Drain Current



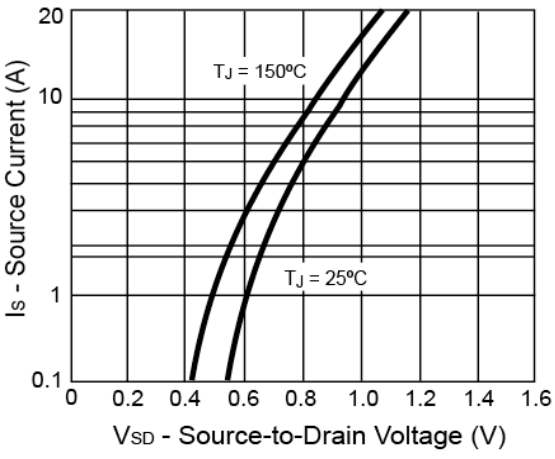
Gate Charge



On-Resistance vs. Junction Temperature

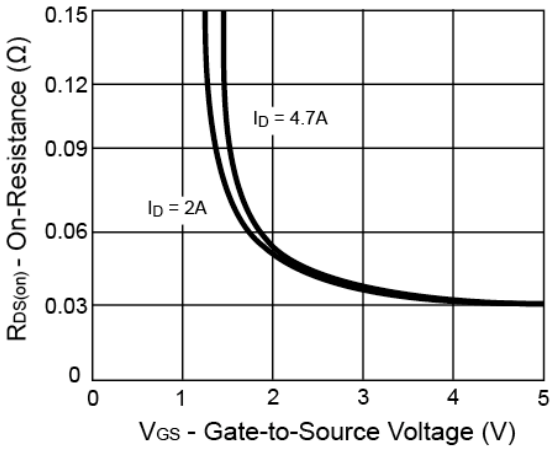


Source-Drain Diode Forward Voltage

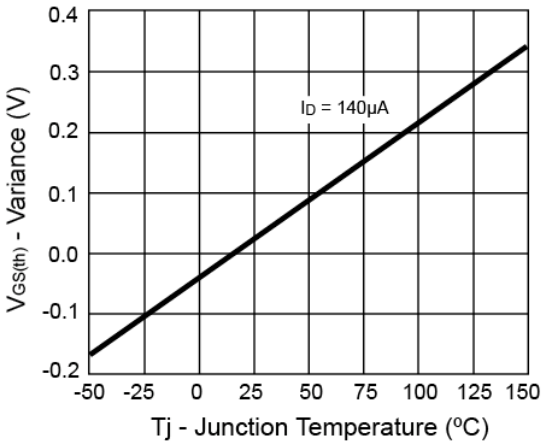


Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

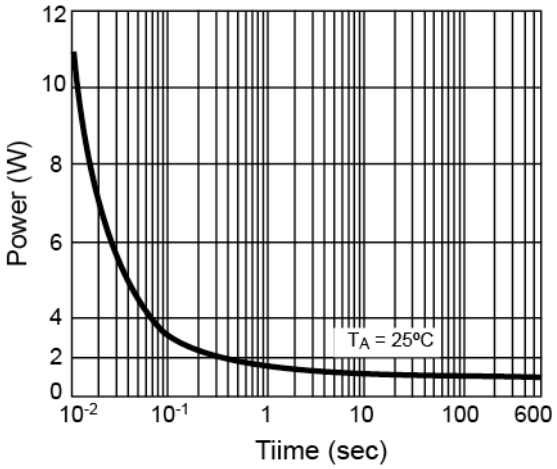
On-Resistance vs. Gate-Source Voltage



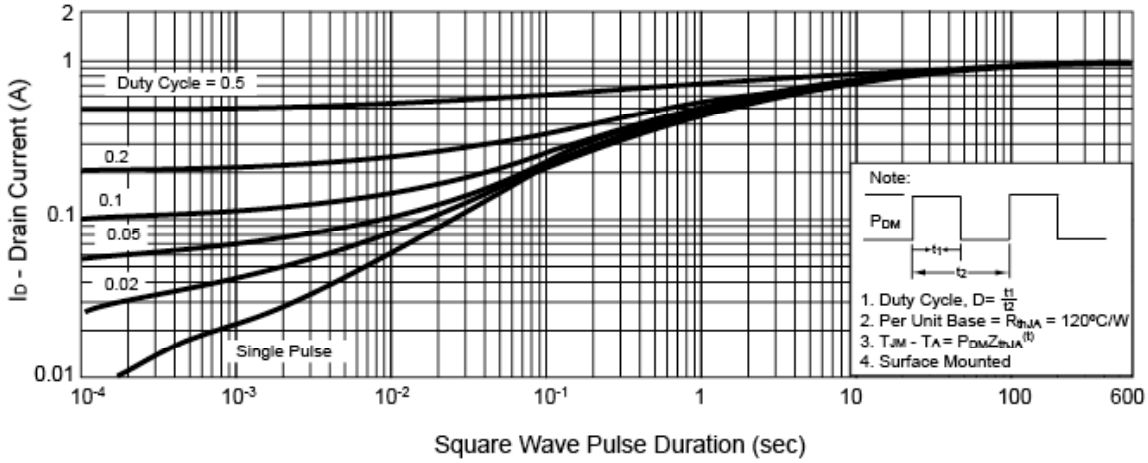
Threshold Voltage



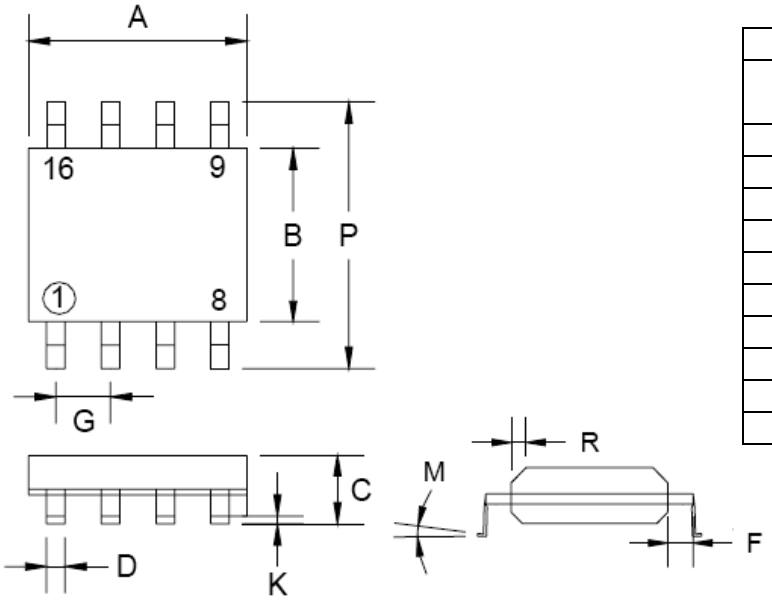
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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