



SANYO Semiconductors

DATA SHEET

LV5106FN — Bi-CMOS IC For cell phone system Power supply

Overview

The LV5106FN is a power supply for a cell phone system that integrates four series regulators, two de-writers, and an LED driver (with 5V output) on a single chip.

Functions

- REG×4 (CMOS output)
- DET circuit (one for REG1, one for VBAT (with reset output))
- Thermal shutdown circuit (150°C)
- Three-color LED driver (charge pump 5V output incorporated)
- FRONT LED driver
- Mic bias output

Features

- Low power consumption 4μA when REG4 and VBATDET operate
30μA when REG1, REG2, REG3, and REG4 + DET1 and VBATDET operate
- Built-in charge pump circuit VBAT : 3.2V to 4.5V, 5V constant output with a load of 80mA
- Built-in 3-color LED drive circuit Three independent colors, 128-step PWM intensity control

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7	V
Allowable power dissipation	Pd max	Ta ≤ 75°C *Mounted on a board.	440	mW
Operating temperature	T _{opr}		-30 to +75	°C
Storage temperature	T _{stg}		-40 to +125	°C

* Mounted on a 50.0mm×50.0mm×0.8mm, glass epoxy board.

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61307 TI PC B8-6923 No.8931-1/6

LV5106FN

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	VBAT	29, 33pin	3.2 to 4.5	V
Supply voltage 2	VBATCP	3pin	3.2 to 5.9	V

Electrical Characteristics $T_a = 25^\circ\text{C}$, VBAT = 3.6V, VCHARGE = 0V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Analog :						
Current dissipation						
Current dissipation 1	I_{CC1}	REG4, VBATDET : ON REG1, 2, 3, charge pump, DET1 : OFF no-load VBAT = 3.2V to 4.2V		4	10	μA
Current dissipation 2	I_{CC2}	REG1, 2, 4, DET1, VBATDET : ON REG3, charge pump : OFF no load		25	35	μA
Current dissipation 3	I_{CC3}	REG3, 4, VBATDET : ON REG1, 2, DET1, charge pump : OFF no load		20	28	μA
Current dissipation 4	I_{CC4}	REG1, 2, 3, 4, DET1, VBATDET : ON charge pump : OFF no load		30	42	μA
Current dissipation 5	I_{CC5}	REG1, 2, 3, 4, DET1, VBATDET : ON charge pump : OFF no load ECO : L		15	21	μA
Current dissipation 6	I_{CC6}	REG1, 2, 3, 4, charge pump, DET1, VBATDET : ON no load		5	8	mA
REG1						
Output voltage 1	V_{O1}	$I_O = 30\text{mA}$, ECO = H	2.74	2.8	2.86	V
Output voltage 2	V_{O1E}	$I_O = 30\text{mA}$, ECO = L	2.71	2.8	2.89	V
Output voltage 3	ΔV_{O1}	($I_O = 30\text{mA}$, REG1 output voltage at ECO = H) - ($I_O = 10\text{mA}$, REG1 output voltage at $I_O = 10\text{mA}$ and ECO = L)	0	15	35	mV
Output voltage 4	ΔV_{O2}	$I_O = 30\text{mA}$ (charge-pump on-time REG1 output voltage) - (charge-pump off-time REG1 output voltage)	-35		35	mV
Drop out voltage	VDR1	VBAT = 2.7V, $I_O = 30\text{mA}$		0.04	0.06	V
Load regulation	ΔV_{OLO1}	$I_O = 1$ to 150mA		10	50	mV
Line regulation	ΔV_{OLN1}	VBAT = 3.3 to 4.5V, $I_O = 1\text{mA}$		10	60	mV
Output voltage temperature coefficient	$\Delta V_{O1}/\Delta T_j$	$T_a = -25$ to 75°C , $I_O = 30\text{mA}$		± 100		ppm/ $^\circ\text{C}$
Ripple rejection	V_R1	VBAT = 3.6V, $I_O = 30\text{mA}$, VRR = -20dBV, $f_{RR} = 1\text{kHz}$		65		dB
Output noise voltage	V_{ON1}	$I_O = 30\text{mA}$, 20Hz < f < 20kHz		75		μVrms
REG2						
Output voltage 1	V_{O2}	$I_O = 30\text{mA}$, ECO = H	2.55	2.6	2.65	V
Output voltage 2	V_{O2E}	$I_O = 30\text{mA}$, ECO = L	2.53	2.6	2.67	V
Drop out voltage	VDR1	VBAT = 2.5V, $I_O = 30\text{mA}$		0.06	0.12	V
Load regulation	ΔV_{OLO2}	$I_O = 1$ to 100mA		10	100	mV
Line regulation	ΔV_{OLN2}	VBAT = 3.3 to 4.5V, $I_O = 1\text{mA}$		10	60	mV
Output voltage temperature coefficient	$\Delta V_{O2}/\Delta T_j$	$T_a = -25$ to 75°C , $I_O = 30\text{mA}$		± 100		ppm/ $^\circ\text{C}$
Ripple rejection	V_R2	VBAT = 3.6V, $I_O = 30\text{mA}$, VRR = -20dBV, $f_{RR} = 1\text{kHz}$		65		dB
Output noise voltage	V_{ON2}	$I_O = 30\text{mA}$, 20Hz < f < 20kHz		75		μVrms

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
REG3						
Output voltage 1	V _{O3}	I _O = 30mA, ECO = H	2.45	2.5	2.55	V
Output voltage 2	V _{O3E}	I _O = 30mA, ECO = L	2.43	2.5	2.57	V
Drop out voltage	VDR3	V _{BAT} = 2.4V, I _O = 30mA		0.06	0.12	V
Load regulation	ΔV _{OL03}	I _O = 1 to 50mA		10	50	mV
Line regulation	ΔV _{OLN3}	V _{BAT} = 3.3 to 4.5V, I _O = 1mA		10	60	mV
Output voltage temperature coefficient	ΔV _{O3} /ΔT _j	T _a = -25 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection	V _{R3}	V _{BAT} = 3.6V, I _O = 30mA, VRR = -20dBV, f _{RR} = 1kHz		65		dB
Output noise voltage	V _{ON3}	I _O = 30mA, 20Hz < f < 20kHz		75		μVrms
REG4						
Output voltage	V _{O4}	I _O = 30mA	2.91	3	3.09	V
Drop out voltage	VDR3	V _{BAT} = 2.9V, I _O = 30mA		0.06	0.12	V
Load regulation	ΔV _{OL04}	I _O = 1 to 50mA		10	50	mV
Line regulation	ΔV _{OLN4}	V _{BAT} = 3.3 to 4.5V, I _O = 1mA		10	60	mV
Output voltage temperature coefficient	ΔV _{O4} /ΔT _j	T _a = -25 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection	V _{R4}	V _{BAT} = 3.6V, I _O = 30mA, VRR = -20dBV, f _{RR} = 1kHz		55		dB
Output noise voltage	V _{ON4}	I _O = 30mA, 20Hz < f < 20kHz		75		μVrms
DET1						
Detection voltage	VD1	H→L	2.45	2.5	2.55	V
Hysteresis width	ΔV _{H1}		75	125	175	mV
Detection voltage temperature coefficient	ΔVD1/ΔT _j	T _a = -25 to 75°C		±100		ppm/°C
VBATDET						
Detection voltage	VDB	H→L	3.04	3.1	3.16	V
Hysteresis width	ΔVHB		93	155	217	mV
Output pull-up resistance	RPDET _B		1.4	1.8	2.2	MΩ
Detection voltage temperature coefficient	ΔVDB/ΔT _j	T _a = -25 to 75°C		±100		ppm/°C
Charge pump						
Output voltage 1	VCPO1	V _{BAT} = 3.2 to 5.9V, Load current 80mA	4.8	5	5.2	V
Oscillation frequency	CPOSC		0.7	1	1.3	MHz
Output ripple	VRCP	V _{BAT} = 3.6, Load current 80mA		±200		mVp-p
Efficiency	η	V _{BAT} = 3.2, Load current 80mA		72		%
LED driver						
LEDR output voltage	VLR	I _O = 40mA	0	0.1	0.2	V
LEDG output voltage	VLG	I _O = 40mA	0	0.1	0.2	V
LEDB output voltage	VLB	I _O = 40mA	0	0.1	0.2	V
LEDF output voltage	VLF	I _O = 40mA	0	0.15	0.3	V
LEDR OFF leak	ILR			0	1	μA
LEDG OFF leak	ILG			0	1	μA
LEDB OFF leak	ILB			0	1	μA
LEDF OFF leak	ILF			0	1	μA
Mic bias						
Output ON resistance	RMO	I _O = 10mA		10		Ω
OFF leakage current	ILM			0	1	μA
Output voltage (GP_0, 1)						
Output H level	V _{OH}	I _O = 1mA	REG10 -0.3		REG10	V
Output L level	V _{OL}	I _O = 1mA	0		0.3	V

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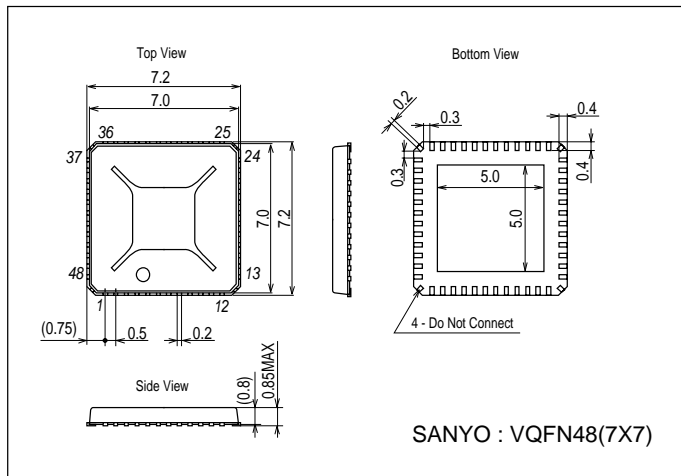
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input voltage 1 (SDATA, SEN, SCLK)						
H level	V _{INH1}	Input H level	REG10 ×0.8		REG10	V
L level	V _{INL1}	Input L level	0		REG10 ×0.2	V
Input voltage 2 (T_CNT, TCXOCNT, ECO, REG3CTL, REG12CTL, PWRON, RTCINT, MSSELO, MSSELOC, KEYSENSE4, HWRESET)						
H level	V _{INH2}	Input H level	REG40 ×0.8		REG40	V
L level	V _{INL2}	Input L level	0		REG40 ×0.2	V
Input voltage 3 (RESOUT_N)						
H level	V _{INH3}	Input H level	REG40 ×0.8		REG40	V
L level	V _{INL3}	Input L level	0		REG40 ×0.2	V
Input voltage 4 (CHG_G)						
H level	V _{INH4}	Input H level	REG40 ×0.8		6	V
L level	V _{INL4}	Input L level	0		REG40 ×0.2	V
Input voltage 5 (Vcharge)						
H level	V _{INH5}	Input H level	4.4		6	V
L level	V _{INL5}	Input L level	0		3.6	V
Input voltage 6 (VBATBK)						
H level	V _{INH6}	Input H level	REG40 ×0.8		VBAT	V
L level	V _{INL6}	Input L level	0		REG40 ×0.2	V
Serial bus :						
Serial transfer timing						
Cycle time	tcy1	SCLK clock cycle	300			ns
Data setup time 1	ts0	SDEN setup time for rise of SCLK	150			ns
Data setup time 2	ts1	SDATA setup time for rise of SCLK	150			ns
Data hold time 1	th0	SDEN hold time for fall of SCLK	150			ns
Data hold time 2	th1	SDATA hold time for rise of SCLK	150			ns
Pulse width 1	tw1L	SCLK L-period pulse width	150			ns
Pulse width 2	tw1H	SCLK H-period pulse width	150			ns
Pulse width 3	tw2L	SDEN L-period pulse width	1			μs

Package Dimensions

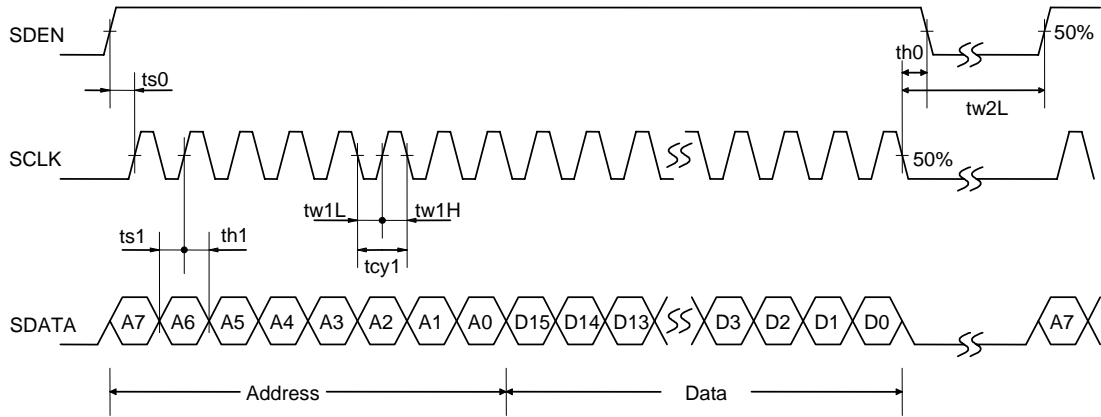
unit : mm (typ)

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Serial transfer timing conditions



Data length : 24bit

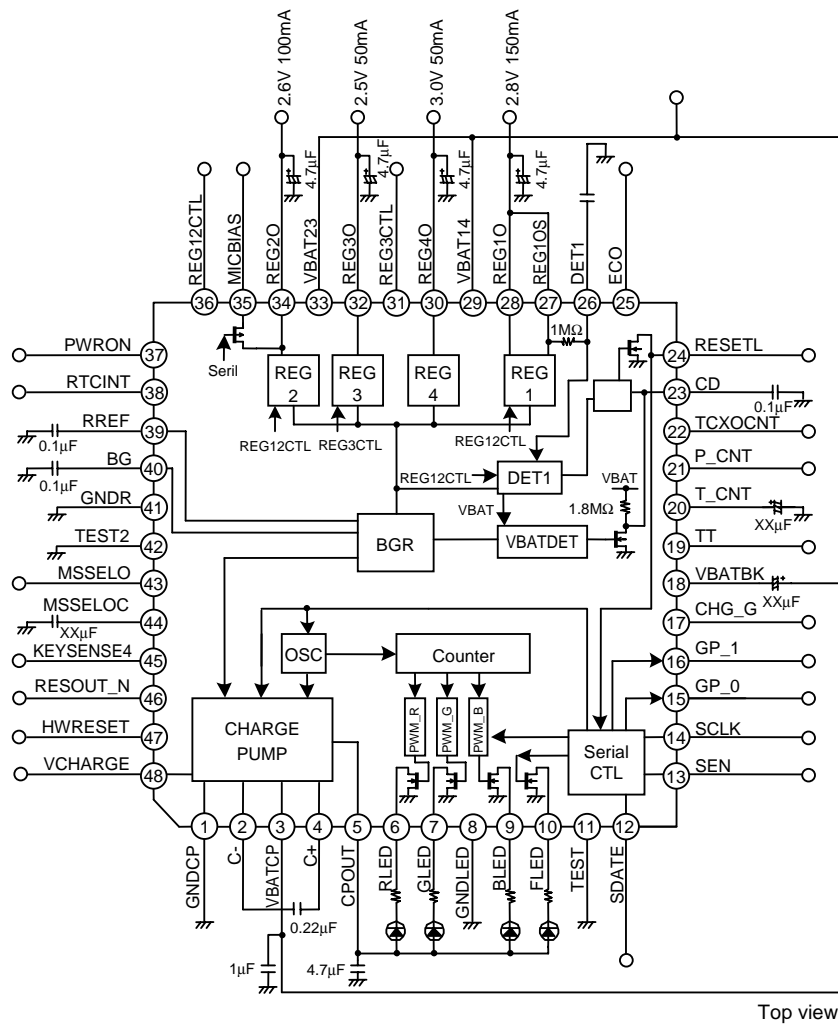
Clock frequency : 3MHz or less

"SDATA" is taken in at fall of "SDEN" when "SCLK" of 24 clock is entered during H period of "SDEN."

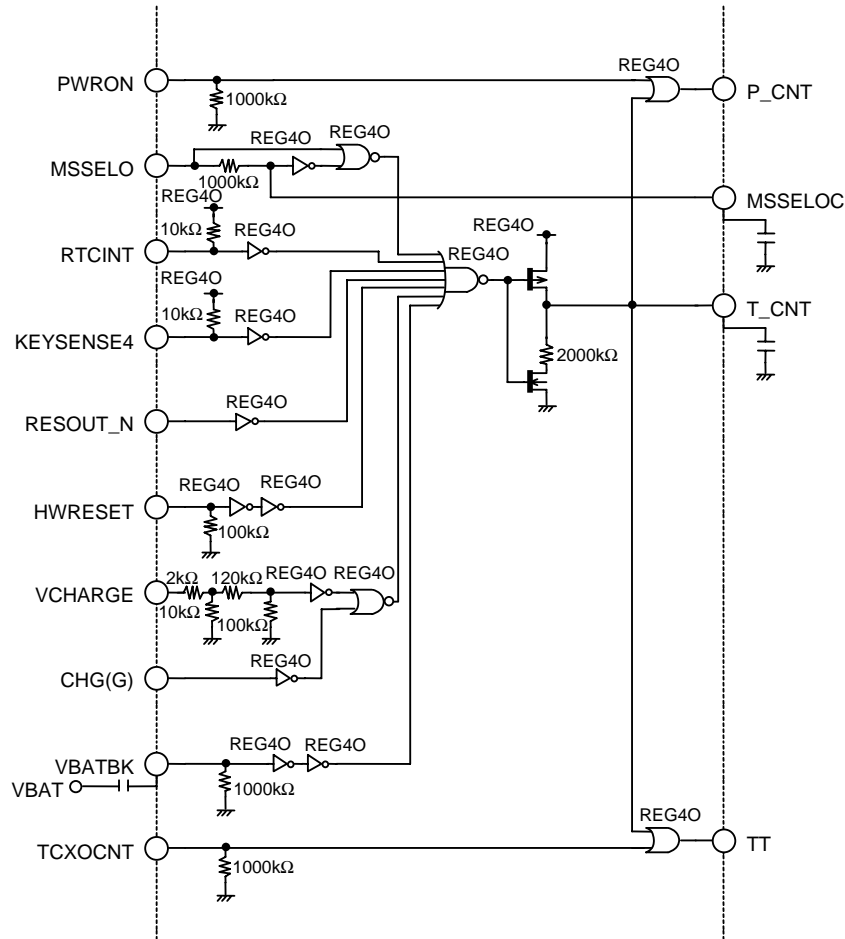
(Note) "SDATA" is not taken in when "SCLK" is 23 clock or less during H period of "SDEN."

When "SCLOCK" exceeds 25 clock, "SDATA" is taken in at the 24th clock, and subsequent "SDATA" is ignored.

Block Diagram



Power Control Block Diagram



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