STL8DN6LF3

Dual N-channel 60 V, 20 mΩ, 7.8 A STripFET™ III Power MOSFET in PowerFLAT™ 5x6 dual pad

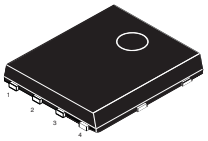
Preliminary data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STL8DN6LF3	60 V	< 30 mΩ	7.8 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- Logic level $V_{GS(th)}$
- 175 °C junction temperature
- 100% avalanche rated



PowerFLAT™ 5x6 dual pad

Applications

- Switching applications
- Automotive

Description

This device is a dual N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

Figure 1. Internal schematic diagram

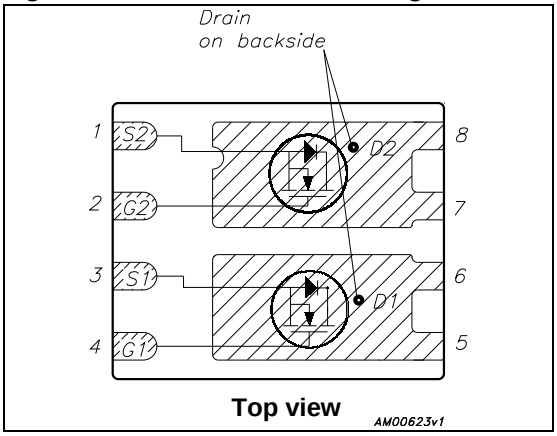


Table 1. Device summary

Order code	Marking	Package	Packaging
STL8DN6LF3	8DN6LF3	PowerFLAT™ 5x6 dual pad	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	60	V
V_{GS}	Gate-source voltage	±20	V
I_D (1),(2)	Drain current (continuous) at T_C = 25 °C	20	A
I_D	Drain current (continuous) at T_C = 100 °C	20	A
I_D (4)	Drain current (continuous) at T_{pcb} = 25 °C	7.8	A
I_D (4)	Drain current (continuous) at T_{pcb}=100 °C	5.5	A
I_{DM} (3),(4)	Drain current (pulsed)	31	A
P_{TOT}	Total dissipation at T_C = 25°C	65	W
P_{TOT} (4)	Total dissipation at T_{pcb} = 25°C	4.3	W
E_{AS} (5)	Single pulse avalanche energy	175	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Specified by design. Not subject to production test.
2. Current is limited by bonding, with an R_{thJC} = 2.3 °C/W the chip is able to carry 30 A at 25 °C.
3. Pulse width limited by safe operating area
4. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec
5. Starting T_J= 25 °C, I_D= 10 A, V_{DD}= 25 V, per channel, 100% tested.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.3	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	35	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 60 V			1	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1		3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 4 A V_{GS}= 5 V, I_D= 4 A		20 30	30 44	mΩ mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	835 167 15	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=44 V, I_D = 7.8 A V_{GS} =10 V *Figure 3*	-	17 TBD TBD	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=TBD, I_D= 4 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 2*	-	TBD	-	ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		7.8	A
I_{SDM}(1)	Source-drain current (pulsed)		-		31	A
V_{SD}(2)	Forward on voltage	I_{SD} = TBD A, V_{GS}=0	-		TBD	V
t_{rr}	Reverse recovery time	I_{SD} = TBD A, di/dt = 100 A/µs, V_{DD}=TBD V, Tj=150 °C	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

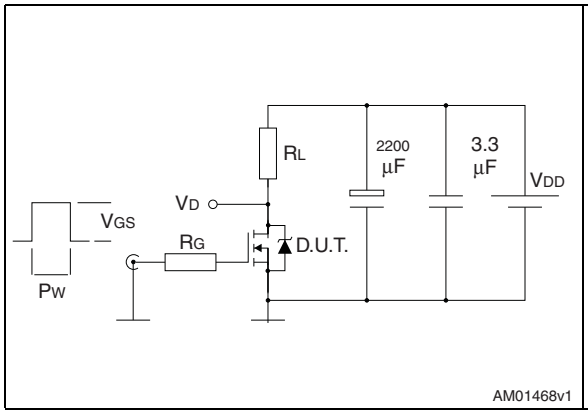


Figure 3. Gate charge test circuit

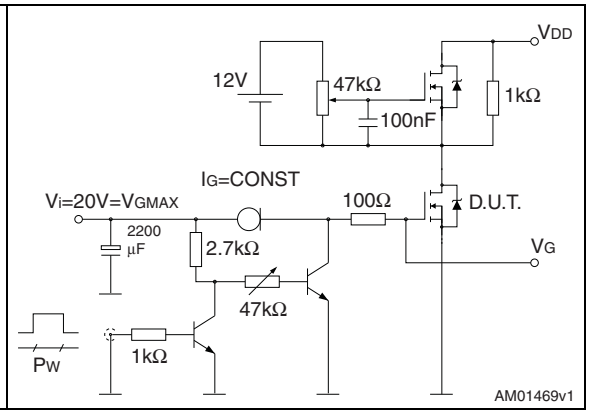


Figure 4. Test circuit for inductive load switching and diode recovery times

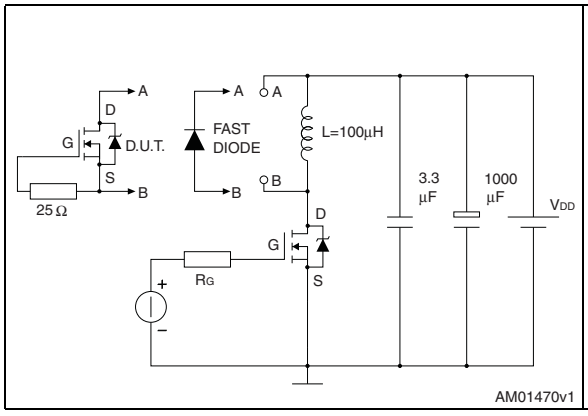


Figure 5. Unclamped inductive load test circuit

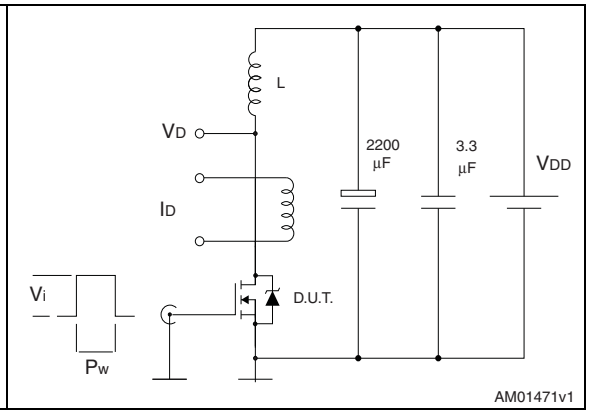


Figure 6. Unclamped inductive waveform

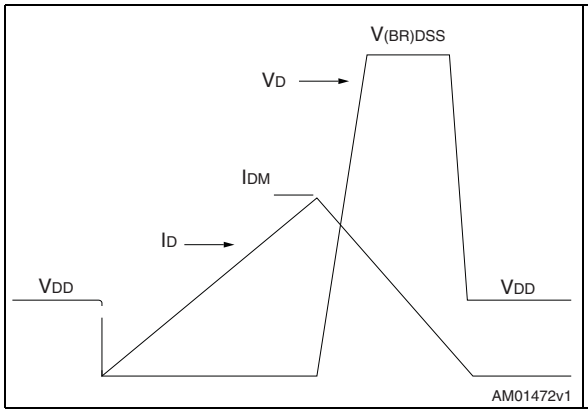
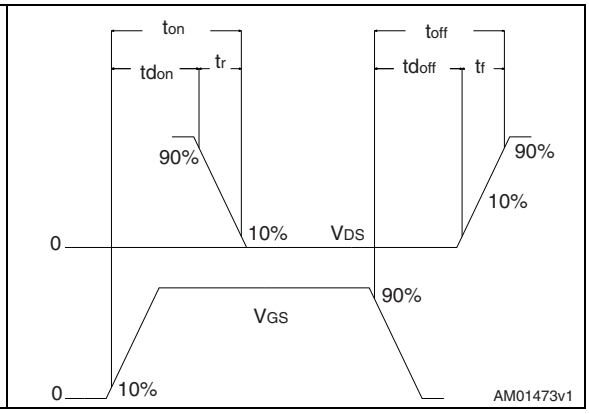


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 dual pad (ribbon) mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 8. PowerFLAT™ 5x6 dual pad (ribbon) drawing

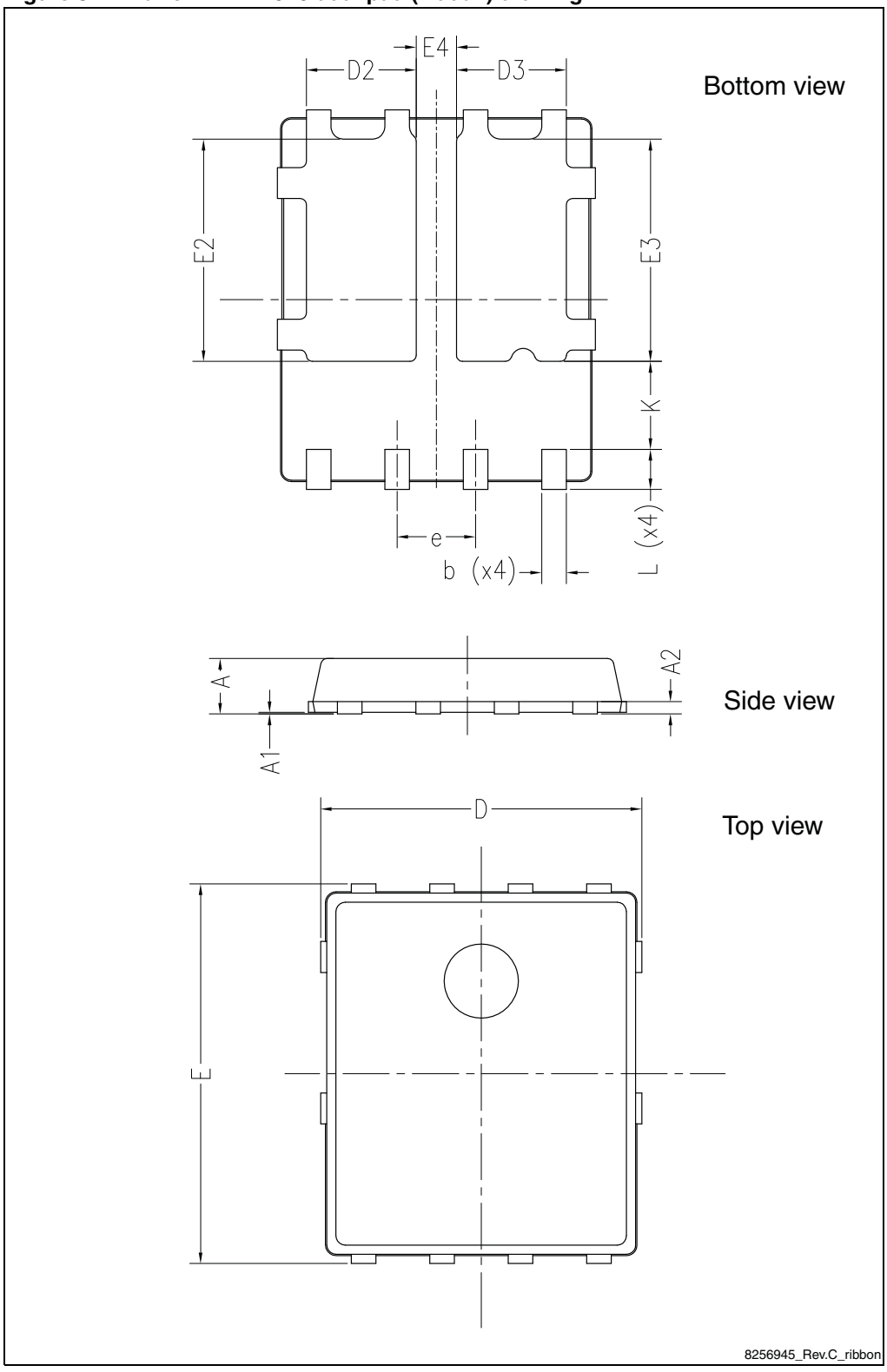
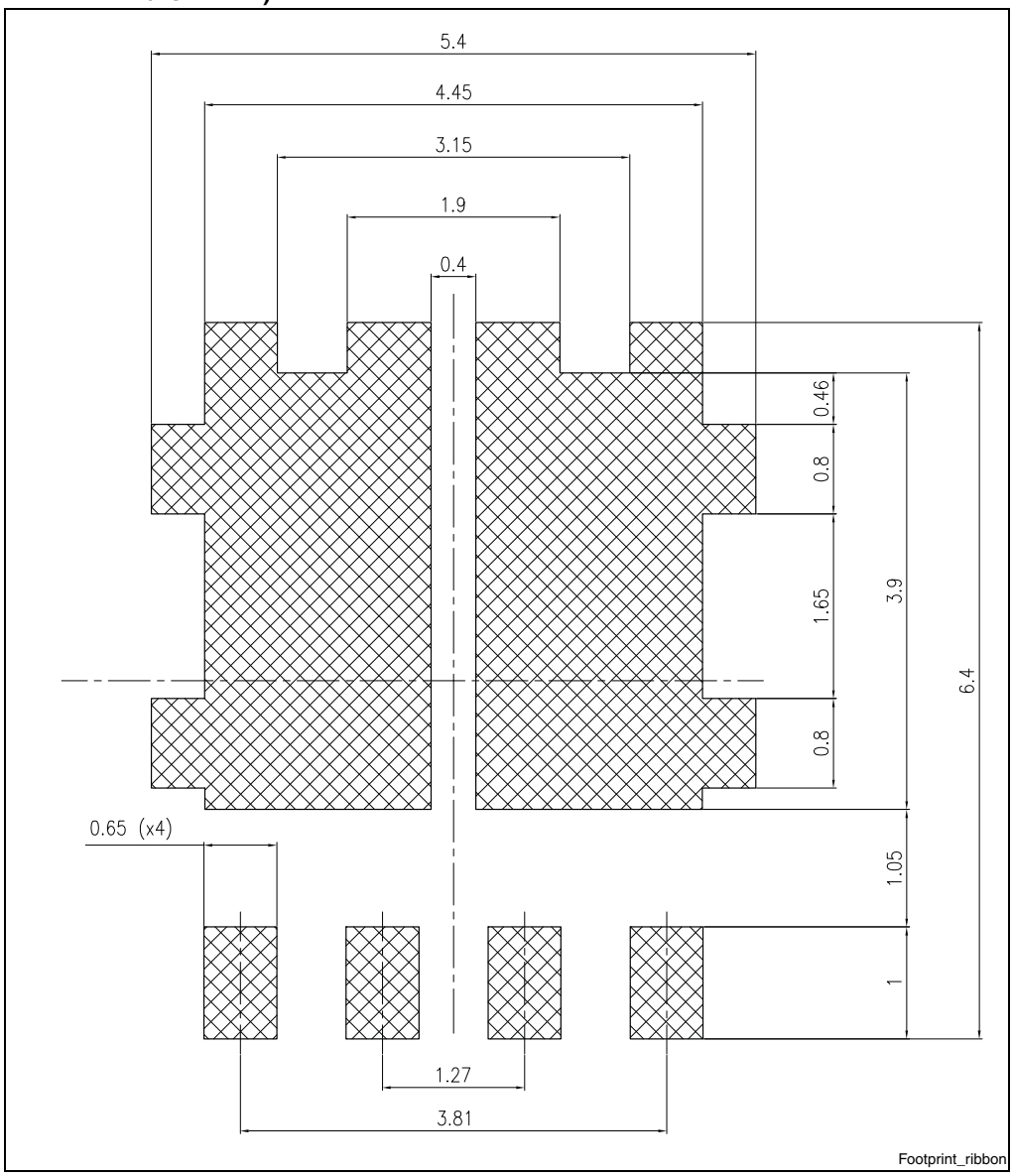


Figure 9. PowerFLAT™ 5x6 dual pad (ribbon) recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Oct-2011	1	First release.

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