Ordering number : ENN6251

CMOS IC

LC897127K

SCSI CD-ROM Decoder with On-Chip DVD Interface

Overview

The LC897127K is a CD-ROM decoder that includes an on-chip DVD interface. Since the LC897127K also includes an on-chip SCSI interface, it can be used to implement a SCSI-compatible DVD-ROM drive simply by combining it with a DVD decoder. It can also operate as an independent SPC functional unit.

Functions

- CD-ROM ECC function, subcode read function, SCSI I/F, CAV audio function, DVD I/F
- ATAPI-to-SCSI conversion function, DMA I/F-to-SCSI conversion function

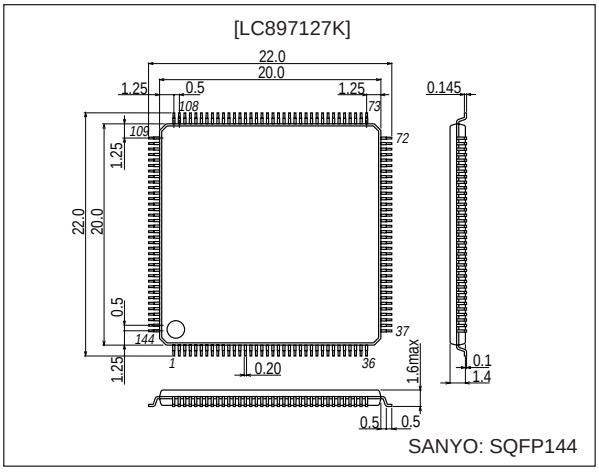
Features

- Built-in SCSI I/F (Built-in register for SCAM selection)
- 20× speed and transfer speed of 10 Mbytes/s supported using EDO-DRAM (×16, 70 ns)
- 32× speed and transfer speed of 10 Mbytes/s supported using EDO-DRAM (16×, 50 ns)
- Up to 4 Mbits of buffer RAM connectable
- CD main channel and C2 flag areas in buffer RAM can be freely set by user
- Built-in batch transfer function (function for sending CD main channel, C2 flag, etc. at one time)
- Built-in multi block transfer function (function for sending several blocks at one time)
- Built-in subcode buffering function and CD text support
- Built-in CAV audio function
- 20 Mbytes/s transfer supported
- Built-in DVD I/F
- Built-in ATAPI I/F-to-SCSI conversion function
- Built-in DMA I/F-to-SCSI conversion function

Package Dimensions

unit: mm

3214-SQFP144



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Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
Input/output voltage	$V_I V_O$	Ta = 25°C	–0.3 to V_{DD} +0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	550	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering temperature (pin part only)		10s	260	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.25	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Input high-level voltage	V_{IH1}	TTL levels	(1)	2.2			V
Input low-level voltage	V_{IL1}					0.8	V
Input high-level voltage	V_{IH2}	TTL levels	(9)	2.2	—	—	V
Input low-level voltage	V_{IL2}	with pull-up resistor		—	—	0.8	V
Input high-level voltage	V_{IH3}	TTL levels	(2)	2.2	—	—	V
Input low-level voltage	V_{IL3}	Schmitt		—	—	0.8	V
Input high-level voltage	V_{IH3}	TTL levels	(11)	2.2	—	—	V
Input low-level voltage	V_{IL3}	Schmitt with pull-down resistor		—	—	0.8	V
Input high-level voltage	V_{IH4}	TTL levels	(12)	2.2	—	—	V
Input low-level voltage	V_{IL4}	Schmitt with pull-up resistor		—	—	0.8	V
Input high-level voltage	V_{IH4}	CMOS levels	(3)	0.8 V_{DD}	—	—	V
Input low-level voltage	V_{IL4}	Schmitt		—	—	0.2 V_{DD}	V
Input high-level voltage	VI_{H5}		(4), (8), (10)	2.0		—	V
Input low-level voltage	V_{IL5}					0.8	V
Output high-level voltage	V_{OH1}	I_{OH1} = –12 mA	(6)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL1}	I_{OL1} = 12 mA		—	—	0.4	V
Output high-level voltage	V_{OH2}	I_{OH2} = –8 mA	(7), (11)	2.4		—	V
Output low-level voltage	V_{OL2}	I_{OL2} = 8 mA				0.4	V
Output high-level voltage	V_{OH2}	I_{OH2} = –2 mA	(9), (5)	2.4		—	V
Output low-level voltage	V_{OL2}	I_{OL2} = 2 mA				0.4	V
Output low-level voltage	V_{OL4}	I_{OL4} = 48 mA	(10)			0.4	V
Input leakage current	I_{IL}	V_I = V_{SS}, V_{DD}	All input pins	–25		+25	µA
Pull-up resistance	R_{UP}		(5), (9)	60	120	240	kΩ
Pull-down resistance	R_{DOWN}		(11)	60	120	240	kΩ

Applicable pin sets are as follows.

INPUT (1) TEST0 to TEST4, CSCTRL, SUA0 to SUA6, C2PO, SDATA, BCK, LRCK, SCOR, WFCK, SBS0, MCK2SEL
(2) $\overline{\text{RESET}}$
(3) $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$
(4) SCSISEL, XTALSEL

OUTPUT (5) $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{SWAIT}}$
(6) MCK
(7) EXCK, DSDATA, DLRCK, DBCK, $\overline{\text{RAS0}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$, $\overline{\text{OE}}$, $\overline{\text{UWE}}$, $\overline{\text{LWE}}$, RA0 to RA8, HDBDIR

INOUT (8) $\overline{\text{ACK}}$, $\overline{\text{ATN}}$
(9) D0 to D7, IO0 to IO15
(10) $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, $\overline{\text{BSY}}$, I/O, $\overline{\text{MSG}}$, $\overline{\text{SEL}}$, $\overline{\text{RST}}$, $\overline{\text{REQ}}$, C/D
(11) DRESP, DREQ, HDB0 to HDB7
(12) IOP0 to IOP7 (No pull-up resistor used when these pins are used as pins HDB0 to HDB7)

Note: Pins XTAL0, XTALCK0, XTAL1, XTALCK1, and X1EN are not included in DC characteristics.

SCSI Pin Input Characteristics

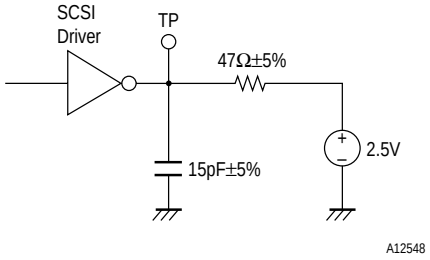
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input threshold voltage	V_{t+t1}	V_{DD} = 4.50 to 5.50 V		1.60	2.00	V
	V_{t-t1}		0.80	1.10		V
Hysteresis width	ΔV_{tt1}	V_{DD} = 5.0 V	0.41	0.5		V

Active Low Output Characteristics

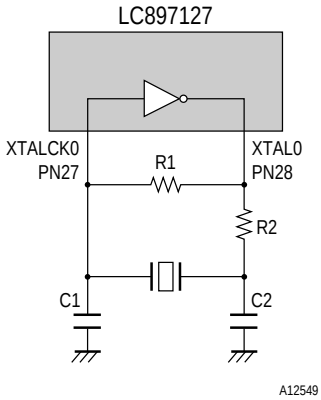
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output high-level voltage	V_{OH}		2.5			V
Output low-level voltage	V_{OL}				0.4	V

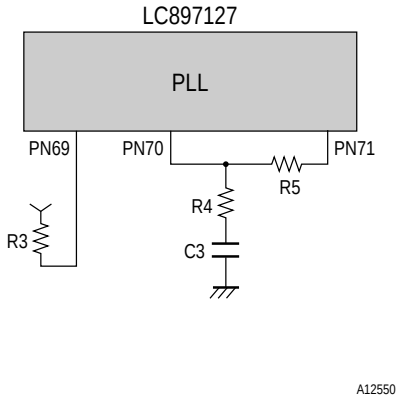
Note: Only applies to the active-low output pins $\overline{DB0}$ to $\overline{DB7}$, $\overline{REQ}$, and $\overline{DBPB}$

Rise Time Test Circuit



Recommended Oscillator and PLL Circuits





R1 = 120 kΩ, R2 = 47 Ω, C1 = 30 pF

Crystal element oscillator frequency XTALCK0 = 16.9344 MHz

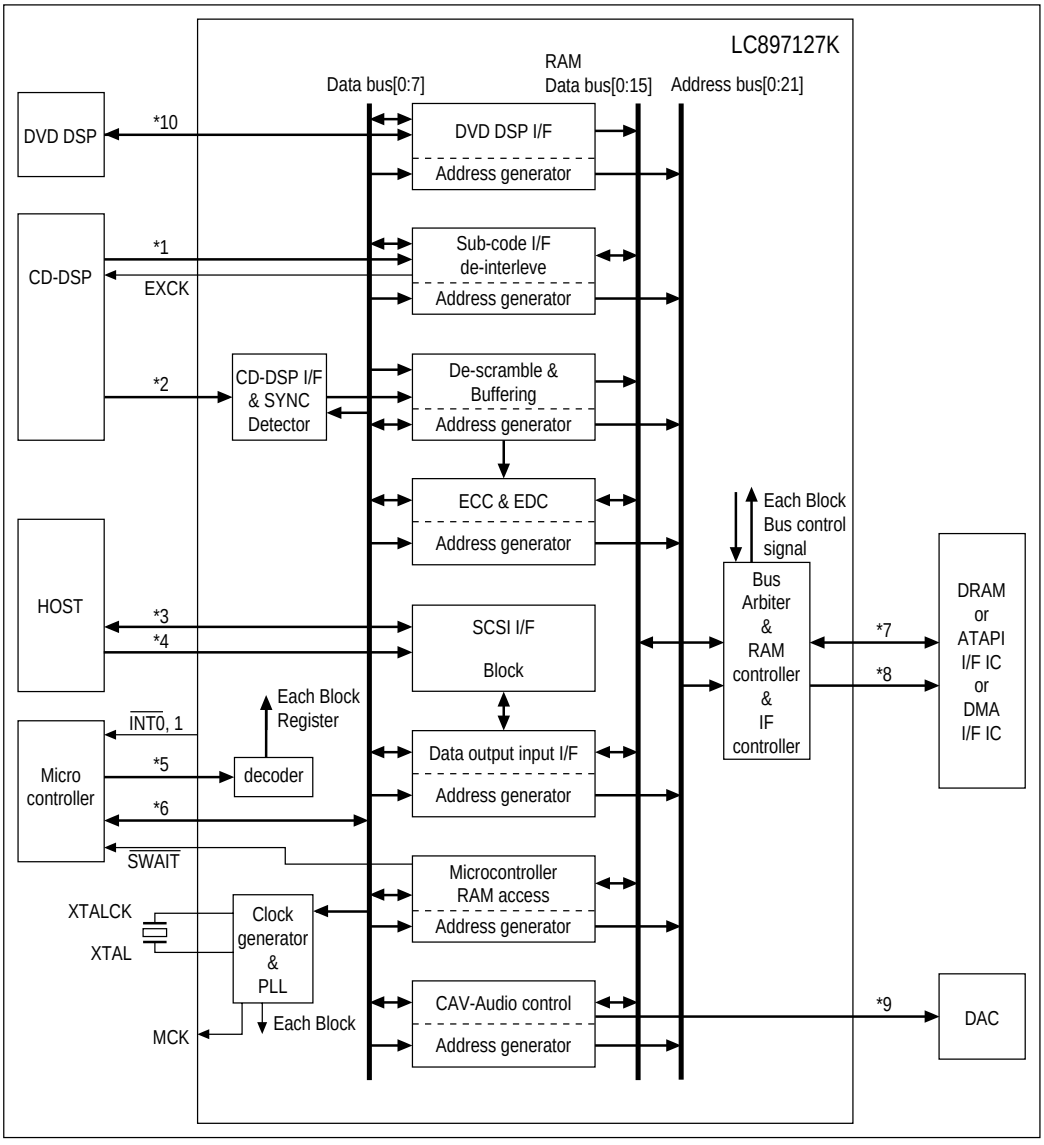
R3 = 7.5 kΩ, R4 = 200 Ω, R5 = 10k Ω, C3 = 0.1 µF

Note: The values listed above for R3, R4, R5, and C3 also apply when the XTALKC0 frequency is 33.8688 MHz.

Applications must be designed so that the analog V_{DD} and V_{SS} power supply system is completely independent of the logic system power supply and is not affected by the logic system power supply in any way.

Since the exact values of these components will vary depending on characteristics of the printed circuit board used and other factors, consult the manufacturer of the crystal element when designing the oscillator circuit.

Block Diagram



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*1. WFCK, SBSO, SCOR
*2. BCK, SDATA, LRCK, C2PO
*3. DB0 to DB7, DBP, BSY, MSG, SEL, RST, REQ, I/O, C/D
*4. ACK, ATN
*5. RD, WR, SUA0 to SUA6, CS, CSCTRL
*6. D0 to D7
*7. IO0 to IO15 (Data bus for both ATAPI and DMA interfaces)
*8. RA0 to RA10, RAS1, RAS0, OE, UWE, LWE
ATAPI interface: SBSO (DMARQ), DBCK (DMACK), DLRCK (DIOR), DSDATA (DIOW)
DMA interface: EXCK (DMARQ), C2PO (DMACK), SDATA (DIOR), BCK (DIOW)
*9. DBCK, DLRCK, DSDATA
*10. HDB7 to HDB0, DRESP, DREQ
See the circuit examples for details on ATAPI and DMA interface IC connection.

LC897127K Pin Functions

When the DVD Interface is Used

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

Pin No.	Pin	Type	Function
1	V_{SS0}	P	
2	IO2	B	Buffer RAM data I/O. These pins have built-in pull-up resistors.
3	IO1	B	
4	IO0	B	
5	MCK2SEL	I	PLL frequency selection. This pin must be connected to V_{DD}.
6	C2PO	I	CD DSP interface
7	SDATA	I	
8	BCK	I	
9	LRCK	I	
10	EXCK	O	Subcode I/O
11	WFCK	I	
12	SBSO	I	Subcode I/O
13	SCOR	I	
14	DSDATA	O	D/A converter outputs
15	DLRCK	O	
16	DBCK	O	
17	MCK	O	XTALCLK0 1/1, 1/2, and stop output
18	V_{DD}	P	
19	V_{SS0}	P	
20	$\overline{\text{RESET}}$	I	IC reset. The IC is reset on a low-level input.
21	CSCTRL	I	Microcontroller CS low/high
22	TEST3	I	Test pins. These pins must be connected to V_{SS0} in normal operation.
23	TEST0	I	
24	TEST1	I	
25	TEST2	I	
26	V_{SS0}	P	
27	XTALCK0	I	Crystal oscillator circuit input
28	XTAL0	O	Crystal oscillator circuit output
29	TEST4	I	Test pin. This pin must be connected to V_{SS0} in normal operation.
30	DRESP	B	DVD ECC data latching. A pull-down resistor is built in.
31	HDBDIR	O	DVD data bus direction output. A pull-down resistor is built in.
32	DREQ	B	DVD ECC data request. A pull-down resistor is built in.
33	V_{SS0}	P	
34	HDB7	I	DVD data input
35	HDB6	I	
36	V_{SS0}	P	
37	V_{DD}	P	
38	HDB5	I	DVD data input
39	HDB4	I	
40	HDB3	I	
41	HDB2	I	
42	HDB1	I	
43	HDB0	I	
44	V_{SS0}	P	
45	$\overline{\text{RD}}$	I	Microcontroller data read signal input
46	$\overline{\text{WR}}$	I	Microcontroller data write signal input
47	$\overline{\text{CS}}$	I	Register chip select input from the microcontroller
48	SUA0	I	Microcontroller register selection signals
49	SUA1	I	
50	SUA2	I	
51	SUA3	I	
52	SUA4	I	
53	SUA5	I	

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Pin No.	Pin	Type	Function
54	V_{DD}	P	
55	V_{SS0}	P	
56	SUA6	I	Microcontroller register selection signals
57	D0	B	Microcontroller data signals
58	D1	B	
59	D2	B	
60	D3	B	
61	D4	B	
62	D5	B	
63	V_{SS0}	P	
64	D6	B	Microcontroller data signals
65	D7	B	
66	$\overline{INT0}$	O	Interrupt request signal output to the microcontroller (ECC side. Set by setting a register value.)
67	$\overline{INT1}$	O	Interrupt request signal output to the microcontroller (SCSI side. Set by setting a register value.)
68	$\overline{SWAIT}$	O	Wait signal output to the microcontroller
69	X1EN	I	Used by the PLL. This pin must be connected to V_{DD} through a resistor.
70	XTALCK1	I	Used by the PLL.
71	XTAL1	O	Used by the PLL.
72	V_{SS0}	P	Analog V_{SS}
73	V_{DD}	P	Analog V_{DD}
74		NC	
75	I/O	B	SCSI interface
76	$\overline{REQ}$	B	
77	V_{SS1}	P	
78	C/D	B	SCSI interface
79	$\overline{SEL}$	B	
80		NC	
81	V_{DD}	P	
82	V_{SS1}	P	
83	$\overline{MSG}$	B	SCSI interface
84	$\overline{RST}$	B	
85	V_{SS1}	P	
86	$\overline{ACK}$	B	SCSI interface
87	$\overline{BSY}$	B	
88	V_{SS1}	P	
89	$\overline{ATN}$	B	SCSI interface
90	V_{DD}	P	
91	V_{SS1}	P	
92		NC	
93	$\overline{DBP}$	B	SCSI interface
94	V_{DD}	P	
95	$\overline{DB7}$	B	SCSI interface
96	$\overline{DB6}$	B	
97	V_{SS1}	P	
98	$\overline{DB5}$	B	SCSI interface
99	$\overline{DB4}$	B	
100	V_{DD}	P	
101	$\overline{DB3}$	B	SCSI interface
102	$\overline{DB2}$	B	
103	V_{SS1}	P	
104	$\overline{DB1}$	B	SCSI interface
105	$\overline{DB0}$	B	
106	SCSISEL	I	SCSI pin layout selection. (This pin must be connected to V_{SS0}.)
107	XTALSEL	I	PLL XATL oscillator selection

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Pin No.	Pin	Type	Function
108	V_{SS1}	P	
109	V_{DD}	P	
110	V_{SS0}	P	
111	$\overline{RAS0}$	O	Buffer RAM RAS signal output 0
112	DVDSEL	P	V_{SS0} selects the DVD interface and V_{DD} selects the I/O port function.
113	$\overline{CAS0}$	O	Buffer RAM CAS signal output 0 (Normally fixed at 0 (low).)
114	$\overline{CAS1}$	O	Buffer RAM CAS signal output 1
115	$\overline{OE}$	O	Buffer RAM output enable
116	$\overline{UWE(RA9)}$	O	Buffer RAM upper write enable (RA9 when 8M or more DRAM is used.)
117	$\overline{LWE}$	O	Buffer RAM lower write enable
118	V_{SS0}	P	
119	RA0	O	Buffer RAM address signal outputs
120	RA1	O	
121	RA2	O	
122	RA3	O	
123	RA4	O	
124	RA5	O	
125	RA6	O	
126	V_{DD}	P	
127	V_{SS0}	P	
128	RA7	O	Buffer RAM address signal outputs
129	RA8	O	
130	IO15	B	Buffer RAM data I/O. These pins have built-in pull-up resistors.
131	IO14	B	
132	IO13	B	
133	IO12	B	
134	IO11	B	
135	IO10	B	
136	IO9	B	
137	IO8	B	
138	V_{SS0}	P	
139	IO7	B	Buffer RAM data I/O. These pins have built-in pull-up resistors.
140	IO6	B	
141	IO5	B	
142	IO4	B	
143	IO3	B	
144	V_{DD}	P	

- Unused ("NC") pins must be left open.
- Pins whose name is under a bar operate with inverted (negative) logic.
- V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface driver ground.
- If DRAM is used, applications must adopt measures to prevent undershoot and other DRAM problems. Such measures include inserting resistors in the RAS and CAS lines and inserting capacitors between V_{SS} pins. See the article on Designing with the Latest Microcontrollers and Memory in special issue number 25 of Transistor Technology for details on these measures.
- Since this device includes buffers that sink a current of 48 mA, applications must take adequate noise prevention measures.

LC897127K Pin Functions

When ATAPI to SCSI Conversion is Used

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

Pin No.	Pin	Type	Function
1	V_{SS0}	P	
2	IO2	B	ATAPI data I/O. These pins have built-in pull-up resistors.
3	IO1	B	
4	IO0	B	
5	MCK2SEL	I	This pin must be connected to V_{DD}.
6	V_{SS0}	P	
7	V_{SS0}	P	
8	V_{SS0}	P	
9	V_{DD}	P	
10		NC	
11	V_{DD}	P	
12	DMARQ	I	ATAPI interface
13	V_{DD}	P	
14	DIOW	O	ATAPI interface
15	DIOR	O	
16	DMACK	O	
17	MCK	O	XTALCLK0 1/1, 1/2, and stop output
18	V_{DD}	P	
19	V_{SS0}	P	
20	$\overline{\text{RESET}}$	I	IC reset. The IC is reset on a low-level input.
21	CSCTRL	I	Microcontroller CS low/high
22	TEST3	I	Test pins. These pins must be connected to V_{SS0} in normal operation.
23	TEST0	I	
24	TEST1	I	
25	TEST2	I	
26	V_{SS0}	P	
27	XTALCK0	I	Crystal oscillator circuit input
28	XTAL0	O	Crystal oscillator circuit output
29	TEST4	I	Test pin. This pin must be connected to V_{SS0} in normal operation.
30	V_{SS0}	P	
31	V_{SS0}	P	
32	V_{SS0}	P	
33	V_{SS0}	P	
34	IOP7	I	General-purpose inputs These pins have built-in pull-up resistors.
35	IOP6	I	
36	V_{SS0}	P	
37	V_{DD}	P	
38	IOP5	I	General-purpose inputs These pins have built-in pull-up resistors.
39	IOP4	I	
40	IOP3	I	
41	IOP2	I	
42	IOP1	I	
43	IOP0	I	
44	V_{SS0}	P	
45	$\overline{\text{RD}}$	I	Microcontroller data read signal input
46	$\overline{\text{WR}}$	I	Microcontroller data write signal input
47	$\overline{\text{CS}}$	I	Register chip select input from the microcontroller
48	SUA0	I	Microcontroller register selection signals
49	SUA1	I	
50	SUA2	I	
51	SUA3	I	
52	SUA4	I	
53	SUA5	I	

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Pin No.	Pin	Type	Function
54	V_{DD}	P	
55	V_{SS0}	P	
56	SUA6	I	Microcontroller register selection signals
57	D0	B	Microcontroller data signals
58	D1	B	
59	D2	B	
60	D3	B	
61	D4	B	
62	D5	B	
63	V_{SS0}	P	
64	D6	B	Microcontroller data signals
65	D7	B	
66	$\overline{INT0}$	O	Interrupt request signal output to the microcontroller (ECC side. Set by setting a register value.)
67	$\overline{INT1}$	O	Interrupt request signal output to the microcontroller (SCSI side. Set by setting a register value.)
68	$\overline{SWAIT}$	O	Wait signal output to the microcontroller
69	X1EN	I	Used by the PLL. This pin must be connected to V_{DD} through a resistor.
70	XTALCK1	I	Used by the PLL.
71	XTAL1	O	Used by the PLL.
72	V_{SS0}	P	Analog V_{SS}
73	V_{DD}	P	Analog V_{DD}
74		NC	
75	I/O	B	SCSI interface
76	$\overline{REQ}$	B	
77	V_{SS1}	P	
78	C/D	B	SCSI interface
79	$\overline{SEL}$	B	
80		NC	
81	V_{DD}	P	
82	V_{SS1}	P	
83	$\overline{MSG}$	B	SCSI interface
84	$\overline{RST}$	B	
85	V_{SS1}	P	
86	$\overline{ACK}$	B	SCSI interface
87	$\overline{BSY}$	B	
88	V_{SS1}	P	
89	$\overline{ATN}$	B	SCSI interface
90	V_{DD}	P	
91	V_{SS1}	P	
92		NC	
93	$\overline{DBP}$	B	SCSI interface
94	V_{DD}	P	
95	$\overline{DB7}$	B	SCSI interface
96	$\overline{DB6}$	B	
97	V_{SS1}	P	
98	$\overline{DB5}$	B	SCSI interface
99	$\overline{DB4}$	B	
100	V_{DD}	P	
101	$\overline{DB3}$	B	SCSI interface
102	$\overline{DB2}$	B	
103	V_{SS1}	P	
104	$\overline{DB1}$	B	SCSI interface
105	$\overline{DB0}$	B	
106	SCSISEL	I	SCSI pin layout selection. (This pin must be connected to V_{SS0}.)
107	XTALSEL	I	PLL XATL oscillator selection

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Pin No.	Pin	Type	Function
108	V_{SS1}	P	
109	V_{DD}	P	
110	V_{SS0}	P	
111		NC	
112	V_{DD}	P	
113		NC	
114		NC	
115		NC	
116		NC	
117		NC	
118	V_{SS0}	P	
119		NC	
120		NC	
121		NC	
122		NC	
123		NC	
124		NC	
125		NC	
126	V_{DD}	P	
127	V_{SS0}	P	
128		NC	
129		NC	
130	IO15	B	
131	IO14	B	
132	IO13	B	
133	IO12	B	ATAPI data I/O These pins have built-in pull-up resistors.
134	IO11	B	
135	IO10	B	
136	IO9	B	
137	IO8	B	
138	V_{SS0}	P	
139	IO7	B	
140	IO6	B	
141	IO5	B	ATAPI data I/O These pins have built-in pull-up resistors.
142	IO4	B	
143	IO3	B	
144	V_{DD}	P	

- Unused ("NC") pins must be left open.
- Pins whose name is under a bar operate with inverted (negative) logic.
- V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface driver ground.
- Since this device includes buffers that sink a current of 48 mA, applications must take adequate noise prevention measures.

LC897127K Pin Functions

When DMA Interface to SCSI Conversion is Used

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

Pin No.	Pin	Type	Function
1	V_{SS0}	P	
2	IO2	B	DAM interface data I/O. These pins have built-in pull-up resistors.
3	IO1	B	
4	IO0	B	
5	MCK2SEL	I	This pin must be connected to V_{DD}.
6	DMACK	I	DMA interface functions
7	DIOR	I	
8	DIOW	I	
9	V_{DD}	P	
10	DMARQ	O	DMA interface functions
11	V_{DD}	P	
12	V_{DD}	P	
13	V_{DD}	P	
14		NC	
15		NC	
16		NC	
17	MCK	O	XTALCLK0 1/1, 1/2, and stop output
18	V_{DD}	P	
19	V_{SS0}	P	
20	$\overline{\text{RESET}}$	I	IC reset. The IC is reset on a low-level input.
21	CSCTRL	I	Microcontroller CS low/high
22	TEST3	I	Test pins. These pins must be connected to V_{SS0} in normal operation.
23	TEST0	I	
24	TEST1	I	
25	TEST2	I	
26	V_{SS0}	P	
27	XTALCK0	I	Crystal oscillator circuit input
28	XTAL0	O	Crystal oscillator circuit output
29	TEST4	I	Test pin. This pin must be connected to V_{SS0} in normal operation.
30	V_{SS0}	P	
31	V_{SS0}	P	
32	V_{SS0}	P	
33	V_{SS0}	P	
34	IOP7	I	General-purpose inputs These pins have built-in pull-up resistors.
35	IOP6	I	
36	V_{SS0}	P	
37	V_{DD}	P	
38	IOP5	I	General-purpose inputs These pins have built-in pull-up resistors.
39	IOP4	I	
40	IOP3	I	
41	IOP2	I	
42	IOP1	I	
43	IOP0	I	
44	V_{SS0}	P	
45	$\overline{\text{RD}}$	I	Microcontroller data read signal input
46	$\overline{\text{WR}}$	I	Microcontroller data write signal input
47	$\overline{\text{CS}}$	I	Register chip select input from the microcontroller
48	SUA0	I	Microcontroller register selection signals
49	SUA1	I	
50	SUA2	I	
51	SUA3	I	
52	SUA4	I	
53	SUA5	I	

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Pin No.	Pin	Type	Function
54	V_{DD}	P	
55	V_{SS0}	P	
56	SUA6	I	Microcontroller register selection signals
57	D0	B	Microcontroller data signals
58	D1	B	
59	D2	B	
60	D3	B	
61	D4	B	
62	D5	B	
63	V_{SS0}	P	
64	D6	B	Microcontroller data signals
65	D7	B	
66	$\overline{INT0}$	O	Interrupt request signal output to the microcontroller (ECC side. Set by setting a register value.)
67	$\overline{INT1}$	O	Interrupt request signal output to the microcontroller (SCSI side. Set by setting a register value.)
68	$\overline{SWAIT}$	O	Wait signal output to the microcontroller
69	X1EN	I	Used by the PLL. This pin must be connected to V_{DD} through a resistor.
70	XTALCK1	I	Used by the PLL.
71	XTAL1	O	Used by the PLL.
72	V_{SS0}	P	Analog V_{SS}
73	V_{DD}	P	Analog V_{DD}
74		NC	
75	I/O	B	SCSI interface
76	$\overline{REQ}$	B	
77	V_{SS1}	P	
78	C/D	B	SCSI interface
79	$\overline{SEL}$	B	
80		NC	
81	V_{DD}	P	
82	V_{SS1}	P	
83	$\overline{MSG}$	B	SCSI interface
84	$\overline{RST}$	B	
85	V_{SS1}	P	
86	$\overline{ACK}$	B	SCSI interface
87	$\overline{BSY}$	B	
88	V_{SS1}	P	
89	$\overline{ATN}$	B	SCSI interface
90	V_{DD}	P	
91	V_{SS1}	P	
92		NC	
93	$\overline{DBP}$	B	SCSI interface
94	V_{DD}	P	
95	$\overline{DB7}$	B	SCSI interface
96	$\overline{DB6}$	B	
97	V_{SS1}	P	
98	$\overline{DB5}$	B	SCSI interface
99	$\overline{DB4}$	B	
100	V_{DD}	P	
101	$\overline{DB3}$	B	SCSI interface
102	$\overline{DB2}$	B	
103	V_{SS1}	P	
104	$\overline{DB1}$	B	SCSI interface
105	$\overline{DB0}$	B	
106	SCSISEL	I	SCSI pin layout selection. (This pin must be connected to V_{SS0}.)
107	XTALSEL	I	PLL XATL oscillator selection

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Pin No.	Pin	Type	Function
108	V_{SS1}	P	
109	V_{DD}	P	
110	V_{SS0}	P	
111		NC	
112	V_{DD}	P	
113		NC	
114		NC	
115		NC	
116		NC	
117		NC	
118	V_{SS0}	P	
119		NC	
120		NC	
121		NC	
122		NC	
123		NC	
124		NC	
125		NC	
126	V_{DD}	P	
127	V_{SS0}	P	
128		NC	
129		NC	
130	IO15	B	DMA interface data I/O. These pins have built-in pull-up resistors.
131	IO14	B	
132	IO13	B	
133	IO12	B	
134	IO11	B	
135	IO10	B	
136	IO9	B	
137	IO8	B	
138	V_{SS0}	P	
139	IO7	B	ATAPI data I/O. These pins have built-in pull-up resistors.
140	IO6	B	
141	IO5	B	
142	IO4	B	
143	IO3	B	
144	V_{DD}	P	

- Unused ("NC") pins must be left open.
- Pins whose name is under a bar operate with inverted (negative) logic.
- V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface driver ground.
- Since this device includes buffers that sink a current of 48 mA, applications must take adequate noise prevention measures.