Ordering number : EN*4974

CMOS LSI

LC89201

9600-bps Facsimile Modem

Preliminary

Overview

The LC89201 is a CMOS single-chip, synchronous, half-duplex, 9600-bps fax modem designed for use with public telephone networks. Built in are such essential features for Group III facsimile systems as modulator, demodulator, transmission filters, and V.24 interface.

The LSI supports the V.29, V.27ter, V.21ch2, T.30, and T.4 telecommunications standards promulgated by the ITU-T (formerly the CCITT) for transmission at 9600, 7200, 4800, 2400 and 300 bps. Advanced signal processing provides reliable data transmissions even under adverse circuit conditions. Built-in High-level Data Link Control (HDLC) support permits the construction of Error Correction Mode (ECM) facsimile machines.

Features

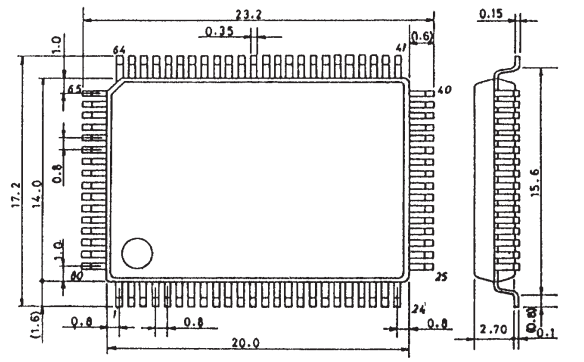
- Support for the following ITU-T standards: V.29 (9600, 7200 and 4800 bps), V.27ter (4800 and 2400 bps), V.21ch2 (300 bps), T.30, and T.4.
- Half-duplex operation.
- Group III facsimile support.
- Automatic switching between high- (V.29 and V.27ter) and low-speed (V.21ch2) incoming facsimiles.
- Short training (for ITU-T V.27ter only).
- HDLC framing and deframing (V.29, V.27ter, and V.21ch2).
- Tone generation and detection.
- Dual-tone multifrequency (DTMF) generation and detection.
- Call progress tone detection.
- Pseudo link back tone generation.
- Built-in automatic adaptive equalizer.
- Built-in fixed-amplitude amplifier.
  - — Link amplitude equalizer
  - — Cable amplitude equalizer
- Built-in transmission filters (digital filters).
- Programmable transmission level adjustment.
- Dynamic range for reception of 0 to –47 dBm.
- Programmable reception sensitivity adjustment.
- DTE interface.
  - — Serial interface (ITU-T V.24)
  - — Parallel interface (4 words × 8 bits, with built-in FIFO)
- Programmable interrupt generator.
- Built-in eye pattern generator.
- Adaptive differential pulse-code modulation (ADPCM).
- Caller ID detection.
- Built-in diagnostics.
- Energy-saving CMOS design (typ. 250 mW).
- Single 5 V power supply.
- 80-pin flat package (QIP-80E).

Package Dimensions

unit: mm

3174-QFP80E

[LC89201]



SANYO: QIP80E

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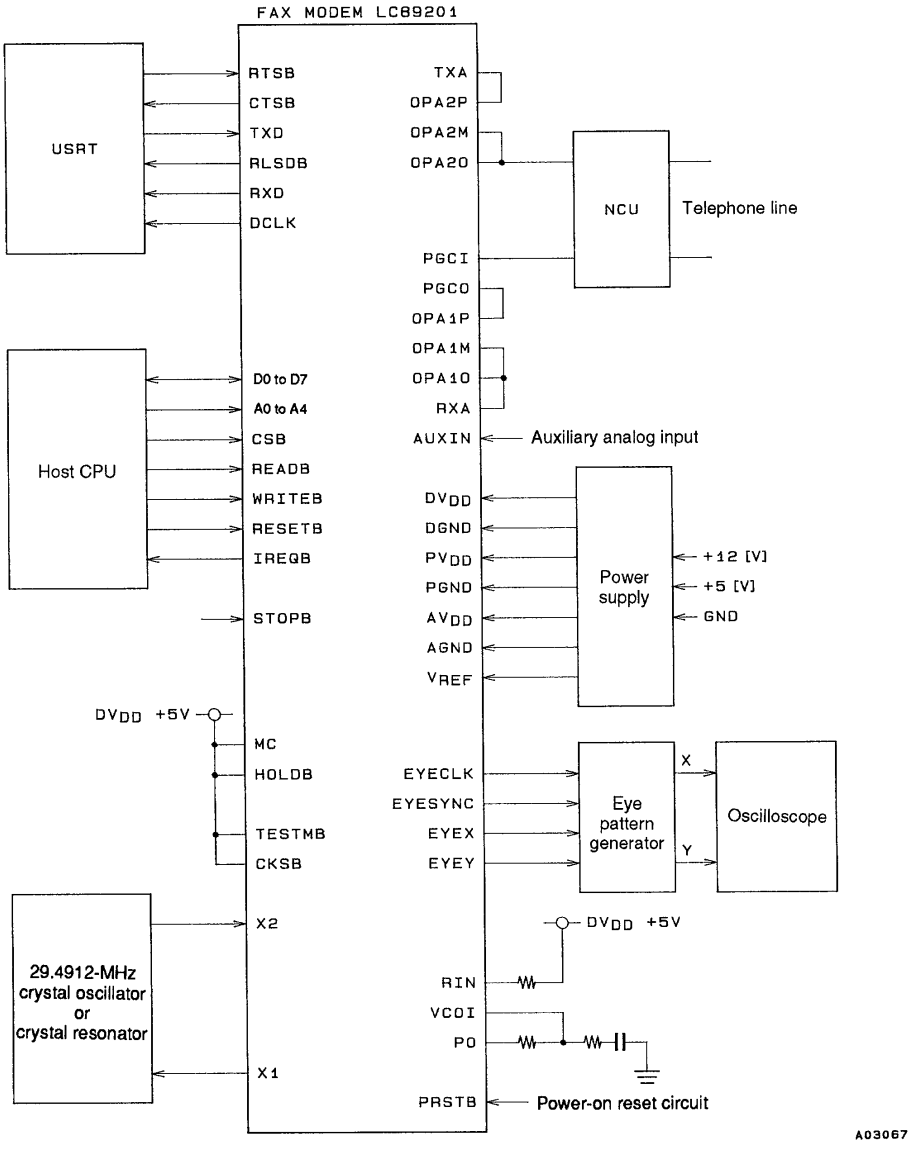
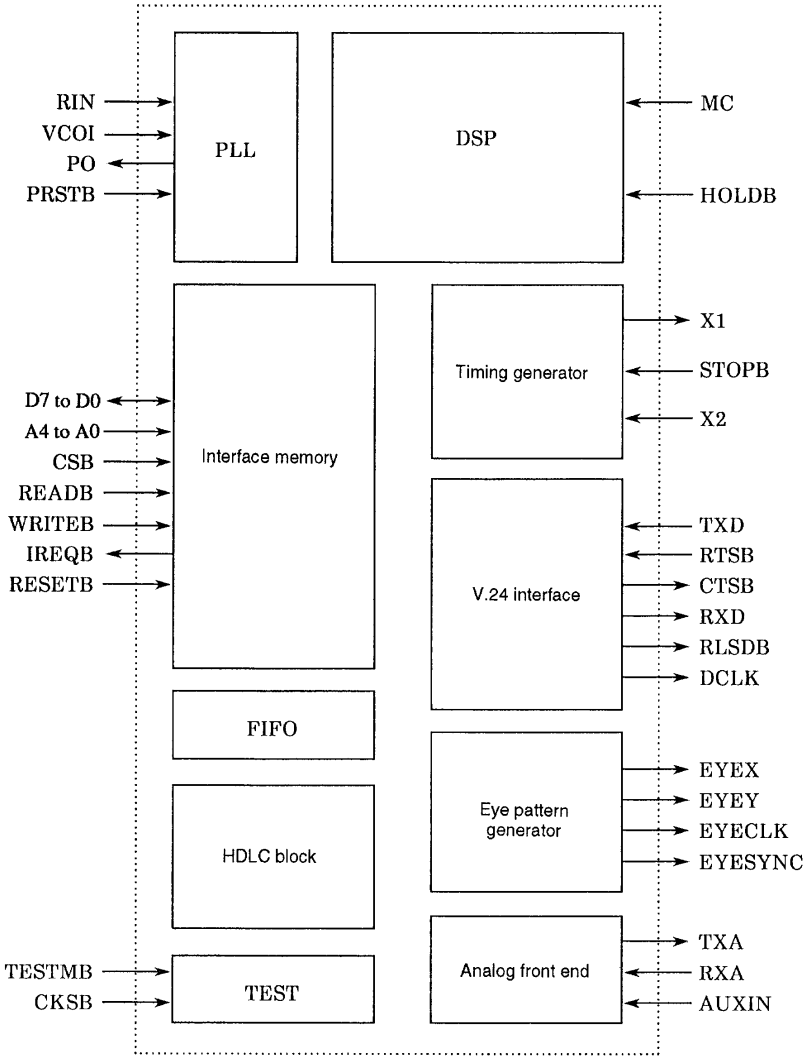
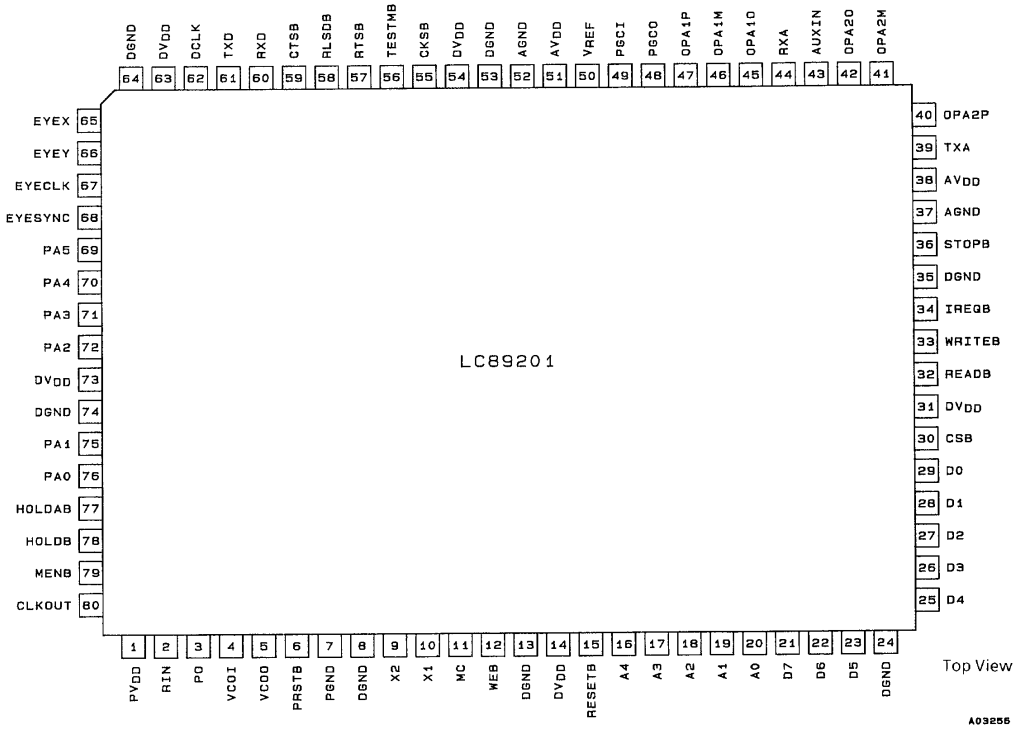
System Block Diagram



Internal Block Diagram



Pin Assignment



Pin Functions

1. Power Supply, Clock and Test Pins

Pin No.	Symbol	I/O	Function
14 31 54 63 73	DV_{DD}	P	Digital power supply
8 13 24 35 53 64 74	DGND	P	Digital ground
38 51	AV_{DD}	P	Analog power supply
37 52	AGND	P	Analog ground
1	PV_{DD}	P	Frequency multiplier PLL power supply
7	PGND	P	Frequency multiplier PLL ground
50	V_{REF}	P	Reference power supply. This must be half AV_{DD}.
9	X2	I	System clock input (29.4912 MHz)
10	X1	O	Oscillator amplifier output
80	CLKOUT	O	Output clock, one-quarter the frequency of the internal master clock (9.216 MHz).
56	TESTMB	I	Test pin. Connect to DV_{DD}.
55	CKSB	I	Test pin. Connect to DV_{DD}.

2. DTE Interface Pins

Pin No.	Symbol	I/O	Function
29 28 27 26 25 23 22 21	D0 D1 D2 D3 D4 D5 D6 D7	B	Data bus to host CPU
20 19 18 17 16	A0 A1 A2 A3 A4	I	Address bus to host CPU
30	CSB	I	Chip select signal
32	READB	I	Interface memory read signal
33	WRITEB	I	Interface memory write signal
34	IREQB	O	Interrupt request to host CPU
15	RESETB	I	System reset signal

3. Eye Pattern Interface Pins

Pin No.	Symbol	I/O	Function
67	EYECLK	O	Timing clock for generating eye pattern data. This may be used as the shift clock for an external shift register.
68	EYESYNC	O	Eye pattern synchronization signal
66 65	EYEX EYEY	O	Eye pattern data serial outputs (8 bits, MSB first)

4. V.24 (RS-232C) Interface Pins

Pin No.	Symbol	I/O	Function
57	RTSB	I	Request to send signal. The low level at this pin starts transmission; the high level suspends it.
59	CTSB	O	Clear to send signal. The low level at this pin signals the availability of data for transmission; the high level indicates that the data is invalid.
58	RLSDB	O	Received line signal data signal. The low level at this pin gives the timing for transferring the data received to the terminal.
61	TXD	I	Transmit data input
60	RXD	O	Receive data output
62	DCLK	O	Transmission data clock output

5. Analog Signal Pins

Pin No.	Symbol	I/O	Function
39	TXA	O	Transmitter analog output
44	RXA	I	Receiver analog input
43	AUXIN	I	Auxiliary analog input
40	OPA2P	I	Transmission buffer input/output pins. (For details, see circuit diagram.)
41	OPA2M	I	
42	OPA2O	O	
47	OPA1P	I	Reception buffer input/output pins (For details, see circuit diagram.)
46	OPA1M	I	
45	OPA1O	O	
49	PGCI	I	Reception gain adjustment circuit input. (For details, seecircuit diagram.)
48	PGCO	O	Reception gain adjustment circuit output.

6. System signal pins

Pin No.	Symbol	I/O	Function
11	MC	I	Program mode control signal. Connect to DV_{DD}.
78	HOLDB	I	System hold signal. Connect to DV_{DD}.
77	HOLDAB	O	System hold confirmation signal.
6	PRTSB	I	Frequency multiplier PLL reset input. (For details, see circuit diagram.)
3	PO	O	Phase comparator output. (For details, see circuit diagram.)
4	VCOI	I	Voltage-controlled oscillator input. (For details, seecircuit diagram.)
5	VCOO	O	Voltage-controlled oscillator output
2	RIN	I	Voltage-controlled oscillator adjustment input. (For details, see circuit diagram.)
36	STOPB	I	Oscillator amplifier STOP input

Note: All other pins are to be left unconnected.

Specifications

Absolute Maximum Ratings at DGND, AGND, PGND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	DV_{DD} max	Ta = 25°C	–0.3 to +7.0	V
	AV_{DD} max	Ta = 25°C	–0.3 to +7.0	V
	PV_{DD} max	Ta = 25°C	–0.3 to +7.0	V
I/O voltages	V_I V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	400	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering heat resistance		Hand soldering (3 seconds)	350	°C
		Reflow (10 seconds)	235	°C

Allowable Operating Ranges at Ta = –30 to +70°C, DGND, AGND, PGND = 0 V

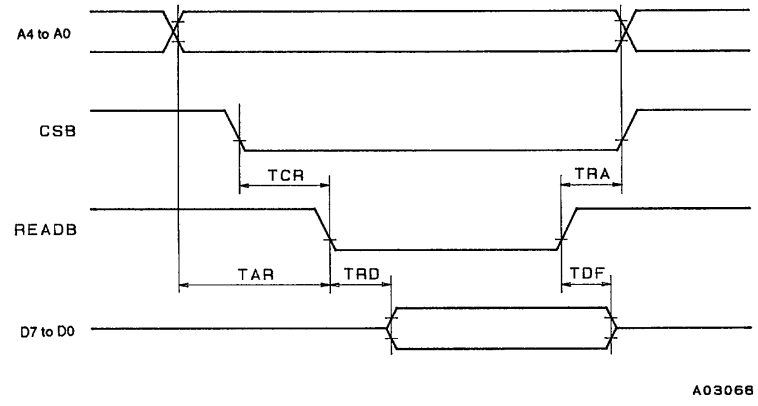
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	DV_{DD}		4.5	5.0	5.5	V
	AV_{DD}		4.5	5.0	5.5	V
	PV_{DD}		4.5	5.0	5.5	V
Input voltage	V_{IN}		0		V_{DD}	V

Electrical Characteristics at Ta = –30 to +70°C, DGND, AGND, PGND = 0 V, DV_{DD}, AV_{DD}, PV_{DD} = 4.5 to 5.5 V

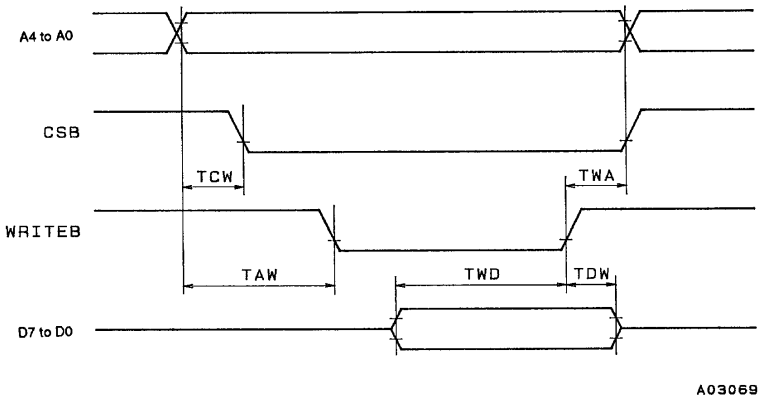
Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V_{IH}	TTL levels: RESETB, PRSTB, STOPB, A0 to A4, D0 to D7, CSB, READB, WRITEB, RTSB, TXD, HOLDB, MC, TESTMB, CKSB	2.2			V
Input low level voltage	V_{IL}				0.8	V
Input leak current	I_L	V_{IN} = DGND, AGND, PGND, DV_{DD}, AV_{DD}, PV_{DD}: RESETB, PRSTB, STOPB, A0 to A4, D0 to D7, CSB, READB, WRITEB, RTSB, TXD, HOLDB, MC, TESTMB, CKSB	–1		+1	µA
Output high level voltage	V_{OH}	I_{OH} = –3 mA, TTL levels: WEB, MENB, CLKOUT, HOLDAB, PA0 to PA5, D0 to D7, IREQB, CTSB, RLSDB, RXD, DCLK, VCOO, EYEX, EYEY, EYECLK, EYESYNC	2.4			V
Output low level voltage	V_{OL}	I_{OL} = 3 mA, TTL levels: WEB, MENB, CLKOUT, HOLDAB, PA0 to PA5, D0 to D7, IREQB, CTSB, RLSDB, RXD, DCLK, VCOO, EYEX, EYEY, EYECLK, EYESYNC			0.4	V
Output leak current	I_{OZ}	For high-impedance output: D0 to D7	–10	+10		µA
Oscillator frequency	f_{OSC}	X2, X1		29.4912		MHz
V_{REF} input voltage	V_{REF}	V_{REF}		V_{DD}/2		V
V_{REF} impedance	R_{REF}	V_{REF}	1			MΩ
Input voltage range	V_{IA}	RIN, VCOI, OPA1M, OPA1P, RAX, OPA2M, OPA2P, PGCI	V_{DD}*0.2		V_{DD}*0.8	V
Output voltage range	V_{OA}	TXA, PGCO, OPA1O, OPA2O	V_{DD}*0.2		V_{DD}*0.8	V
Output impedance	R_O	TXA, PGCO, OPA1O, OPA2O			7	kΩ
Current drain	I_{DD}	V_{DD} = 5.5 V			80	mA
		V_{DD} = 5.0 V		50		mA

AC Characteristics

1. DTE interface timing

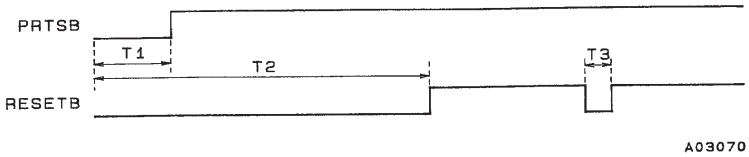


Read cycle timing



Parameter	Symbol	Conditions	min	typ	max	Unit
Address stabilization time (relative to READB signal)	TAR		15			ns
Chip select stabilization time (relative to READB signal)	TCR		0			ns
Data propagation delay	TRD				30	ns
Data float propagation delay	TDF		10			ns
Address hold time (relative to READB signal)	TRA		10			ns
Address stabilization time (relative to WRITEB signal)	TAW		15			ns
Chip select stabilization time (relative to WRITEB signal)	TCW		0			ns
Data setup time	TDW		20			ns
Data hold time	TWD		5			ns
Address hold time (relative to WRITEB signal)	TWA		10			ns

2. Reset timing



Parameter	Symbol	Conditions	min	typ	max	Unit
PRTSB pulse width	T1		500			µs
PRTSB propagation delay relative to RESETB	T2		5			ms
RESETB pulse width	T3		500			ns

Caption

P.2

1. Host CPU
2. 29.4912-MHz crystal oscillator or crystal resonator
3. Telephone line
4. Power supply
5. Auxiliary analog input
6. Eye pattern generator
7. Oscilloscope
8. Power-on reset circuit

P.3

1. Interface memory
2. Timing generator
3. V.24 interface
4. Eye pattern generator
5. HDLC block
6. Analog front end

New P2/8

2. 29.4912-MHz crystal oscillator or crystal resonator
8. Power-on reset circuit

D0 to D7

A0 to A4

P3/8

D7 to D0

A4 to A0

P.7/8

A4 to A0
D7 to D0
A4 to A0
D7 to D0