Ordering number : EN*5543

CMOS LSI

LC89051V

Digital Audio Interface Receiver

Preliminary

Overview

The LC89051V is for use in IEC958 format data transmission between digital audio equipment. This LSI is used on the receiving side, and handles synchronization with the input signal and demodulation of that signal to a normal format signal.

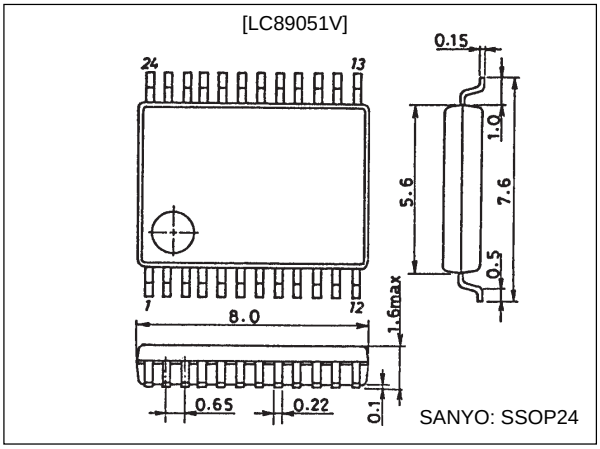
Features

- On-chip PLL circuit synchronizes with the transmitted IEC958 format signal.
- Low-voltage operation (3.3 V)
- Provides 128fs, bit, and L/R clock outputs.
- System clock can be selected to be either 384fs or 512fs.
- Microcontroller interface code settings for different output types
  - — Input pin, emphasis output, input bi-phase data output, and validity flag output settings
  - — Audio data output format setting
  - — Channel status output (32-bit output for consumer products)
  - — Subcode Q output with CRC flags (80 bits)
  - — Start ID and shortening (skip) ID detection for DAT with subcodes
- The built-in VCO can receive at speeds up to twice fs only when operating from a 5-V power supply.
- Miniature package: SSOP-24

Package Dimensions

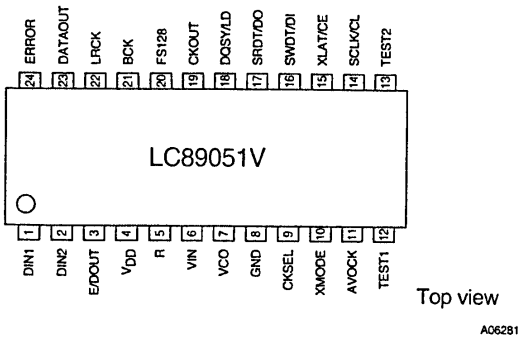
unit: mm

3175A-SSOP24



SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

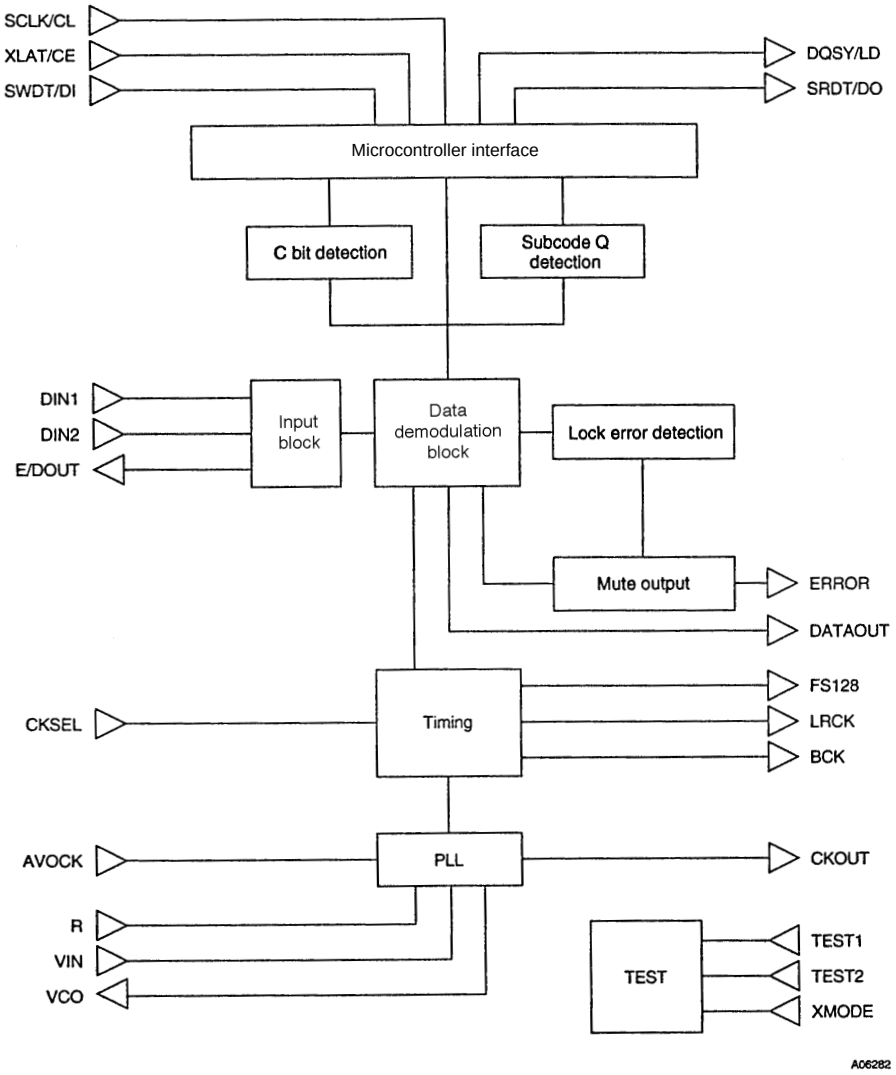
Pin Assignment



Pin Functions

Pin No.	Symbol	I/O	Description
1	DIN1	I	Data input with built-in amplifier (for coaxial or optical module input)
2	DIN2	I	Data input (for optical module input)
3	E/DOUT	O	Emphasis, input bi-phase, and validity flag output
4	V_{DD}	–	Power supply
5	R	I	VCO gain control input
6	VIN	I	VCO free-running setting input
7	VCO	O	PLL low-pass filter setting
8	GND	–	Ground
9	CKSEL	I	System clock selection input (384fs or 512fs)
10	XMODE	I	Reset input
11	AVOCK	I	PLL error lock avoidance clock input
12	TEST1	I	Test input (Must be connected to ground in normal operation)
13	TEST2	I	Test input (Must be connected to ground in normal operation)
14	SCLK/CL	I	Microcontroller interface clock input
15	XLAT/CE	I	Microcontroller interface latch/chip enable input
16	SWDT/DI	I	Microcontroller interface write data input
17	SRDT/DO	O	Microcontroller interface read data output
18	DQSY/LD	O	Microcontroller interface subcode Q and ID synchronization output
19	CKOUT	O	VCO clock output (free running, 384fs, or 512fs)
20	FS128	O	128fs clock output
21	BCK	O	Bit clock output
22	LRCK	O	L/R clock output (left channel = high, right channel = low)
23	DATAOUT	O	Audio data output
24	ERROR	O	PLL lock error mute output

Block Diagram



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
I/O voltages	V_I, V_O		–0.3 to V_{DD} + 0.3	V
I/O current	I_I, I_O		±20	mA
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		3.0	5.0	5.5	V
				(3.3)		
Operating temperature	T_{OPR}		–30		+75	C°

Electrical Characteristics

DC Characteristics (1) at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	$V_{IH}1$	*1	0.7 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}1$	*1	–0.3		0.3 V_{DD}	V
Input high-level voltage	$V_{IH}2$	*2	0.8 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}2$	*2	–0.3		0.2 V_{DD}	V
Input high-level voltage	$V_{IH}3$	*3	2.5		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}3$	*3	–0.3		+0.6	V
Output high-level voltage	V_{OH}	I_{OH} = –4 mA	V_{DD} – 2.1			V
Output low-level voltage	V_{OL}	I_{OL}= 4 mA			0.4	V
Current drain	I_{DD}	*4			20	mA
Input amplitude	Vpp	*5	0.4		V_{DD} + 0.3	V

Note: 1. Applies to the CKSEL, AVOCK, TEST1, and TEST2 pins. CMOS levels.
2. Applies to the XMODE, SCLK/CL, XLAT/CE, SWDT/DI pins. CMOS Schmitt inputs.
3. Applies to the DIN2 pin. TTL Schmitt levels.
4. V_{DD} = 5.0 V, Ta = 25°C, input data fs = 96 kHz
5. Measured before the DIN1 pin input capacitor.

DC Characteristics (2) at Ta = –30 to +75°C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	$V_{IH}1$	*6	0.7 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}1$	*6	–0.3		0.2 V_{DD}	V
Input high-level voltage	$V_{IH}2$	*7	0.75 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}2$	*7	–0.3		0.15 V_{DD}	V
Input high-level voltage	$V_{IH}3$	*8	2.4		V_{DD} + 0.3	V
Input low-level voltage	$V_{IL}3$	*8	–0.3		+0.3	V
Output high-level voltage	V_{OH}	I_{OH} = –2 mA	V_{DD} – 0.8			V
Output low-level voltage	V_{OL}	I_{OL}= 2 mA			0.4	V
Current drain	I_{DD}	*9			10	mA
Input amplitude	Vpp	*10	0.4		V_{DD} + 0.3	V

Note: 6. Applies to the CKSEL, AVOCK, TEST1, and TEST2 pins. CMOS levels.
7. Applies to the XMODE, SCLK/CL, XLAT/CE, SWDT/DI pins. CMOS Schmitt inputs.
8. Applies to the DIN2 pin. TTL Schmitt levels.
9. V_{DD} = 3.3 V, Ta = 25°C, input data fs = 48 kHz
10. Measured before the DIN1 pin input capacitor.

AC Characteristics (Normal Mode) at Ta = –30 to +75°C, V_{DD} = 3.0 to 5.5 V

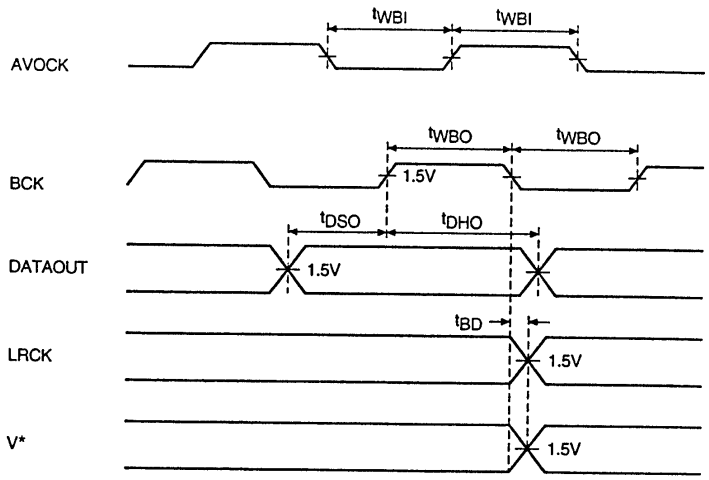
Parameter	Symbol	Conditions	min	typ	max	Unit
AVOCK input pulse width	t_{WBI}		10			µs
VCO free-running frequency	f_{VCO}	*11			50	MHz
		*12			75	MHz
BCK output pulse width	t_{WBO}	fs = 48 kHz	160			ns
Output data setup time	t_{DSO}		80			ns
Output data hold time	t_{DHO}		80			ns
Output delay	t_{BD}		–10	0	+10	ns

Note: 11. Ta = 25°C, V_{DD} = 3.3 V, with the circuit constants for standard speed operation in the sample application circuit.
12. Ta = 25°C, V_{DD} = 5.0 V, with the circuit constants for standard speed operation in the sample application circuit.

AC Characteristics (Double Speed Mode) at Ta = –30 to +75°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
AVOCK input pulse width	t_{WBI}		10			µs
VCO free-running frequency	f_{VCO}	*13			80	MHz
BCK output pulse width	t_{WBO}	fs = 96 kHz	80			ns
Output data setup time	t_{DSO}		40			ns
Output data hold time	t_{DHO}		40			ns
Output delay	t_{BD}		–10	0	+10	ns

Note: 13. Ta = 25°C, V_{DD} = 5.0 V, with the circuit constants for 2× speed operation in the sample application circuit.



Note: When the validity flag is output from the E/DOUT pin.

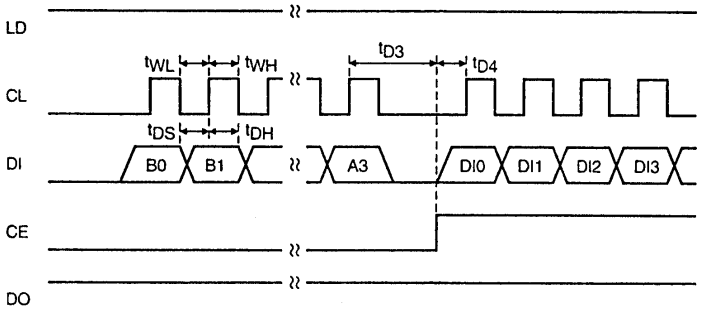
A06283

Microcontroller Interface Block AC Characteristics

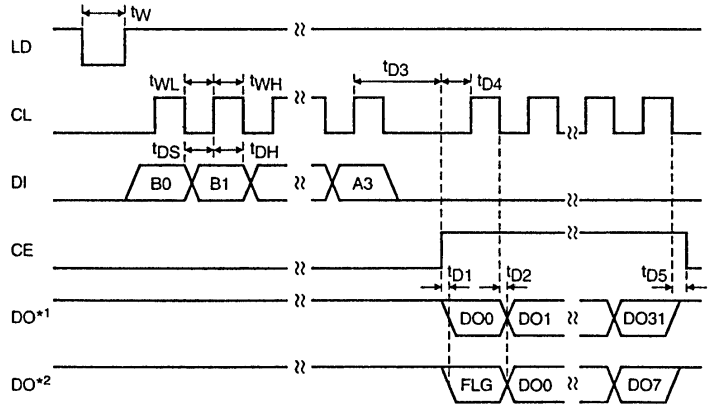
at Ta = –30 to +75°C, V_{DD} = 3.0 to 5.5 V (when CKSEL is low)

Parameter	Symbol	Conditions	min	typ	max	Unit
CL low pulse width	t_{WL}		100			ns
CL high pulse width	t_{WH}		100			ns
Data setup time	t_{DS}		50			ns
Data hold time	t_{DH}		50			ns
CE delay time	t_{D3}		1.0			µs
CL delay time	t_{D4}		50			ns
CE delay time	t_{D5}				100	ns
LD pulse width	t_W	fs = 44.1 kHz		136		µs
		fs = 88.2 kHz		68		µs
Data delay time	t_{D1}	C_L = 30 pF			100	ns
Data delay time	t_{D2}	C_L = 30 pF			100	ns

Input mode



Output mode



Note: 1. C bit output
2. Subcode Q output

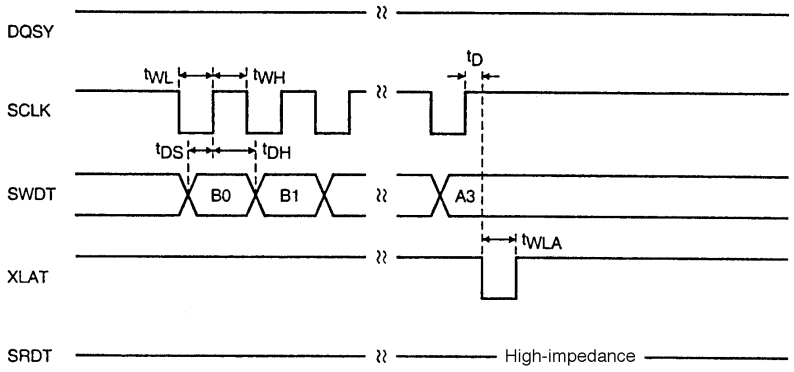
A06284

Microcontroller Interface Block AC Characteristics

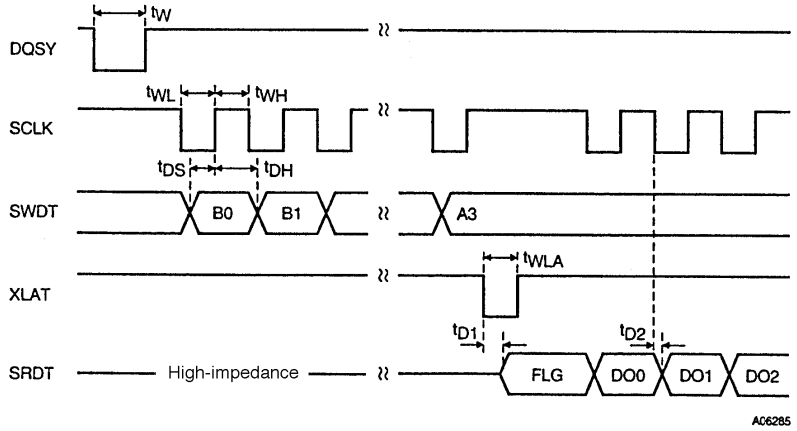
at Ta = –30 to +75°C, V_{DD} = 3.0 to 5.5 V (when CKSEL is high)

Parameter	Symbol	Conditions	min	typ	max	Unit
SCLK low pulse width	t_{WL}		100			ns
SCLK high pulse width	t_{WH}		100			ns
Setup time	t_{DS}		50			ns
Hold time	t_{DH}		50			ns
Delay time	t_D		100			µs
DQSY pulse width	t_W	fs = 44.1 kHz		136		µs
		fs = 88.2 kHz		68		µs
XLAT pulse width	t_{WLA}		100			ns
Data delay time	t_{D1}	C_L = 30 pF			100	ns
Data delay time	t_{D2}	C_L = 30 pF			100	ns

Input mode

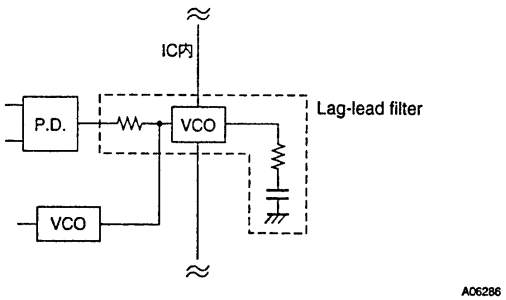


Output mode



Functions

1. Data Input and Output (DIN1, DIN2, E/DOUT)
   The DIN1 pin has a built-in amplifier, and can receive signals with an amplitude of about 400 mVp-p (coaxial input).
   The DIN2 pin is only for use in optical modules.
   Note that although the data input pins are controlled by the microcontroller, DIN1 can be selected when a microcontroller is not used. The microcontroller interface pins must be tied low in such applications.
   The E/DOUT normally outputs channel status information. However, it can be set to output either the input bi-phase data or the validity flag by command codes from the microcontroller.
2. PLL (R, VIN, VCO, AVOCK)
   This circuit includes a built-in VCO and supports sampling frequencies of 32, 44.1, and 48 kHz.
   This LSI can also receive at the 2× sampling frequencies of 64 kHz, 88.2 kHz, and 96 kHz, but only when operating from a 5-V power-supply voltage. However, the demodulated data and clock output during double speed reception follow the received sampling frequency, and the transmission format for 2×-speed data must follow the IEC958 standard.
   The built-in VCO is controlled by the resistors connected to the R and VIN pins.
   The resistor connected to R functions as both the VCO gain control and as temperature compensation. The VIN pin sets the VCO free-running frequency. Recommended circuit constants are shown in the sample application circuit.
   Note that the VCO free-running frequency varies with temperature and with manufacturing variations between samples. The recommended circuit constants shown in the sample application circuit take these variations into account so that the PLL circuit lockup characteristics are not adversely affected. These values are not designed to reduce variations in the free-running frequency. The VCO pin is the PLL loop filter pin. The loop filter is formed by attaching an external capacitor and a resistor to this pin. See the sample application circuit for these circuit constants.



PLL Loop Filter Structure

   The PLL circuit will be reset within a fixed period when PLL lock pull-in fails if a continuously operating clock of no more than 50 kHz is input to the AVOCK pin. This allows incorrect PLL operation to be avoided.

3. Clock Settings and Output (FS128, BCK, LRCK, DATAOUT, CKSEL, CKOUT)
   A 128fs clock signal is output from the FS128 pin. Figure 1 shows the output timing for the BCK, LRCK, and DATAOUT pins.
   The CKOUT clock output is set by the CKSEL pin as listed in the table below.

CKSEL	CKOUT
L	384fs clock output
H	512fs clock output

   The microcontroller interface format is also set by CKSEL as listed in the table below.

CKSEL	Microcontroller interface
L	Figure 2
H	Figure 3

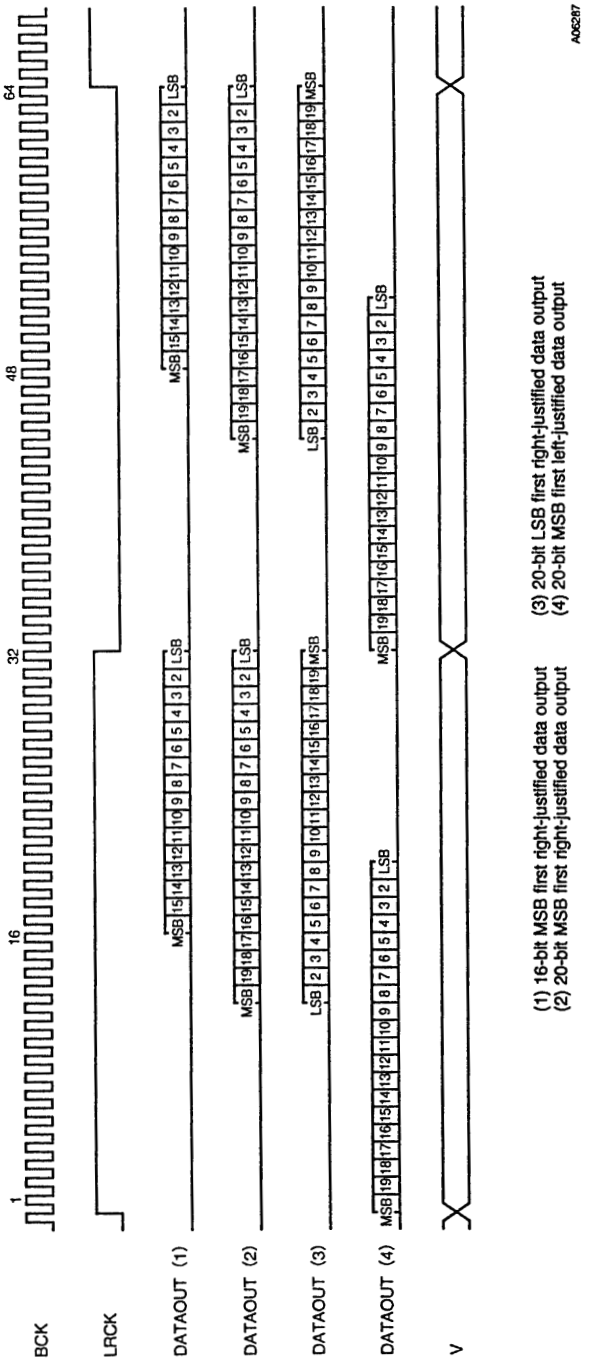
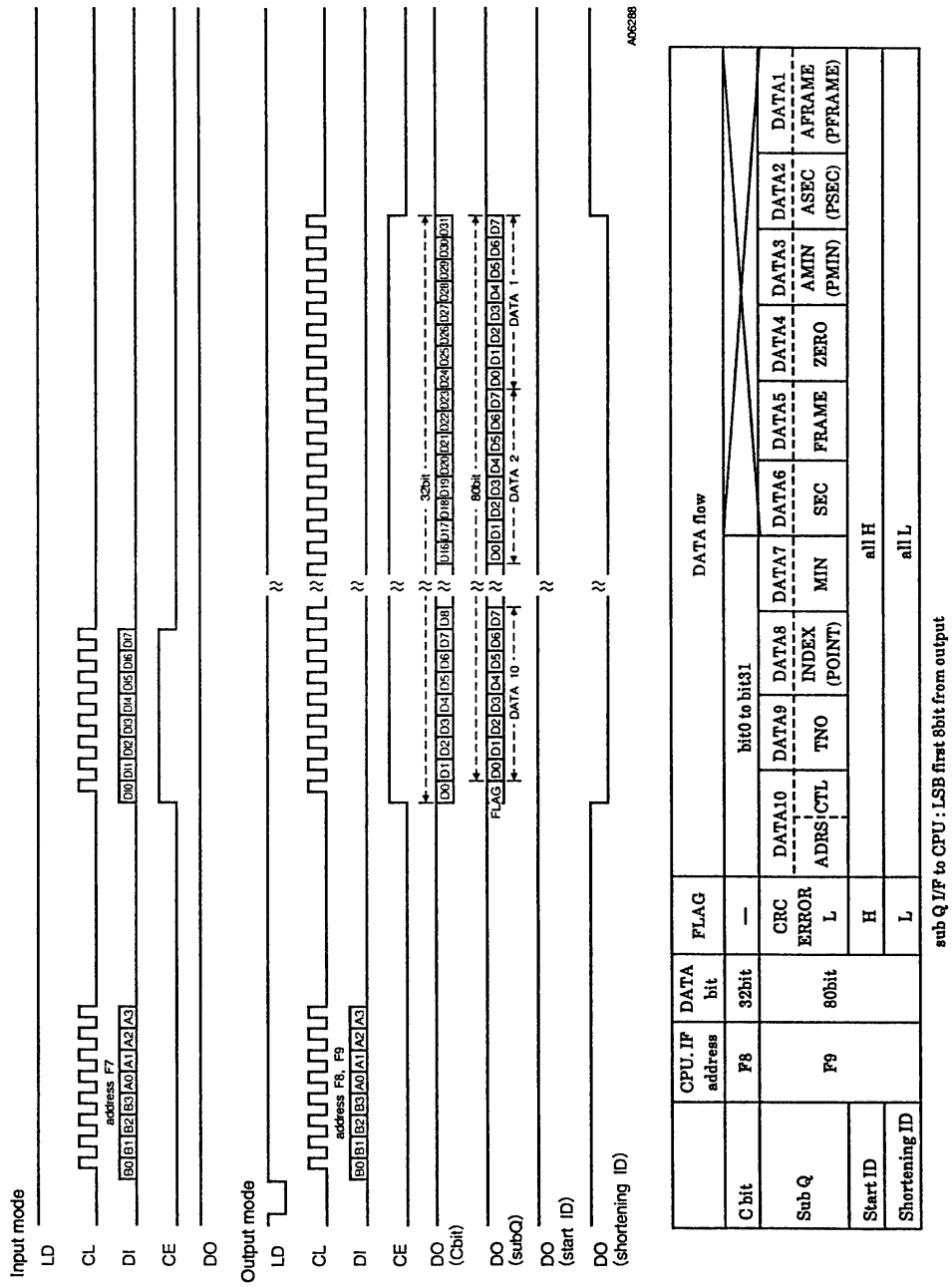


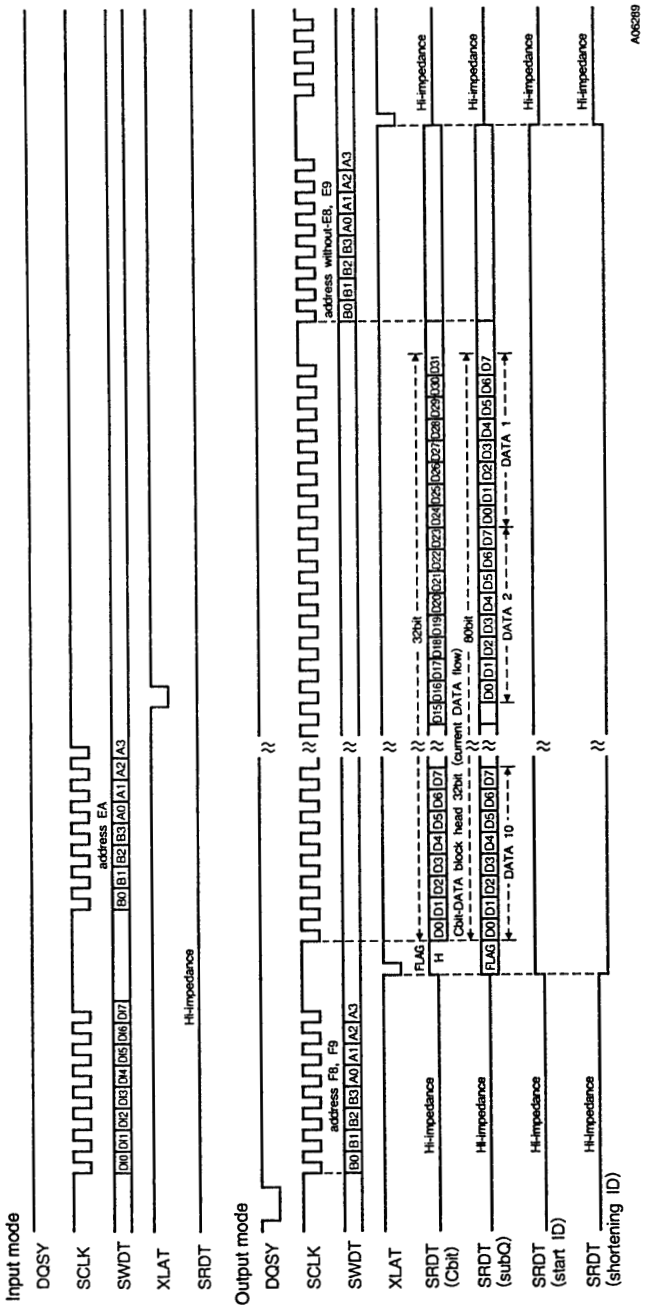
Figure 1 Data Output Timing



	CPU. IF address	DATA bit	FLAG	DATA flow										
C bit	F8	32bit	—	bit0 to bit31										
Sub Q	F9	80bit	CRC ERROR L	DATA10 ADRS CTL	DATA9 TNO	DATA8 INDEX (POINT)	DATA7 MIN	DATA6 SEC	DATA5 FRAME	DATA4 ZERO	DATA3 AMIN (PMIN)	DATA2 ASEC (PSEC)	DATA1 AFRAME (PFRAME)
Start ID			H	all H										
Shortening ID			L	all L										

sub Q I/F to CPU : LSB first 8bit from output

Figure 2 Microcontroller Interface Timing 1



	CPU. IF address	DATA bit	FLAG	DATA flow									
C bit	E9	32bit	H constant	bit0 to bit31									
Sub Q	E8	80bit	CRC ERROR L	DATA10 ADRS/CTL	DATA9 TNO	DATA8 INDEX (POINT)	DATA7 MIN	DATA6 SEC	DATA5 FRAME	DATA4 ZERO	DATA3 AMIN (PMIN)	DATA2 ASEC (PSEC)	DATA1 AFRAME (PFRAME)
Start ID			H	all H									
Shortening ID			L	all L									

sub Q I/F to CPU : LSB first 8bit from output

Figure 3 Microcontroller Interface Timing 2

Microcontroller Interface (SCLK/CL, XLAT/CE, SWDT/DI, SRDT/DO, DQSY/LD)

1. Data input and output addresses are allocated as follows:

Data input or output	Figure 2: Microcontroller Interface Timing 1									Figure 3: Microcontroller Interface Timing 2								
		B0	B1	B2	B3	A0	A1	A2	A3		B0	B1	B2	B3	A0	A1	A2	A3
Data input	F7	1	1	1	0	1	1	1	1	EA	0	1	0	1	0	1	1	1
C bit output	F8	0	0	0	1	1	1	1	1	E9	1	0	0	1	0	1	1	1
Subcode Q, ID output	F9	1	0	0	1	1	1	1	1	E8	0	0	0	1	0	1	1	1

2. The input command codes control the following setting:
   - System stop
   - Data input pin setting
   - Input bi-phase data output selection
   - Validity flag output selection
   - Audio data output format setting

   DI1: Stops VCO operation and thus stops the system.

DI1	L	H
System	Operating	Stopped

   DI2: Selects which input data to demodulate.

DI2	L	H
Data demodulation input	DIN1	DIN2

   DI3 and DI4: Select the E/DOUT pin output.

DI3	L		H	
DI4	L	H	L	H
E/DOUT	Emphasis data output	Validity flag output	DIN1 input data output	DIN2 input data output

   DI5 and DI6: Set the audio data output format.

DI5	L		H	
DI6	L	H	L	H
DATAOUT	16-bit right-justified MSB first	20-bit right-justified LSB first	20-bit right-justified MSB first	20-bit left-justified MSB first

   All bits are set low immediately after XMODE is switched from low to high. DI0 and DI7 are not used.

3. The following output settings can be controlled:
   - Channel status (C bit) output
   - Subcode Q data output
   - Start ID and shortening ID detection for DAT with subcodes

   C bit output
   - This IC only handles the first 32 bits.
   - The flag is fixed at the high level (only when CKSEL is high), and the data format is LSB first.
   - Error and update checking is not applied to the data.
   - The internal shift register is reset if a PLL lock error occurs.
   - Since the channel status information consists of 192 frames, a fixed period must be provided between data readout operations.

     $$\frac{1}{fs} \times 192 \text{ (ms)} < \text{(the interval between data readout operations)}$$

   Subcode Q output
   - Subcode Q can be read out after the fall of the DQSY/LD signal. Also note that the data is updated every time this signal falls. However, this signal will not be output (fall) unless 96-bit subcode Q data (including the CRC check bits) is input.
   - The flag outputs a high when the CRC check passes, and low if the CRC check fails. Besides, the shift clock SCLK is required to be input regardless of the CRC flag status after latch pulse input.
   - The bit order is LSB first within each byte of the 80 bits of subcode Q data.

   ID detection
   - The start ID and shortening ID are only detected when the DAT category code (1100000L) is received.
   - These IDs are detected as follows:
     — A low pulse is output from DQSY/LD if a start ID (R_0) or a shortening ID (L_1) is detected following a sync signal (L_0).
     — After this signal, data can be read out from SRDT/DO by inputting the same address value as that used for subcode Q data to SWDT/DI.

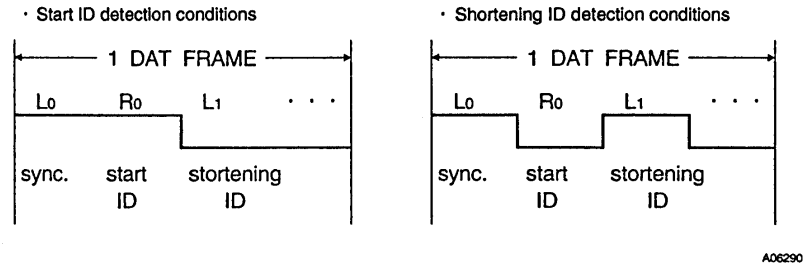


Figure 4 User Data for DAT with Subcodes

- The table below shows the relationship between the sync signal (L_0), the start ID (R_0), the shortening ID (L_1), and the data output.

(L_0): SYNC	H	H
(R_0): Start ID	H	L
(L_1): Shortening ID	L	H
Flags + 80 data bits	all H	all L
Detected ID	Start ID	Shortening ID

- Output pins
  The output scheme used for SRDT/DO differs depending on the microcontroller interface format selected by

CKSEL	Format	SRDT/DO
L	Figure 2	High open-drain output
H	Figure 3	Three-state output

Error (ERROR)

The ERROR pin goes high if there is an error in the input data or if the PLL is unlocked. It holds the high level for about 100 to 300 ms after data demodulation returns to normal and then goes low. The table below lists the data processing when an error has occurred.

Type of error	DATAOUT	C bit	Sub Q	ID	E/DOUT
Up to 8 consecutive parity errors	Previous data value	Output	Output	Output	Output
Over 8 consecutive parity errors	L	Output	Output	Output	Output
PLL lock error	L	L	L	L	L

System Reset (XMODE)

Normal system operation is started by setting XMODE high after the power supply has risen above at least 4.5 V (3.0 V). After power is applied, the system will be reset if a low level is applied once more to the XMODE pin. If XMODE is set low, the VCO free-running oscillator clock is output from CKOUT.

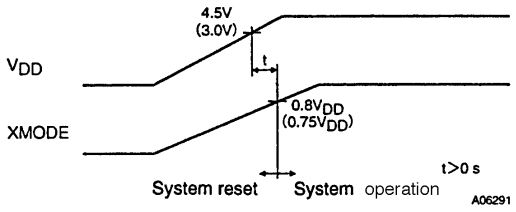
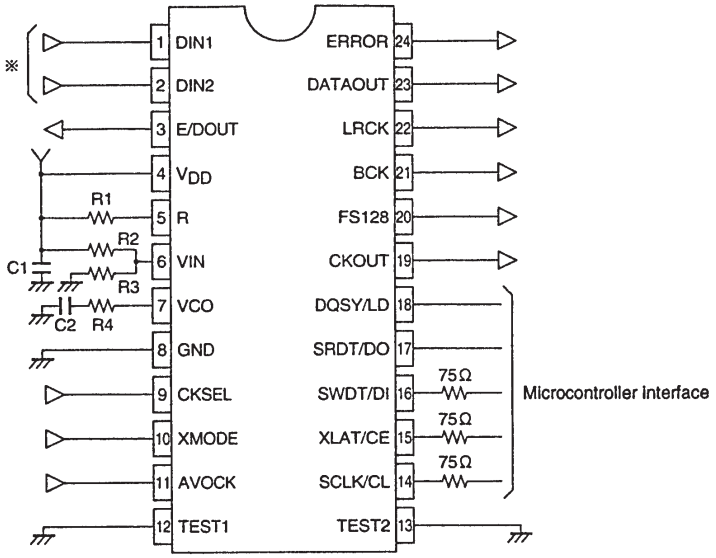
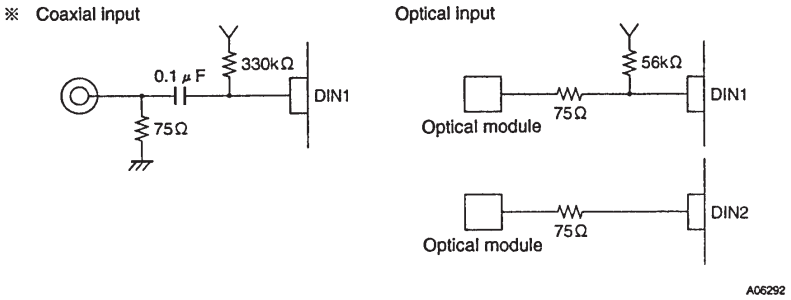


Figure 5 XMODE Pin Operation

Sample Application Circuit





Circuit constants

Item	Symbol	Value		
		5.0-V operation		3.3-V operation
		Standard speed	2× speed	Standard speed
Resistors	R1	24 kΩ	24 kΩ	24 kΩ
	R2	5.1 kΩ	5.1 kΩ	5.1 kΩ
	R3	5.1 kΩ	12 kΩ	5.1 kΩ
	R4	150 Ω	150 Ω	150 Ω
Capacitors	C1	0.1μF	0.1μF	0.1μF
	C2	0.01 μF	0.01 μF	0.01 μF