



# LC89978M

## CCD Delay Line for Multi-System

### Overview

The LC89978M is a CCD delay line for multi television system that incorporates a comb filter to remove noise from the chrominance signal and a 1-H delay line for the luminance signal.

### Features

- 5-V single-voltage power supply
- Built-in  $4 \times$  PLL frequency multiplier circuit allows 4fsc operation from an fsc (3.58 MHz) input.
- Can be switched between the NTSC/M, PAL/GBI, and PAL/M formats by setting control pin values.
- Includes a built-in crosstalk exclusion comb filter for the chrominance signal that provides high-precision comb characteristics in an adjustment-free circuit.
- Peripheral circuits provided on chip for operation with a minimum of external components.
- Positive-phase signal input, positive-phase signal output (luminance signal)

### Functions

- CCD shift registers (for chrominance and luminance signals)
- Timing generator and clock driver for CCD
- Delay time selective circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamp circuit (luminance signal)
- Center bias circuit (chrominance signal)
- Sample-and-hold circuit
- $4 \times$  PLL frequency multiplier circuit
- 4fsc clock output circuit
- High voltage generator for CCD Reset Drain (RD).

### Specifications

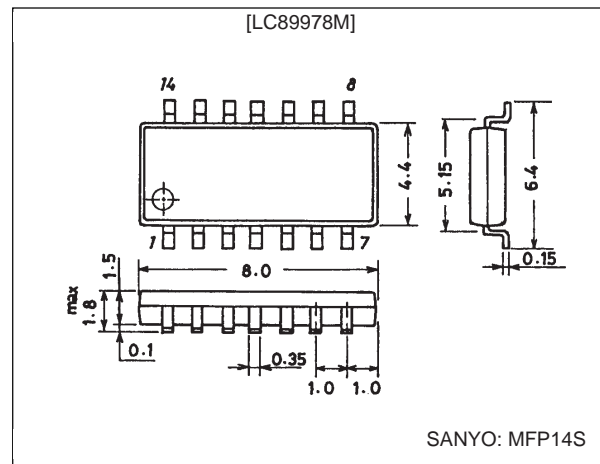
#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$		-0.3 to +6.0	V
Allowable power dissipation	$P_d \text{ max}$		250	mW
Operating temperature	$T_{opr}$		-10 to +60	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

### Package Dimensions

unit: mm

#### 3111-MFP14S

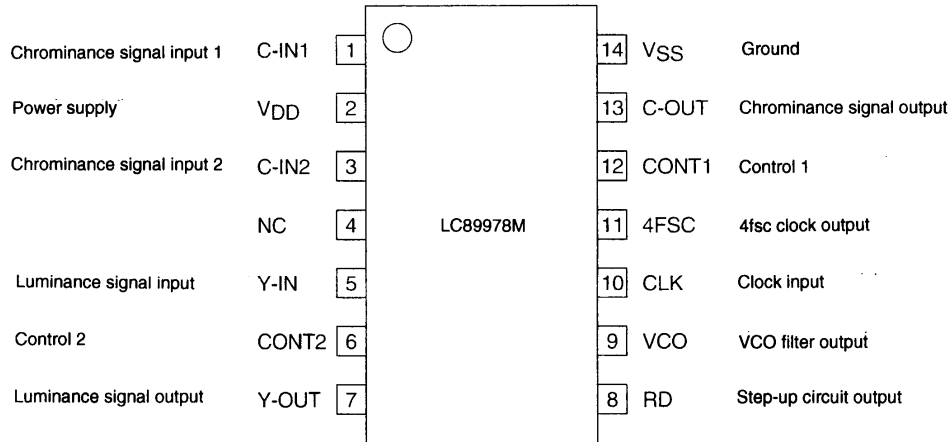


## LC89978M

### Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V <sub>DD</sub>		4.75	5.00	5.25	V
Clock input amplitude	V <sub>CLK</sub>		300	500	1000	mVp-p
Clock frequency	F <sub>CLK</sub>	Sine wave		3.579545		MHz
Chrominance signal input amplitude	V <sub>IN-C</sub>			350	500	mVp-p
Luminance signal input amplitude	V <sub>IN-Y</sub>			400	572	mVp-p

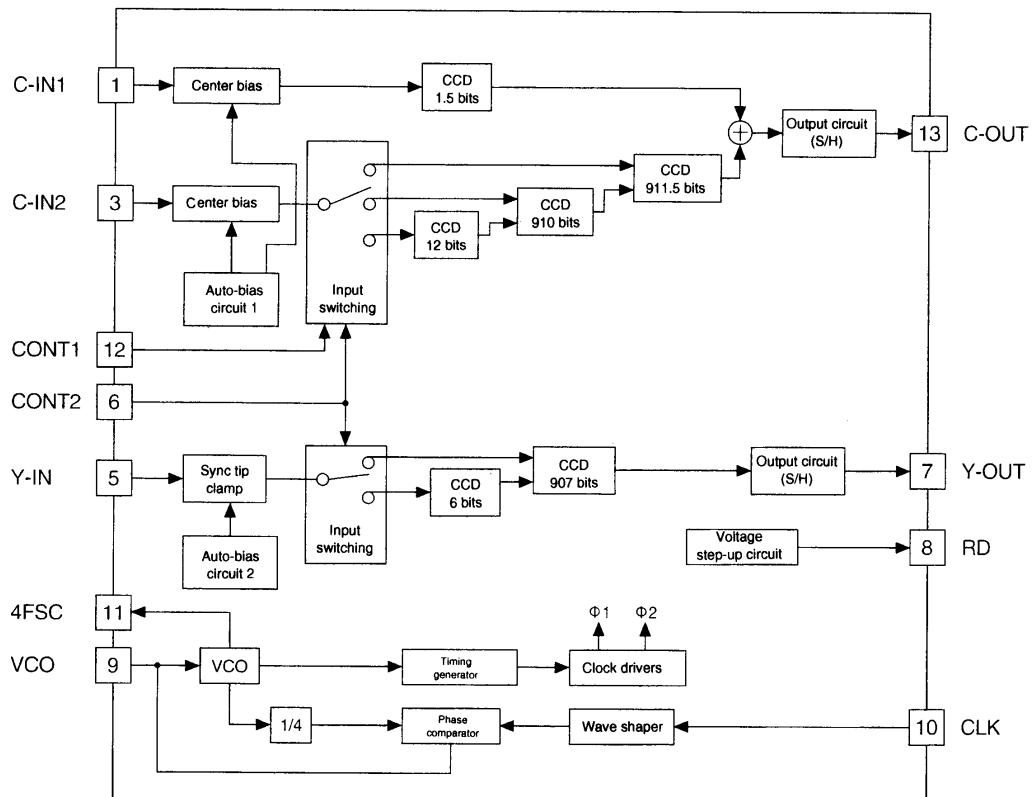
### Pin Assignment



Top view

A06305

### Block Diagram



A06306

## LC89978M

### Control Pin Functions

CONT1	CONT2	Mode (representative)	Chrominance signal delay (number of CCD stages)	Luminance signal delay (number of CCD stages)
Low	Low	PAL/GBI	2H (1833.5) + 0H (1.5)	1H (913)
Low	High	PAL/M	2H (1821.5) + 0H (1.5)	1H (907)
High	Low	—	—	—
High	High	NTSC/M	1H (911.5) + 0H (1.5)	1H (907)

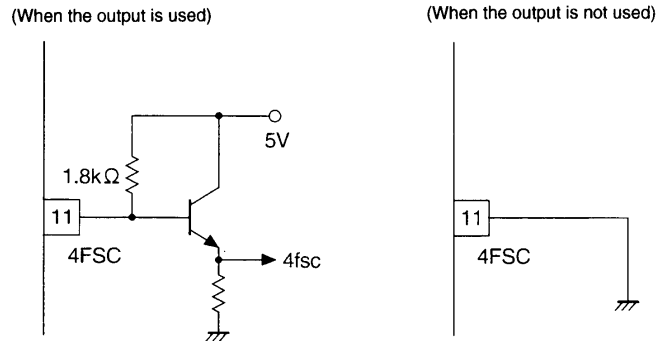
### Switching Voltage Levels

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Switching voltage level: low	$V_L$		-0.3	0.0	+0.5	V
Switching voltage level: high	$V_H$		2.0	5.0	6.0	V

Note: \*Since the control pins have built-in pull-down resistors (about 70 k $\Omega$ ), leaving these pins opens effectively sets them to the low level.

### Function of the 4FSC Pin

This pin provides a 4fsc clock signal generated by the 4  $\times$  PLL frequency multiplier circuit.



A06307

### Electrical Characteristics at $V_{DD} = 5.0$ V, $T_a = 25^\circ\text{C}$ , $F_{CLK} = 3.579545$ MHz, $V_{CLK} = 500$ mVp-p

Parameter	Symbol	Switch states					Ratings			Unit
		SW1	SW2	SW3	SW4	Test conditions	min	typ	max	
Supply current	$I_{DD-1}$	a	a	a	b	*1	31	36	41	mA
	$I_{DD-2}$	a	b	a	b	*1				
	$I_{DD-3}$	b	b	a	b	*1				
[Chrominance signal characteristics] (with no input to Y-IN)										
DC output voltage	$V_{INC-1}$	a	a	a	b	*2	1.9	2.4	2.9	V
	$V_{INC-2}$	a	b	a	b	*2				
	$V_{INC-3}$	b	b	a	b	*2				
	$V_{OUTC-1}$	a	a	a	b	*2	1.4	1.9	2.4	
	$V_{OUTC-2}$	a	b	a	b	*2				
	$V_{OUTC-3}$	b	b	a	b	*2				
Voltage gain	$G_{VC-1}$	a	a	a	b	*3	-2	0	+2	dB
	$G_{VC-2}$	a	b	a	b	*3				
	$G_{VC-3}$	b	b	a	b	*3				
Comb depth	$C_{D-1}$	a	a	a	b	*4	-40	-35	dB	
	$C_{D-2}$	a	b	a	b	*4				
	$C_{D-3}$	b	b	a	b	*4				
Linearity	$L_{NC-1}$	a	a	a	b	*5	-0.3	0.0	+0.3	dB
	$L_{NC-2}$	a	b	a	b	*5				
	$L_{NC-3}$	b	b	a	b	*5				
Clock leakage (4fsc)	$L_{CK4C-1}$	a	a	a	b	*6	10	50	mVrms	
	$L_{CK4C-2}$	a	b	a	b	*6				
	$L_{CK4C-3}$	b	b	a	b	*6				
Clock leakage (fsc)	$L_{CK1C-1}$	a	a	a	b	*6	0.5	1.5	mVrms	
	$L_{CK1C-2}$	a	b	a	b	*6				
	$L_{CK1C-3}$	b	b	a	b	*6				

Continued on next page.

LC89978M

Continued from preceding page.

Parameter	Symbol	Switch states					Ratings			Unit
		SW1	SW2	SW3	SW4	Test conditions	min	typ	max	
Noise	N <sub>C-1</sub>	a	a	a	b	*7		0.5	2.0	mVrms
	N <sub>C-2</sub>	a	b	a	b	*7				
	N <sub>C-3</sub>	b	b	a	b	*7				
Output impedance	Z <sub>OC-1</sub>	a	a	a	a, b	*8	200	350	500	Ω
	Z <sub>OC-2</sub>	a	b	a	a, b	*8				
	Z <sub>OC-3</sub>	b	b	a	a, b	*8				
0-H delay time	T <sub>DC-1</sub>	a	a	a	b	*9		160		ns
	T <sub>DC-2</sub>	a	b	a	b	*9				
	T <sub>DC-3</sub>	b	b	a	b	*9				
[Luminance signal characteristics] (With no signals input to C-IN1 and C-IN2)										
DC output voltage	V <sub>INY-1</sub>	a	a	a	b	*10	1.3	1.8	2.3	V
	V <sub>INY-2</sub>	a	b	a	b	*10				
	V <sub>INY-3</sub>	b	b	a	b	*10				
	V <sub>OUTY-1</sub>	a	a	a	b	*10	0.7	1.2	1.7	V
	V <sub>OUTY-2</sub>	a	b	a	b	*10				
	V <sub>OUTY-3</sub>	b	b	a	b	*10				
Voltage gain	G <sub>VY-1</sub>	a	a	a	b	*11	-2	0	+2	dB
	G <sub>VY-2</sub>	a	b	a	b	*11				
	G <sub>VY-3</sub>	b	b	a	b	*11				
Frequency response	G <sub>FY-1</sub>	a	a	b	b	*12	-2	0	+2	dB
	G <sub>FY-2</sub>	a	b	b	b	*12				
	G <sub>FY-3</sub>	b	b	b	b	*12				
Differential gain	D <sub>GY-1</sub>	a	a	a	b	*13	0	5	8	%
	D <sub>GY-2</sub>	a	b	a	b	*13				
	D <sub>GY-3</sub>	b	b	a	b	*13				
Differential phase	D <sub>PY-1</sub>	a	a	a	b	*13	0	5	8	deg
	D <sub>PY-2</sub>	a	b	a	b	*13				
	D <sub>PY-3</sub>	b	b	a	b	*13				
Linearity	L <sub>SY-1</sub>	a	a	a	b	*14	37	40	43	%
	L <sub>SY-2</sub>	a	b	a	b	*14				
	L <sub>SY-3</sub>	b	b	a	b	*14				
Clock leakage (4fsc)	L <sub>CK4Y-1</sub>	a	a	a	b	*15		10	50	mVrms
	L <sub>CK4Y-2</sub>	a	b	a	b	*15				
	L <sub>CK4Y-3</sub>	b	b	a	b	*15				
Clock leakage (fsc)	L <sub>CK1Y-1</sub>	a	a	a	b	*15		0.5	1.5	mVrms
	L <sub>CK1Y-2</sub>	a	b	a	b	*15				
	L <sub>CK1Y-3</sub>	b	b	a	b	*15				
Noise	N <sub>Y-1</sub>	a	a	a	b	*16		0.5	2.0	mVrms
	N <sub>Y-2</sub>	a	b	a	b	*16				
	N <sub>Y-3</sub>	b	b	a	b	*16				
Output impedance	Z <sub>OY-1</sub>	a	a	a	c, b	*17	250	400	550	Ω
	Z <sub>OY-2</sub>	a	b	a	c, b	*17				
	Z <sub>OY-3</sub>	b	b	a	c, b	*17				
Delay time	T <sub>DY-1</sub>	a	a	a	b	*18		63.81		μs
	T <sub>DY-2</sub>	a	b	a	b	*18		63.39		μs
	T <sub>DY-3</sub>	b	b	a	b	*18		63.39		μs

**Test Conditions**

1. The supply current with no input signal
2. The pin output voltage (the center bias voltage) with no input signal
3. Measure the C-OUT output when a 350-mVp-p sine wave is input to C-IN1 and C-IN2.

$$G_{VC} = 20 \log \frac{\text{C-OUT output [mVp-p]}}{350 \text{ [mVp-p]}} \text{ [dB]}$$

Test frequencies:

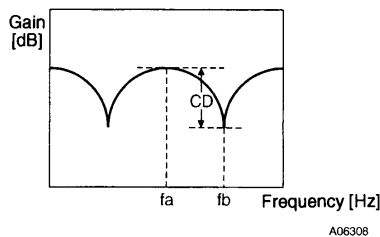
- $G_{VC-1}$ : 4.431395 MHz (PAL/GBI)
- $G_{VC-2}$ : 3.571628 MHz (PAL/M)
- $G_{VC-3}$ : 3.571628 MHz (NTSC/M)

4. Measure the comb depth from the C-OUT output when a 350-mVp-p sine wave with frequency  $f_a$  is input to C-IN1 and C-IN2, and when a sine wave of frequency  $f_b$  is input.

$$C_D = 20 \log \frac{\text{The C-OUT output for an } f_b \text{ input [mVp-p]}}{\text{The C-OUT output for an } f_a \text{ input [mVp-p]}} \text{ [dB]}$$

Test Frequencies

$f_a$	$f_b$
$C_{D-1}$ : 4.431395 MHz (PAL/GBI)	4.435303 (PAL/GBI)
$G_{D-2}$ : 3.571628 MHz (PAL/M)	3.575561 (PAL/M)
$G_{D-3}$ : 3.571628 MHz (NTSC/M)	3.563761 (NTSC/M)



5. Measure the C-OUT output when a 200-mVp-p sine wave is input to C-IN1 and C-IN2, and when a 500-mVp-p sine wave is input, and calculate the gain difference as follows:

$$L_{NC} = 20 \log \left( \frac{\text{The output for a 500-mVp-p input [mVp-p]}}{500 \text{ [mVp-p]}} \bigg/ \frac{\text{The output for a 200-mVp-p input [mVp-p]}}{200 \text{ [mVp-p]}} \right) \text{ [dB]}$$

Test Frequencies

- $L_{NC-1}$  4.431395MHz (PAL/GBI)
- $L_{NC-2}$  3.571628MHz (PAL/M)
- $L_{NC-3}$  3.571628MHz (NTSC/M)

6. Measure the 4fsc (14.3 MHz) and fsc (3.58 MHz) components in the C-OUT output with no input signal.
7. Measure the noise in the C-OUT output with no input signal.  
Measure the noise with a noise meter with a 200-kHz high-pass filter and a 5-MHz low-pass filter.
8. Input a 350-mVp-p sine wave to C-IN1 and C-IN2. Let V1 be the C-OUT output when SW3 is set to the 'a' position, and let V2 be the C-OUT output when SW3 is set to the 'b' position.

$$Z_{OC} = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [dB]}$$

Test Frequencies

- $Z_{OC-1}$ : 4.431395 MHz (PAL/GBI)
- $Z_{OC-2}$ : 3.571628 MHz (PAL/M)
- $Z_{OC-3}$ : 3.571628 MHz (NTSC/M)

9. The delay time in the C-OUT output with respect to the C-IN1 input. This is the CCD 1.5-bit delay.
10. The pin output voltage (clamp voltage) with no input signal.

11. Measure the Y-OUT output with a 200-kHz 400-mVp-p sine wave input to Y-IN.

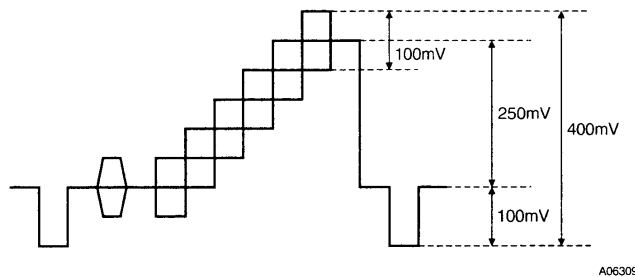
$$G_{VY} = 20 \log \frac{\text{Y-OUT output [mVp-p]}}{400 \text{ [mVp-p]}} \text{ [dB]}$$

12. Measure the Y-OUT output when a 200-kHz 200-mVp-p sine wave is input to Y-IN, and when a 3.5-MHz 200-mVp-p sine wave is input.

$$G_{FY} = 20 \log \frac{\text{The Y-OUT output for a 3.5-MHz input [mVp-p]}}{\text{The Y-OUT output for a 200-kHz input [mVp-p]}} \text{ [dB]}$$

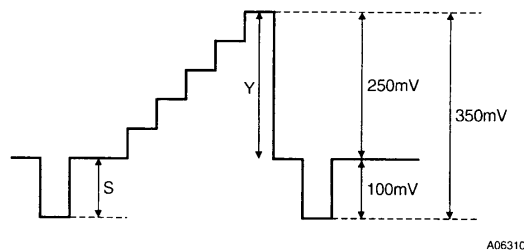
Here, adjust Vbias so that the clamp level is +250 mV.

13. Apply a 5-step staircase wave (as in the figure below) to Y-IN, and measure the differential gain and differential phase in the Y-OUT output using a vector scope.



14. Apply a 5-step staircase wave (as in the figure below) to Y-IN, and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.

$$L_S = \frac{S \text{ [mV]}}{Y \text{ [mV]}} \times 100 \text{ [%]}$$



15. Measure the 4fsc (14.3 MHz) and fsc (3.58 MHz) components in the Y-OUT output with no input signal.

16. Measure the noise in the Y-OUT output with no input signal.

Measure the noise with a noise meter with a 200-kHz low-pass filter, a 4.2-MHz low-pass filter, and a 3.58-MHz trap filter.

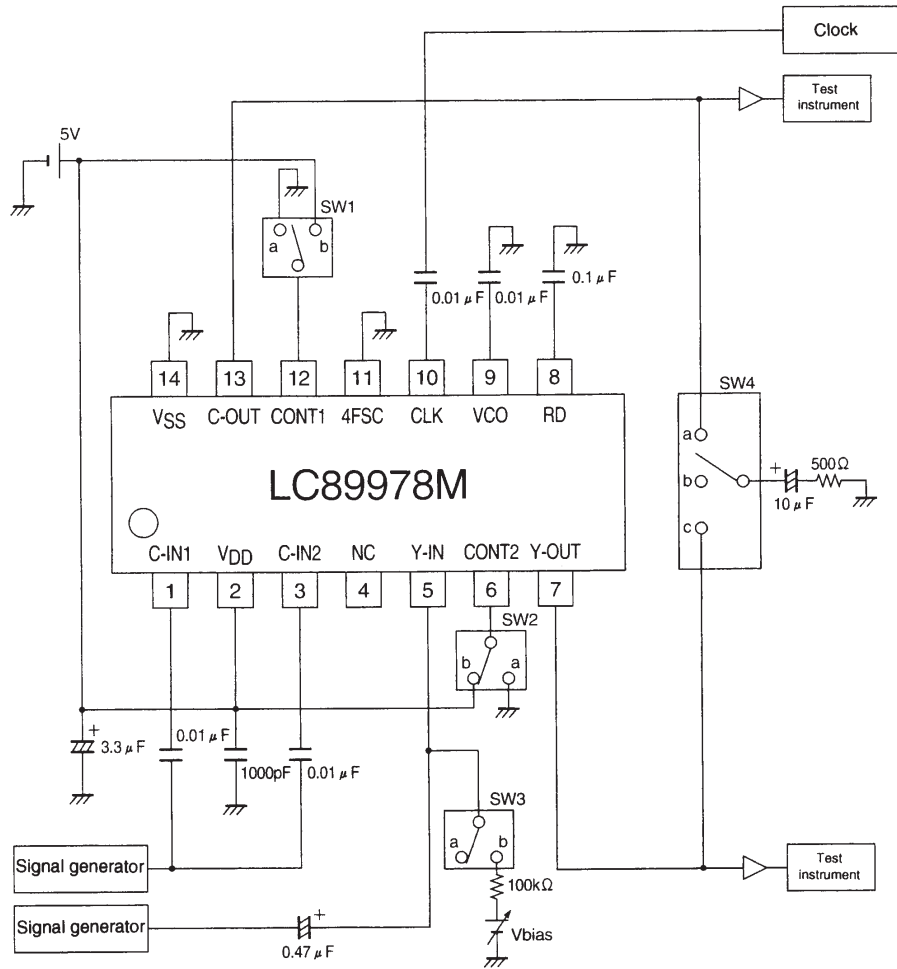
17. Input a 200-kHz, 400-mVp-p sine wave to Y-IN1. Let V1 be the V-OUT output when SW3 is set to the 'c' position, and let V2 be the Y-OUT output when SW3 is set to the 'b' position.

$$Z_{OY} = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [\Omega]}$$

18. Measure the delay time in the Y-OUT output with respect to the input to Y-IN.

## LC89978M

### Test Circuit



A06311

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of July, 1997. Specifications and information herein are subject to change without notice.