

Overview

The Sanyo LC8955 is a stereo/mono replay LSI for CD-I format ADPCM data. In addition to an ADPCM decoding circuit, the LC8955 also incorporates a DMA interface, buffer RAM interface and a D/A converter serial interface.

The LC8955 interfaces directly with the Sanyo LC8951 Real-time Error-correction and Host Interface Processor, allowing a CD-I replay system to be configured easily.

The LC8955 is designed to operate with a host microprocessor which sets the operating mode. It operates from a single 5V supply, and is available in 80-pin plastic QIPs.

Features

- Real-time ADPCM decoder LSI
- Direct interface to Sanyo's LC8951 error-correction LSI for high-speed data transfer
- Data transfer under program or DMA control
- Independent data and control busses in auto-request transfer
- 8K byte external static RAM interface
- Buffers up to 64 ADPCM sound groups in external RAM
- DAC interface circuit
- 80-pin plastic QIP

Functional Description

The LC8955 is divided into three major functional blocks.

ADPCM Input Block

The ADPCM input block has three data input modes, selected by setting internal registers.

① Auto-request transfer

Data is transferred automatically into the LC8955's data port without CPU intervention. A number of handshaking signals control data transfer. The input device can be an LC8951 Real-time Error-correction and Host Interface Processor or another CD-ROM output device.

② Program transfer

The CPU writes each byte of data directly into the LC8955 under program control. Data is transferred using the CPU data bus.

③ DMA transfer

Data is written into the LC8955 by an external DMA controller using the CPU data bus. Up to 64 ADPCM sound groups can be written to an external 8K byte buffer RAM. One sound group consists of 128 bytes of CD-I data.

The LC8955 then decodes data in the buffer without intervention from the CPU or DMA controller, leaving these devices free for other tasks.

Decoder Block

The decoder block converts the ADPCM data into 16-bit linear PCM data. Decoding parameters can either be set by the CPU, or read from subheader information in the ADPCM data stream.

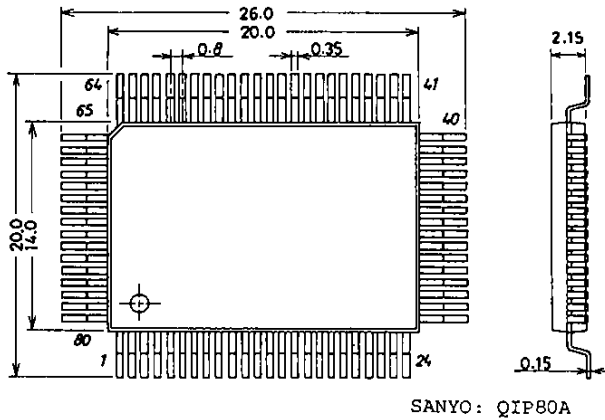
SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

8030JN,TA/3260YT/D119TA,TS (US) No.3215-1/4

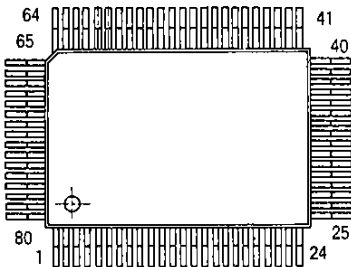
DAC Interface Block

Two output formats are available. The first is suitable for input to Sanyo's LC7883, 7883M DA converters, and the second is the standard CD-I format. The output circuit will also accept CD-DA format input data and, by setting an LC8955 internal register, switch it through to the output pins without processing.

Package Dimensions 3044B-Q80AIC
(unit: mm)



Pin Assignment



Type

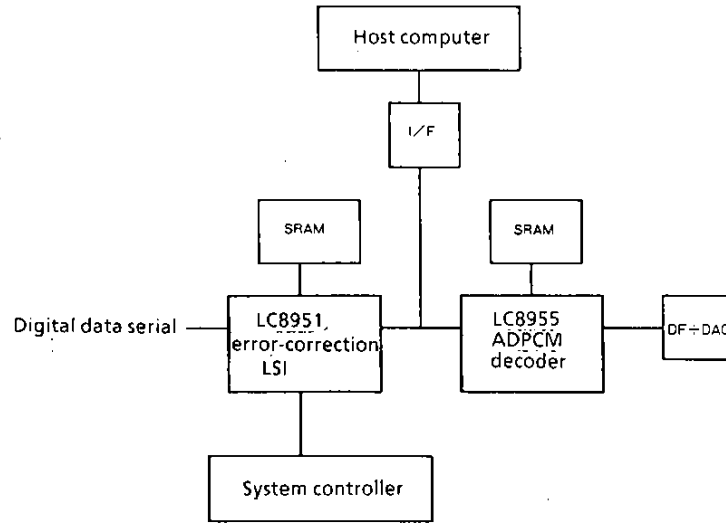
- I : Input pin
- O : Output pin
- B : Bidirectional pin
- P : Power supply pin
- NC : No connection

Note) All V_{DD} and V_{SS} pins should be connected to the positive supply or ground.

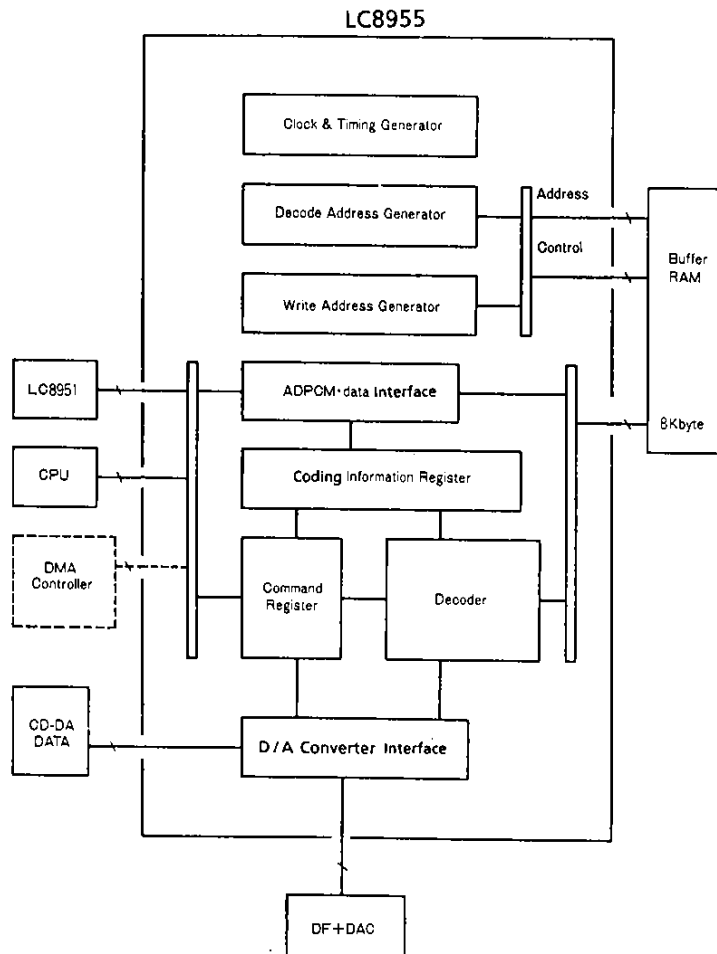
| No. | Pin Name | Type | No. | Pin Name | Type |
|-----|----------|------|-----|----------|------|
| 1 | T2 | I | 41 | WAITB | I |
| 2 | T1 | I | 42 | MCK | I |
| 3 | OUTSET | I | 43 | DTENB | I |
| 4 | Vss | P | 44 | EOPB | I |
| 5 | A12 | O | 45 | SD7 | B |
| 6 | A11 | O | 46 | SD6 | B |
| 7 | A10 | O | 47 | SD5 | B |
| 8 | A9 | O | 48 | SD4 | B |
| 9 | A8 | O | 49 | SD3 | B |
| 10 | A7 | O | 50 | SD2 | B |
| 11 | A6 | O | 51 | SD1 | B |
| 12 | A5 | O | 52 | Vss | P |
| 13 | Vss | P | 53 | SD0 | B |
| 14 | A4 | O | 54 | SA1 | I |
| 15 | A3 | O | 55 | SA0 | I |
| 16 | A2 | O | 56 | CSB | I |
| 17 | A1 | O | 57 | RDB | I |
| 18 | A0 | O | 58 | WRB | I |
| 19 | MWEB | O | 59 | BUSY | O |
| 20 | MCSB | O | 60 | BUFFULL | O |
| 21 | Vss | P | 61 | UNDFLOW | O |
| 22 | IO7 | B | 62 | DATAEMP | O |
| 23 | IO6 | B | 63 | MEMPHAS | O |
| 24 | IO5 | B | 64 | MBITSPL | O |
| 25 | IO4 | B | 65 | MSPLFRQ | O |
| 26 | IO3 | B | 66 | MSTEMON | O |
| 27 | IO2 | B | 67 | RESETB | I |
| 28 | IO1 | B | 68 | LRCLK | O |
| 29 | IO0 | B | 69 | WCLK | O |
| 30 | DD7 | I | 70 | DATA | O |
| 31 | VDD | P | 71 | BCLK | O |
| 32 | DD6 | I | 72 | CLRCLK | I |
| 33 | DD5 | I | 73 | VDD | P |
| 34 | DD4 | I | 74 | CWCLK | I |
| 35 | DD3 | I | 75 | CDATA | I |
| 36 | DD2 | I | 76 | CBCLK | I |
| 37 | DD1 | I | 77 | REQB | O |
| 38 | DD0 | I | 78 | DACKB | I |
| 39 | EFLAG | I | 79 | READYB | O |
| 40 | READB | O | 80 | DONEB | I |

LC8955

System Diagram



Block Diagram



Absolute Maximum Ratings at $V_{SS}=0V$

| Parameter | Symbol | Condition | Ratings | Unit |
|-----------------------------|---------------|------------------------------|----------------------|------------|
| Maximum Supply Voltage | $V_{DD\ max}$ | $T_a=25^\circ C$ | -0.3 to +7.0 | V |
| Input/Output Voltage | V_I, V_O | $T_a=25^\circ C$ | -0.3 to $V_{DD}+0.3$ | V |
| Allowable Power Dissipation | $P_d\ max$ | $T_a \leq 70^\circ C$ | 350 | mW |
| Operating Temperature | T_{opr} | | -30 to +70 | $^\circ C$ |
| Storage Temperature | T_{stg} | | -55 to +125 | $^\circ C$ |
| Solder Temperature | | 10sec., dipping of pins only | 260 | $^\circ C$ |

Allowable Operating Conditions at $T_a = -30$ to $+70^\circ C, V_{SS}=0V$

| Parameter | Symbol | Ratings | | | Unit |
|---------------------|----------|---------|-----|----------|------|
| | | min | typ | max | |
| Supply Voltage | V_{DD} | 4.5 | 5.0 | 5.5 | V |
| Input Voltage Range | V_{IN} | 0 | | V_{DD} | V |

DC Characteristics at $V_{SS}=0V, V_{DD}=4.5$ to $5.5V, T_a = -30$ to $+70^\circ C$

| Parameter | Symbol | Applicable Pins | Condition | Ratings | | | Unit |
|--------------------------|-----------|--|------------------------|---------|-----|-----|-----------|
| | | | | min | typ | max | |
| Input 'H'-Level Voltage | V_{IH1} | All input pins except RESETB, EOPB, IO7 to 0, SD7 to 0 | | 2.2 | | | V |
| Input 'L'-Level Voltage | V_{IL1} | | | | | 0.8 | V |
| Input 'H'-Level Voltage | V_{IH2} | RESETB, EOPB, IO7 to 0, SD7 to 0 | | 2.5 | | | V |
| Input 'L'-Level Voltage | V_{IL2} | | | | | 0.6 | V |
| Output 'H'-Level Voltage | V_{OH} | All output pins | $I_{OH} = -3mA$ | 2.4 | | | V |
| Output 'L'-Level Voltage | V_{OL} | | $I_{OL} = 3mA$ | | | 0.4 | V |
| Input Leakage Current | I_L | All input pins | $V_I = V_{SS}, V_{DD}$ | -25 | | 25 | μA |
| Pull-up Resistor | R_{UP} | 100 to 7, SD0 to 7 | | 10 | 20 | 40 | $k\Omega$ |

■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:

- ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
- ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.