Ordering number: EN※3982

CMOS LSI

No. ※3982

LC89582

ATIP Decoder for CD-WO and CD-MO Recorders

Preliminary

Overview

The LC89582 is an Absolute Time In Pre-groove (ATIP) decoder IC for use with CD-WO and CD-MO discs complying with the Orange Book specifications. It decodes ATIP data from the disc wobble signal, performs data interpolation and parity checking and then outputs the data to the host CPU. In addition, it controls the spindle motor drive, using the wobble signal as the control input.

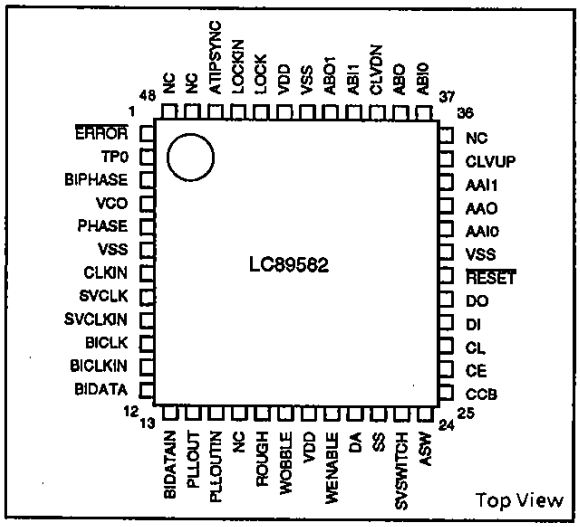
The LC89582 comprises an ATIP decoder circuit, a C²B serial interface, a timing generator, a constant linear velocity (CLV) servocontroller, two analog switches and an adjustment-free digital PLL. Optionally, the LC89582 can use an external, analog PLL if different PLL characteristics are required.

The LC89582 operates from a 5 V supply and is available in 48-pin QIPs.

Features

- ATIP data decoded from wobble signal
- ATIP sync detector output
- Data interpolator
- Parity detector
- C²B serial interface to host CPU
- Constant linear velocity servocontroller
- Adjustment-free digital PLL
- Low-power CMOS process
- 5 V supply
- 48-pin QIP

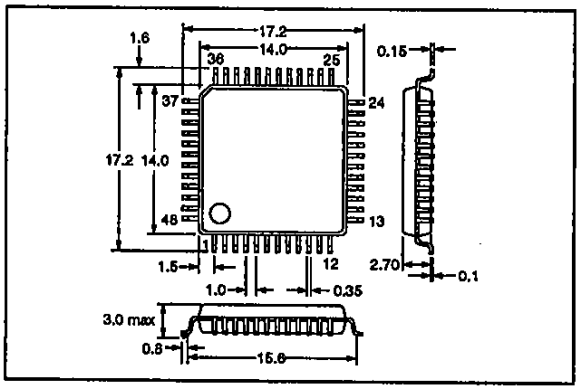
Pin Assignment



Package Dimensions

unit: mm

3156-QIP48E



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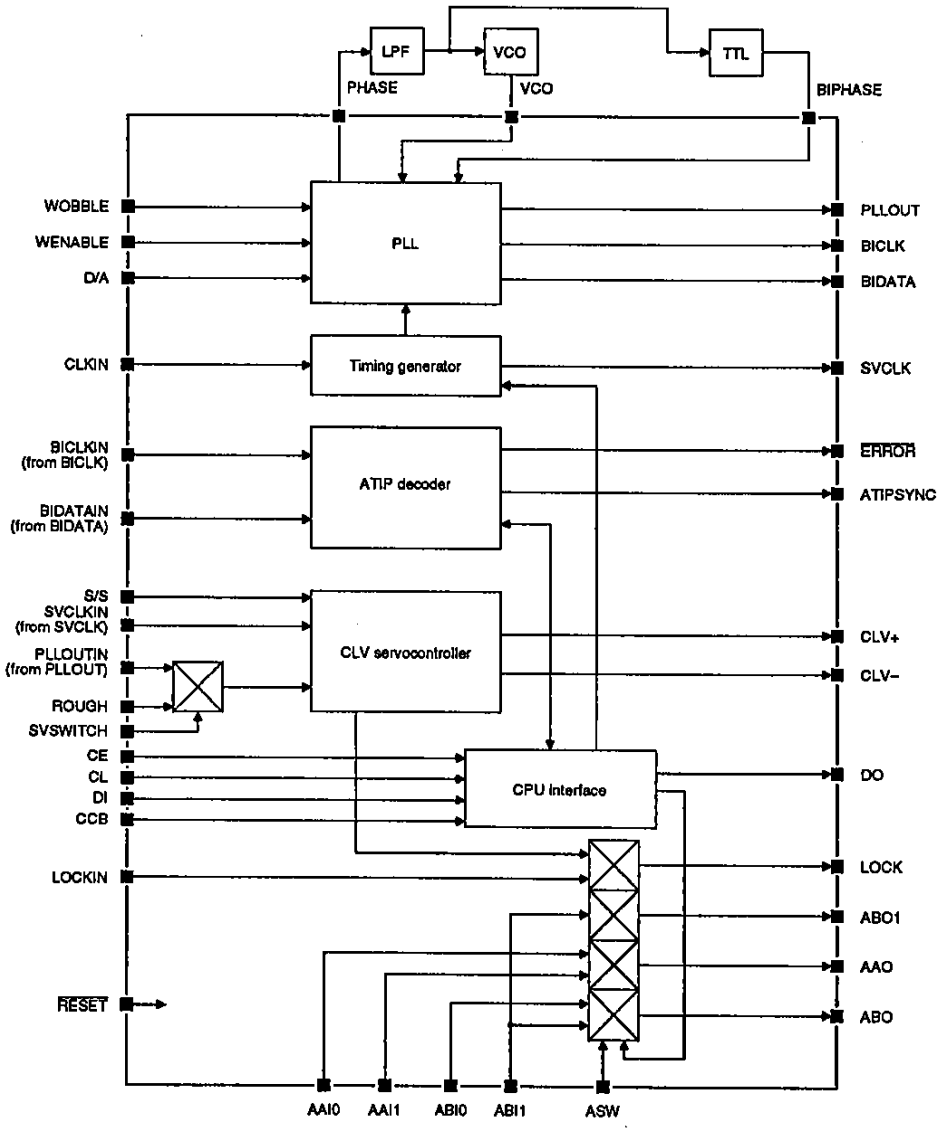
Block Diagram



Pin Functions

Number	Name	Function
1	$\overline{\text{ERROR}}$	Bi-phase data parity error indication output
2	TP0	Test input. Normally connected to VDD
3	BIPHASE	Bi-phase signal input
4	VCO	352.8 kHz VCO output clock input
5	PHASE	PLL phase comparator output
6	VSS	Ground
7	CLKIN	16.9344 MHz clock input
8	SVCLK	2.8224 or 5.6448 MHz CLV servocontroller clock output
9	SVCLKIN	CLV servocontroller reference clock input. Normally connected to SVCLK

Number	Name	Function
10	BICLK	6.3 or 12.6 kHz bi-phase data clock output
11	BICLKIN	Bi-phase clock input for ATIP decoder. Normally connected to BICLK
12	BIDATA	Bi-phase data output
13	BIDATAIN	Bi-phase data input for ATIP decoder. Normally connected to BIDATA
14	PLLOUT	22.05 or 44.1 kHz carrier frequency clock output
15	PLLOUTIN	CLV servocontroller wobble-signal clock input. Normally connected to PLLOUT
16	NC	No connection
17	ROUGH	CLV servocontroller rough-servo mode clock input
18	WOBBLE	Tracking error wobble-component signal input
19	VDD	5 V supply
20	WENABLE	WOBBLE input enable control input
21	D/A	Internal, digital or external, analog PLL select input
22	S/S	CLV+ and CLV– output function select input
23	SVSWITCH	PLLOUTIN or ROUGH clock source select input
24	ASW	Analog switches control input
25	CCB	CPU interface type select input
26	CE	Chip enable input
27	CL	Data clock input
28	DI	Data input
29	DO	Data output
30	$\overline{\text{RESET}}$	Active-LOW reset input
31	VSS	Ground
32	AAI0	Analog switch A input 0
33	AAO	Analog switch A output
34	AAI1	Analog switch A input 1
35	CLV+	CLV servocontroller control output
36	NC	No connection
37	ABI0	Analog switch B input 0
38	ABO	Analog switch B output
39	CLV–	CLV servocontroller control output
40	ABI1	Analog switch B input 1
41	ABO1	Analog switch B output 1
42	VSS	Ground
43	VDD	5 V supply
44	LOCK	CLV servocontroller lock indication output
45	LOCKIN	CD-decoder lock signal input
46	ATIPSYNC	ATIP sync detector output
47, 48	NC	No connection

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Input voltage range (See note 1.)	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage range (See note 1.)	V_O	−0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	−30 to 70	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Soldering temperature (See note 2.)	T_{sol}	260	°C

Notes

1. T_a = 25 °C
2. t < 10 s

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	4.5 to 5.5	V

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
LOW-level input voltage	V_{IL}		–	–	0.8	V
HIGH-level input voltage	V_{IH}		2.2	–	–	V
Input voltage	V_I		0	–	V_{DD}	V
LOW-level output voltage	V_{OL}	I_{OL} = 3 mA	–	–	0.4	V
HIGH-level output voltage	V_{OH}	I_{OH} = 3 mA	2.4	–	–	V

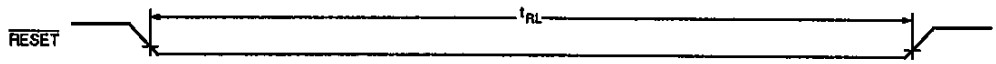
AC Electrical Characteristics

Reset circuit

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C, V_{OL} = 0.8 V, V_{OH} = 2.2 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
$\overline{\text{RESET}}$ LOW-level pulsewidth	t_{RL}		100	–	–	ns

Reset circuit waveform

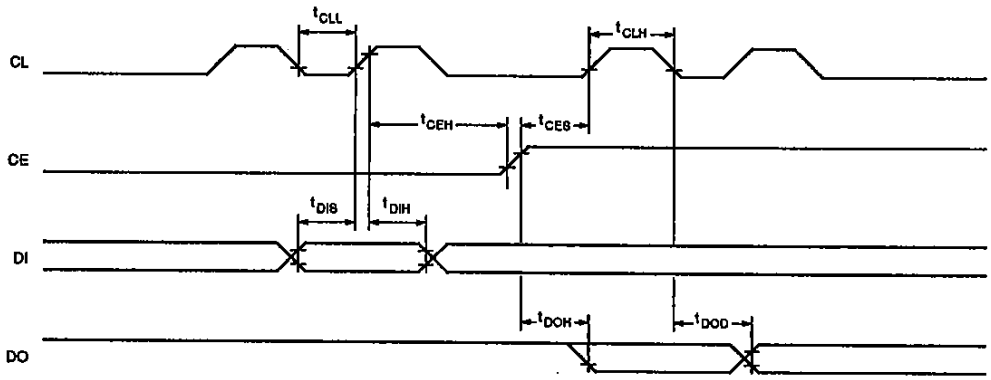


CPU Interface

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 70 °C, V_{IL} = V_{OL} = 0.8 V, V_{IH} = V_{OH} = 2.2 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CL HIGH-level pulsewidth	t_{CLH}		100	–	–	ns
CL LOW-level pulsewidth	t_{CLL}		100	–	–	ns
CE to CL setup time	t_{CES}		10	–	–	ns
CE to CL hold time	t_{CEH}		10	–	–	ns
DI to CL setup time	t_{DIS}		5	–	–	ns
DI to CL hold time	t_{DIH}		15	–	–	ns
CL to DO output delay time	t_{DOD}		–	–	70	ns

CPU Interface waveforms

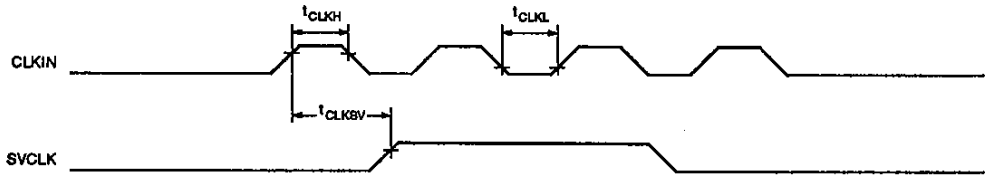


Timing generator

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 70 °C, V_{IL} = V_{OL} = 0.8 V, V_{IH} = V_{OH} = 2.2 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CLKIN input frequency	f_{CLKIN}		–	16.9344	20	MHz
CLKIN HIGH-level pulsewidth	t_{CLKH}		25	–	–	ns
CLKIN LOW-level pulsewidth	t_{CLKL}		25	–	–	ns
CLKIN to SVCLK output delay time	t_{CLKSV}		–	–	50	ns
SVCLK output frequency	f_{SVCLK}	Normal-speed mode	–	$1/8 f_{CLKIN}$	–	MHz
		Double-speed mode	–	$1/3 f_{CLKIN}$	–	

Timing generator waveforms

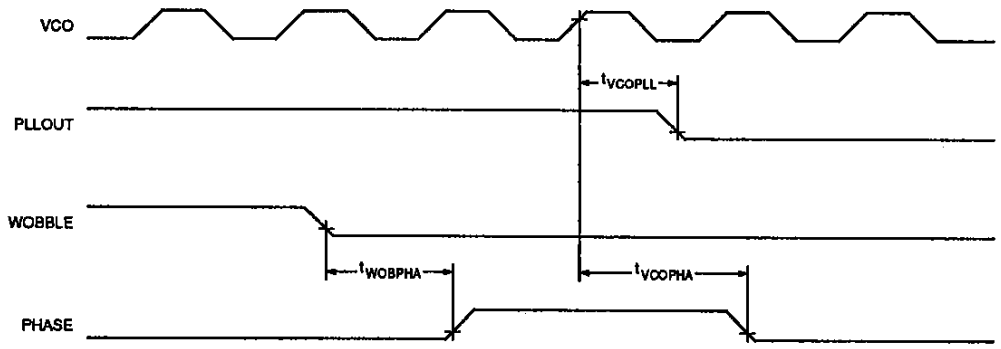


Analog PLL

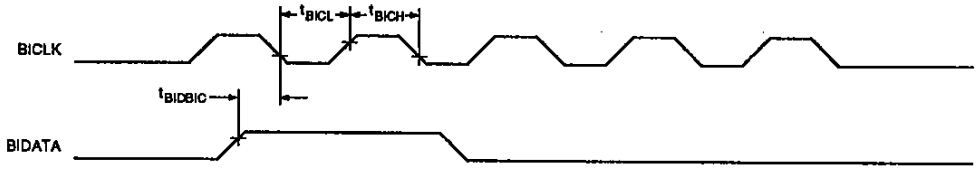
V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C, V_{IL} = V_{OL} = 0.8 V, V_{IH} = V_{OH} = 2.2 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
WOBBLE input frequency	f_{WOBBLE}	Normal-speed mode	–	22.05	–	kHz
		Double-speed mode	–	44.1	–	
VCO input frequency	f_{VCO}	Normal-speed mode	–	16 × f_{WOBBLE}	–	kHz
		Double-speed mode	–	8 × f_{WOBBLE}	–	
BICLK output frequency	f_{BICLK}	Normal-speed mode	–	f_{VCO} ÷ 56	–	kHz
		Double-speed mode	–	f_{VCO} ÷ 28	–	
PLLOUT output frequency	f_{PLLOUT}	Normal-speed mode	–	f_{VCO} ÷ 16	–	kHz
		Double-speed mode	–	f_{VCO} ÷ 8	–	
VCO to PLLOUT output delay time	t_{VCOPLL}		–	–	60	ns
VCO to PHASE output delay time	t_{VCOPHA}		–	–	80	ns
WOBBLE to PHASE output delay time	t_{WOBPHA}		–	–	60	ns
BICLK LOW-level pulsewidth	t_{BICL}	Normal-speed mode	–	24 ÷ f_{VCO}	–	ms
		Double-speed mode	–	12 ÷ f_{VCO}	–	
BICLK HIGH-level pulsewidth	t_{BICH}	Normal-speed mode	–	32 ÷ f_{VCO}	–	ms
		Double-speed mode	–	16 ÷ f_{VCO}	–	
BIDATA to BICLK output delay time	t_{BIDBIC}		−70	–	70	ns

Analog PLL waveforms



Bi-phase clock and data waveforms



Digital PLL

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 70 °C, V_{IL} = V_{OL} = 0.8 V, V_{IH} = V_{OH} = 2.2 V

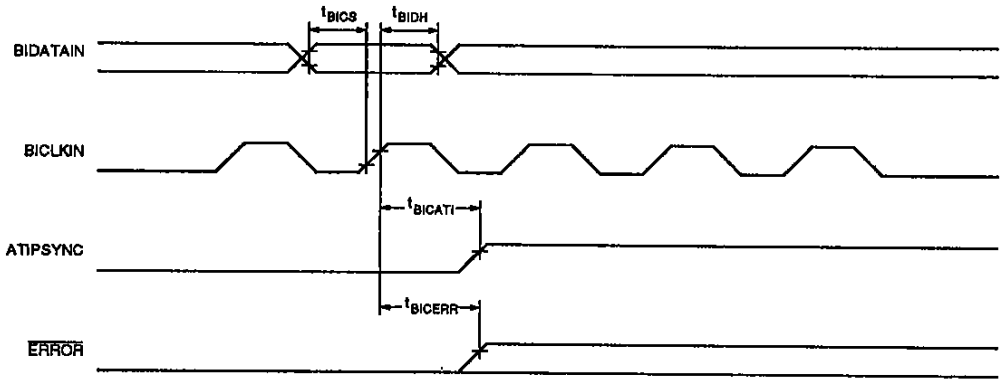
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
WOBBLE input frequency	f_{WOBBLE}	Normal-speed mode	–	22.05	–	kHz
		Double-speed mode	–	44.1	–	
BICLK output frequency	f_{BICLK}		–	2 × f_{PLLOUT} + 7	–	kHz
PLLOUT output frequency	f_{PLLOUT}		–	≤ f_{WOBBLE}	–	kHz

ATIP decoder

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 70 °C, V_{IL} = V_{OL} = 0.8 V, V_{IH} = V_{OH} = 2.2 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
BICLKIN input frequency	$f_{BICLKIN}$		–	f_{BICLK}	–	kHz
BIDATAIN to BICLKIN setup time	t_{BICS}		10	–	–	ns
BIDATAIN to BICLKIN hold time	t_{BIDH}		10	–	–	ns
BICLKIN to $\overline{\text{ERROR}}$ output delay time	t_{BICERR}		–	–	60	ns
ATIPCLK output clock frequency	$f_{ATIPCLK}$		–	f_{SVCLK}	–	kHz
BICLKIN to ATIPCLK output delay time	t_{BICATI}		–	–	60	ns

ATIP decoder waveforms



CLV servocontroller

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C, V_{IL} = V_{OL} = 0.8 V, V_{IH} = V_{OH} = 2.2 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SVCLKIN input frequency	$f_{SVCLKIN}$		–	f_{SVCLK}	–	kHz
PLLOUTIN input frequency	$f_{PLLOUTIN}$		–	f_{PLLOUT}	–	kHz
ROUGH input frequency	f_{ROUGH}		–	f_{PLLOUT}	–	kHz

Functional Description

CPU Interface

The CPU interface uses the Sanyo C²B serial bus format. The CPU inputs commands to the LC89582, and the LC89582 outputs data to the CPU.

The interface waveforms are shown in figures 1 to 4. When CCB is HIGH, command input and output data are preceded by eight address bits, B0 to B3 and A0 to A3, as shown in figures 2 and 4. The command input address is 7AH, and the data output address, 7BH. When CCB is LOW, the address bits are not used.

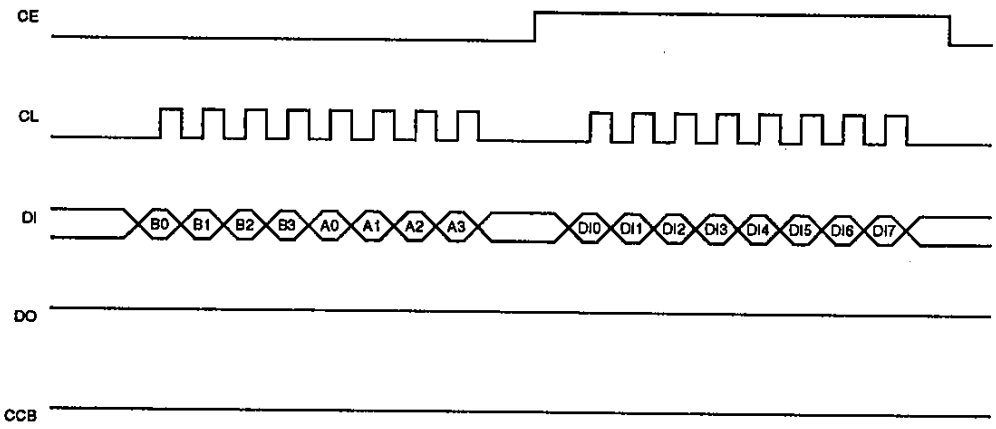


Figure 1. Command input format when CCB is HIGH

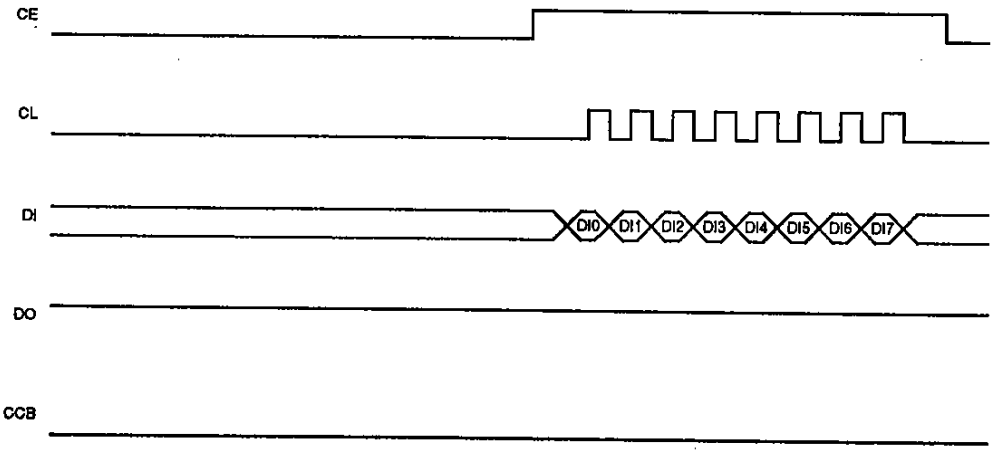


Figure 2. Command input format when CCB is LOW

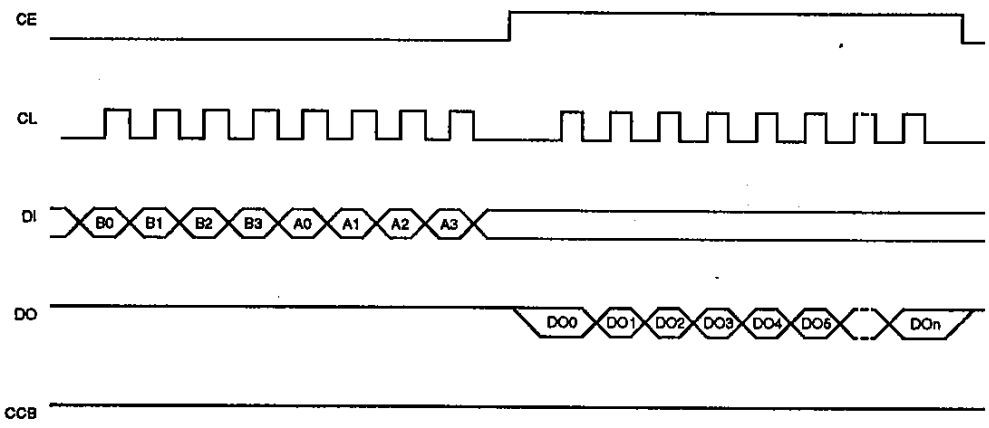


Figure 3. Data output format when CCB is HIGH

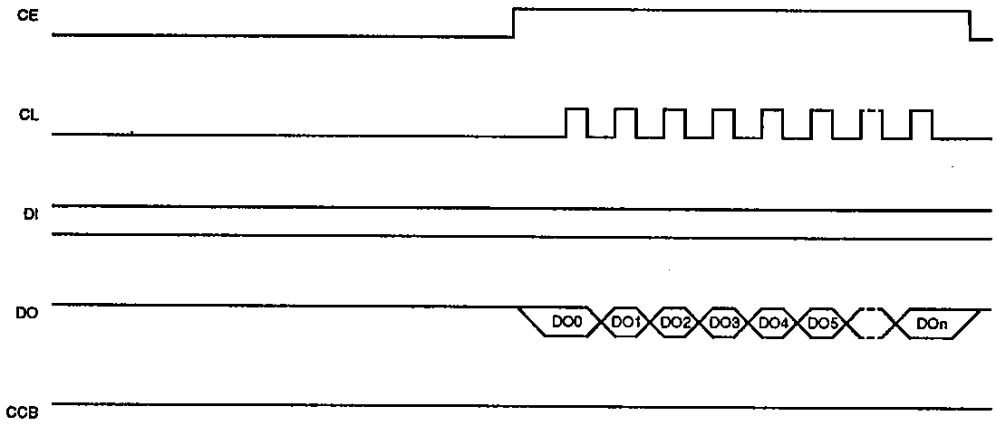


Figure 4. Data output format when CCB is LOW

The commands comprise four address and four data bits as shown in table 1.

Table 1. Command format

Address				Register data			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	RESET	DRES	PRTCT	WS
0	0	0	1	0	0	0	ASWCPU
1	0	0	0	MA3	MA2	MA1	MA0
1	1	×	×	Test data			

Note

× = don't care

The data bits correspond to LC89582 internal registers. The data bit functions are explained in the following sections.

RESET

Setting this bit to 1 resets all circuits except the command registers. The initial value is 0.

DRES

Setting this bit to 1 resets the ATIP sync detector circuit. The initial value is 0.

PRTCT

Setting this bit to 1 turns the ATIP sync detector interpolation protection ON. The initial value is 0.

WS

Setting this bit to 1 turns double-speed mode ON. The initial value is 0.

ASWCPU

This bit is used in combination with the ASW input to control the on-chip analog switches. The initial value is 1.

MA0 to MA3

These bits select the monitor data for output to the CPU. The data formats are shown in table 2.

Table 2. Monitor data

MA3	MA2	MA1	MA0	Monitor data
0	0	0	0	DO0 = CRC, DO1 to DO6 = 0, DO7 = RSTSYS
0	0	0	1	DO0 = CRC, DO1 to DO24 = ATIP data
0	0	1	0	DO0 to DO23 = ATIP data

Notes

RSTSYS	RESET register value
CRC	CRC data value
ATIP data	24-bit ATIP data. Output lsb first

Timing Generator

This circuit generates f_{SVCLK}, which is the digital PLL and CLV servocontroller reference frequency. The normal-speed mode and double-speed mode SVCLK waveforms are shown in figures 5 and 6, respectively.

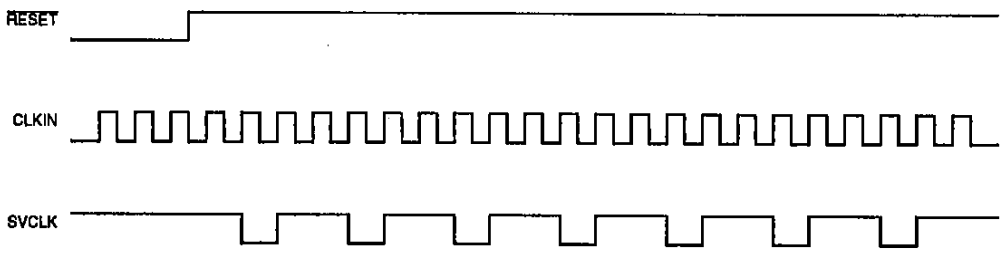


Figure 5. Normal-speed mode SVCLK waveform

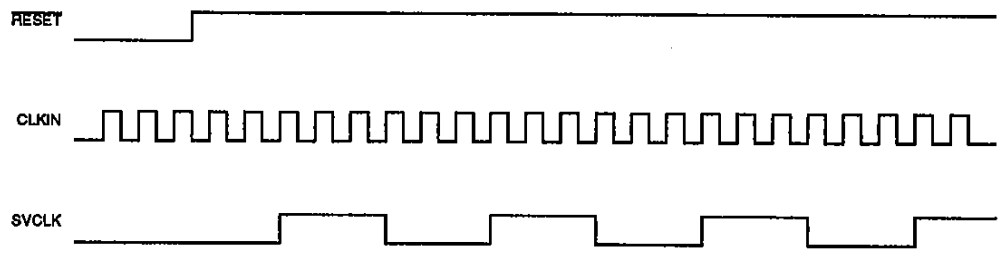


Figure 6. Double-speed mode SVCLK waveform

PLL Circuit

The LC89582 uses either the internal, digital PLL or an external, analog PLL to generate the bi-phase data and clock from the WOBBLE input signal. Note that the internal PLL does not require additional external components whereas an external PLL does. However, an external PLL does allow adjustment of PLL performance. The WOBBLE and bi-phase data and clock waveforms are shown in figure 7, and the analog PLL waveforms, in figure 8.

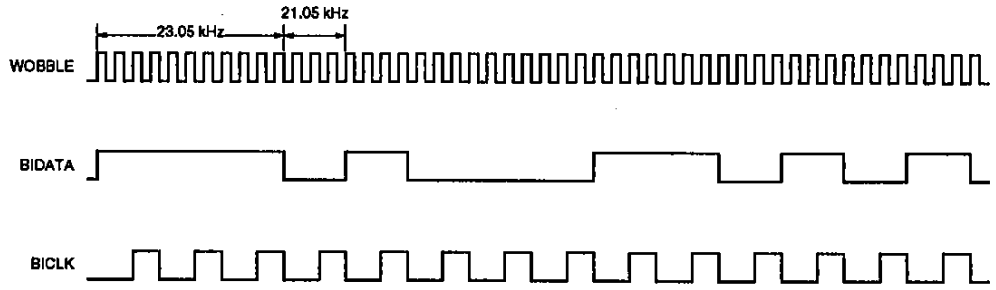


Figure 7. Bi-phase waveforms

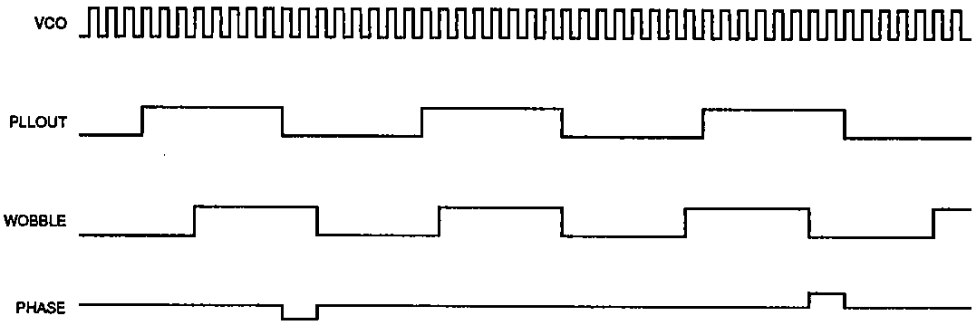


Figure 8. Analog PLL waveforms

ATIP Decoder

The ATIP decoder generates the 24-bit ATIP data and the ATIPSYNC output signal using the bi-phase data and clock generated by the PLL circuit. The ATIP decoder input and output waveforms are shown in figure 9, and the ATIP sync detector flowchart, in figure 10.

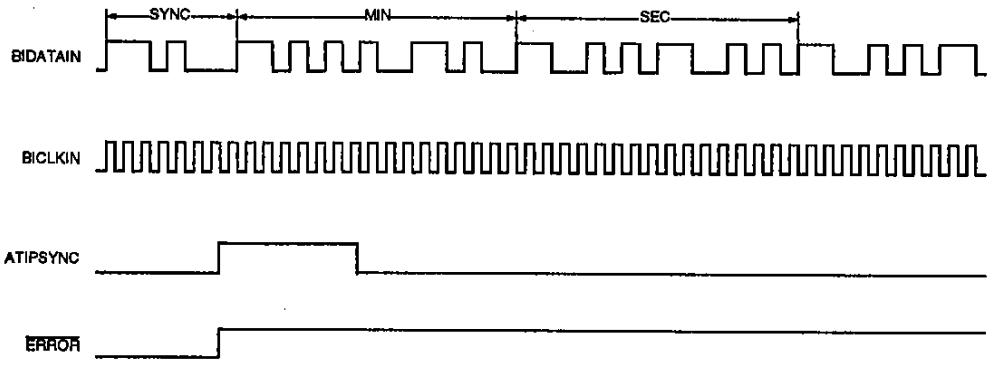


Figure 9. ATIP decoder waveforms

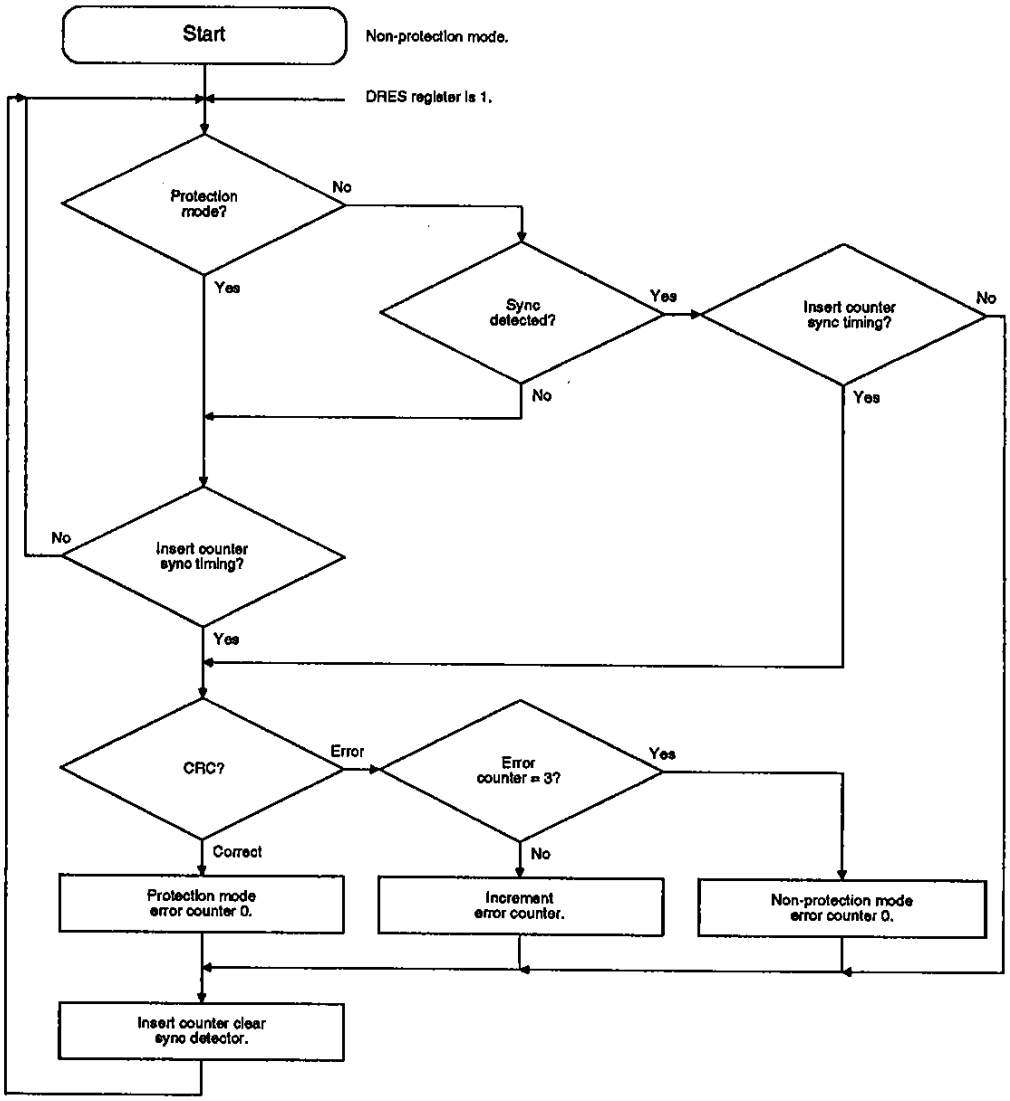


Figure 10. ATIP sync detector flowchart

CLV Servocontroller Outputs

The servocontroller outputs are LOCK, CLV+ and CLV–. LOCK is HIGH when the input clock frequency (from either PLLOUTIN or ROUGH) is within 15% of the SVCLKIN reference frequency.

The CLV+ and CLV– output mode is selected using S/S. When S/S is LOW, CLV+ and CLV– function as disk motor control outputs as shown in table 3.

Table 3. CLV servocontroller modes when S/S is LOW

Internal mode	Condition	CLV+	CLV–	LOCK
Rough servo	Velocity too low	HIGH	LOW	LOW
	Velocity too high	LOW	HIGH	LOW
Phase control	Velocity is correct. The input clock is locked to SVCLKIN.	PWM	PWM	HIGH

When S/S is HIGH, the phase and frequency error signals, MDP and MDS, are output on CLV+ and CLV–, respectively. In this mode, CLV– is HIGH when the reference clock leads the input clock, is LOW when the reference clock lags the input clock, and is high-impedance when they are in phase. CLV+ functions as a clock output. When the reference clock frequency is higher than the input clock frequency, the CLV+ signal has a low duty cycle, and when lower than the input clock frequency, a high duty cycle.

Analog Switches

The built-in analog switches are controlled by the ASW input and the ASWCPU register as shown in table 4.

Table 4. Analog switches

ASW	ASWCPU	Analog switch output		
		AAO	ABO	ABO1
LOW	0	AAI0	ABI0	High impedance
LOW	1	AAI0	ABI0	High impedance
HIGH	0	AAI0	ABI0	High impedance
HIGH	1	AAI1	AAI1	ABI1