

- ◇Structure Silicon Monolithic integrated circuit
- ◇Product name Audio interface + Video driver + POL + RTC LSI
- ◇Type BU76294GUW
- ◇Applications DSC, etc
- ◇Functions <Audio part>
  - Monaural 16 bit  $\Delta \Sigma$  CODEC
  - Monaural microphone amplifier with ALC function
  - Monaural line amplifier
  - BTL output speaker amplifier (300mW@8 $\Omega$ , THD+N=10%, VDD=3.0V)
  - 64-step electronic volume with ALC function
  - PLL built-in (Reference clock: 12MHz, 24MHz, 27MHz, 16fs, 32fs, 64fs)  
(sampling rate: 8kHz ~ 48kHz)
  - Four-line serial interface (power on reset function)
  - Audio IF format MSB First, 2's complement
  - <ADC> 16bit word lengths Left justified, I<sup>2</sup>S
  - <DAC> 16bit word lengths Left, Right justified, I<sup>2</sup>S
- <Video part>
  - Sync-tip-clamp, LPF, 6dB Amplifier
  - Output coupling condenser unnecessary
- <Boot system>
  - Step up charge pump: 1ch, Voltage detect circuit: 4ch built-in
- <RTC part>
  - 32bit counter built-in
  - 128bit back up register built-in

◇Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage	VDD	-0.3~4.5	V	AVDD, IOVDD, SPVDD, VVDD
DVDD Supply voltage	DVDD	-0.3~2.5	V	DVDD
UNREG Supply voltage	UNREG	-0.3~6.0	V	UNREG
BATT Supply voltage	BATT	-0.3~4.5	V	BATT
Input voltage	VIN	-0.3~supply voltage +0.3	V	keep each limits upon
Storage temperature range	TSTG	-50~125	°C	
Operating temperature range	TOPE	-20~85	°C	
Power dissipation *1	PD	800*1	mW	

\* 1: In the case of use at Ta=25°C or more, 8mW should be reduced per 1°C.  
(t=1.6mm, 114.3mm x 76.2mm, board base on SEMI, 4-layer board)  
Radiation resistance design is not arranged.

◇Operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage	VDD	2.7~3.6	V	AVDD, IOVDD, SPVDD, VVDD
DVDD Supply voltage	DVDD	1.62~1.98	V	DVDD
UNREG Supply voltage	UNREG	1.7~5.5	V	UNREG
BATT Supply voltage	BATT	2.0~3.3	V	BATT

(note) Please do not set SPVDD lower than AVDD-0.3V.

(note) Please do not surpass package permissible loss, when SPVDD is set.

◇Electrical characteristics

○Audio interface + Video driver

(Unless specified, Ta=25°C, AVDD=SPVDD=IOVDD=VVDD= 3.0V, DVDD= 1.8V, BATT=3.0V, FBREG=4.2V  
B.W.=22Hz~22kHz, fs=48kHz, fin=1kHz, XIN=32.768kHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
< Current consumption > #MASTER=0 MCLK=24MHz						
Power-down mode	IDDS	-	0.04	0.1	mA	#PWAP=0
Rec mode/PLL mode	IDDR	-	5.8	16	mA	#PWAP=MDREC=MDPLL=1, MCLK=24MHz
Play mode/PLL mode	IDDP	-	5.3	16	mA	#PWAP=MDPB=MDSP=MDPLL=1, MCLK=24MHz
Video mode	IDDV	-	8.2	18	mA	#PWAP=PWVD=1 MDPLL=0
<MREG>						
output voltage	VOREG	0.75AVDD-0.2	0.75AVDD	0.75AVDD+0.2	V	2.2kΩ load
<REC path (MICIN→ADOUT)> #ALC1=OFF, MGAIN=48dB						
Input impedance	ZIN	70	100	130	kΩ	
Input level	VIN	-53	-51	-49	dBV	DOUT=0dBFS
L/R gain mismatch	ΔGV	-1.0	0	+1.0	dB	DOUT=0dBFS
Distortion	THD+N	43	58	-	dB	DOUT=-6dBFS@1kHz
SNR	SNR	59	65	-	dB	B.W.=JIS-A
ALC1 output level	DOALC	-	-7.3	-	dBFS	ALC1=ON
<PB path1 (DAIN→LINEOUT)> #LGAIN=+5dB						
Output level	VO	-5.0	-5.0	-3.5	dBV	DIN=-6dBFS
Distortion	THD+N	-	0.01	0.1	%	DIN=-6dBFS@1kHz
SNR	SNR	81	89	-	dB	B.W.=JIS-A
<PB path2 (DAIN→EVROUT→SPIN→SPOUT BTL output)> #ALC2=OFF, EVR=-6dB, RL=8Ω						
Output level	VO	0.1	2.1	4.1	dBV	DIN=0dBFS
Distortion	THD+N	-	0.1	1.0	%	DIN=0dBFS@1kHz
SNR	SNR	75	82	-	dB	B.W.=JIS-A
ALC2 output level	VOALC	0.1	2.1	4.1	dBV	ALC2=ON, EVR=8dB
< Video path (VIN→VOUT)>						
Voltage gain	GV	+5.0	+6.0	+7.0	dB	VIN=100kHz, 1.0Vpp
Maximum output level	VOM	2.2	2.6	-	Vpp	f=10kHz, THD=1%
Frequency characteristic 1	GF1	-1.0	0	+0.5	dB	f=4.5MHz/100kHz
Frequency characteristic 2	GF2	-	-20	-6	dB	f=18MHz/100kHz

○Back up•RTC

(Unless specified, Ta=25°C, AVDD=SPVDD=IOVDD=VVDD= 3.0V, DVDD= 1.8V, BATT=3.0V, FBREG=4.2V  
B.W.=22Hz~22kHz, fs=48kHz, fin=1kHz, XIN=32.768kHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
< Current consumption >						
UNREG Current consumption	I <sub>cc</sub>	-	50	100	μA	UNREG=4.5V, EV3=no load
BATT Current consumption	I <sub>rtc</sub>	-	1.0	2.0	μA	BATT=3.0V, Counter start
<DC-DC>						
Stop oscillation voltage	V <sub>out</sub>	3.6	3.9	4.2	V	EV3 no load, VDET=FBREG
Operation start voltage	V <sub>start</sub>	-	1.3	1.7	V	Oscillation start, VDET=FBREG*1
<Regulator>						
Output voltage	VREG	2.940	3.000	3.060	V	No load
<Back up SW>						
Change voltage	V <sub>sw</sub>	3.100	3.200	3.300	V	VDET=FBREG
Hysteresis width	V <sub>shys</sub>	40	100	160	mV	VDET=FBREG
<Reset>						
RESET voltage	VRST	2.65	2.75	2.85	V	Hi→Lo detect, VDET=RESETIN
UVLO voltage	VULVO	1.9	2.0	2.1	V	Hi→Lo detect, VDET=UVLO
Hysteresis width	VRhys	40	100	160	mV	
<voltage monitor>						
Output voltage	VPMG	0.45 × UVLO	0.50 × UVLO	0.55 × UVLO	V	
<Logic>						
L input voltage 1	VIL1	DVSS	-	0.3IOVDD	V	ACT
H input voltage 1	VIH1	0.7IOVDD	-	IOVDD	V	ACT
L input voltage 2	VIL2	RTCGND	-	0.3EV3	V	PWRSW0,1
H input voltage 2	VIH2	0.7EV3	-	EV3	V	PWRSW0,1
L output voltage 1	VOL1	DVSS	-	0.2IOVDD	V	I <sub>out</sub> =1.0mA SOUT,PWRSW_STATE,RESETOUT
H output voltage 1	VOH1	0.8IOVDD	-	IOVDD	V	I <sub>out</sub> =-1.0mA SOUT,PWRSW_STATE
L output voltage 2	VOL2	RTCGND	-	0.1EV3	V	I <sub>out</sub> =0.5mA PWRCTRL0,1
H output voltage 2	VOH2	0.9EV3	-	EV3	V	I <sub>out</sub> =-0.5mA PWRCTRL0,1

\*1 The operation of DC-DC start voltage.

◇Block diagram

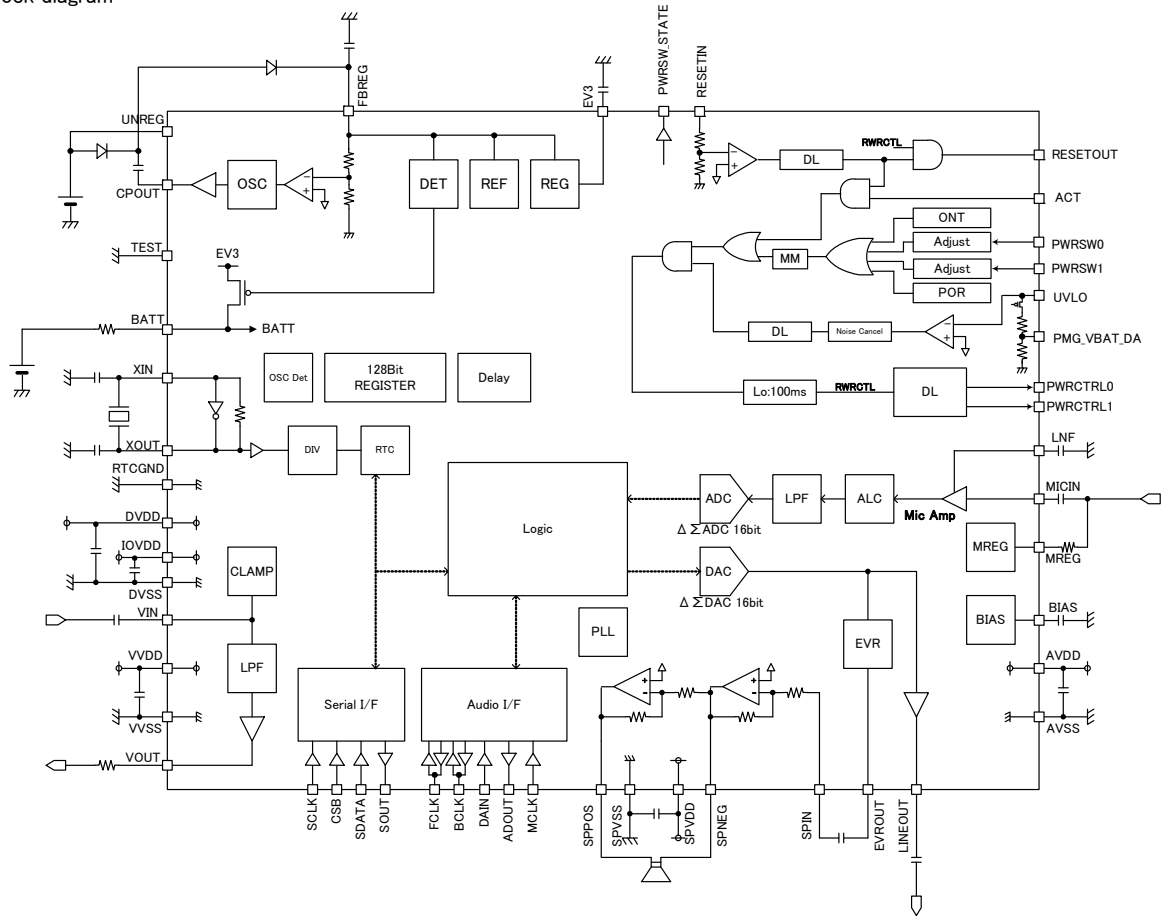


Figure1. Block diagram

(Note)Please the capacitors for AVDD ,BIAS ,LNF ,EV3 pins close to each.

Please the capacitors of X' tal for XIN ,XOUT pins close to each.

◇Pin Functional Descriptions

Pin name	function	Pin name	function
AVDD	Analog power supply	RTCGND	GND for RTC
AVSS	Analog ground	RESETIN	RESET voltage detective output
BIAS	Bias	UVLO	UVLO voltage detective input
MREG	Regulator for MIC	RESETOUT	Reset output
MICIN	MIC input	ACT	ACT input
LNF	MIC NF input	PWRSW0	Power SW0 input
LINEOUT	LINE output	PWRSW1	Power SW1 input
EVROUT	EVR output	PWRCTRL0	Power control0 output
SPIN	SP input	PWRCTRL1	Power control1 output
SPNEG	SP negative output	PMG.VBAT_DA	Voltage monitor output
SPPOS	SP positive output	PWRSW_STATE	Power SW output
SPVDD	SP power supply	DVDD	Digital power supply
SPVSS	SP ground	IOVDD	Digital IO power supply
VVDD	Video driver power supply	FCLK	CODEC frame clock input
VVSS	Video driver ground	BCLK	CODEC bit clock input
VIN	Video driver input	DAIN	CODEC DA serial data input
VOUT	Video driver output	ADOUT	CODEC DA serial data output
UNREG	UNREG voltage input	MCLK	Master clock input
CPOUT	Step up pulse output	DVSS	Digital GND
FBREG	Step up voltage output	SCLK	Serial clock input
EV3	Regulator output	CSB	Serial chip select input
BATT	Back up power supply	SDATA	Serial data input
XIN	Crystal oscillation input	SOUT	Serial data output
XOUT	Crystal oscillation output	TEST	Test terminal

◇Pin assignment(Bottom view)•External dimension

Bottom View

<b>G</b>	RTCGND	XIN	XOUT	VVDD	RESETOUT	SOUT	DVDD
<b>F</b>	PWRSW1	BATT	VVSS	VOUT	ACT	PWRSW_STATE	DAIN
<b>E</b>	PWRCTRL0	PWRSW0	TEST	VIN	DVSS	ADOUT	MCLK
<b>D</b>	EV3	RESETIN	PWRCTRL1	PMG_VBAT_DA	SDATA	FCLK	BCLK
<b>C</b>	UVLO	UNREG	FBREG	SPIN	LNF	SCLK	IOVDD
<b>B</b>		SPPOS	SPVSS	LINEOUT	BIAS	AVDD	CSB
<b>A</b>	CPOUT	SPVDD	SPNEG	EVROUT	MREG	MICIN	AVSS
	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>

Figure 2. pin assignment(Bottom view)

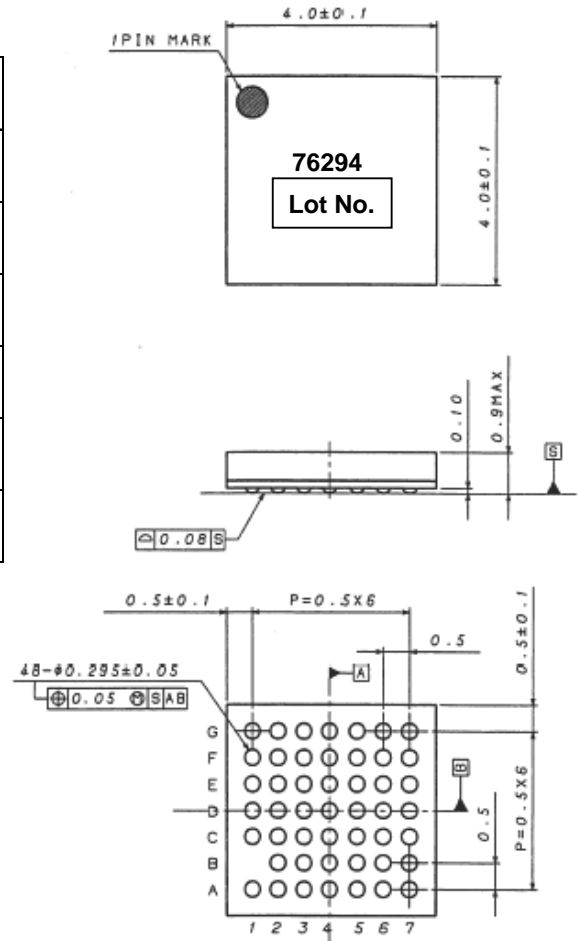


Figure 3. External dimension (Unit: mm)

PKG: VPGA048W040

Drawing No.: EX873-6001

◇Caution

- (1) About absolute maximum rating  
When the absolute maximum rating such as the applied voltage and the ranges of the operating temperature is exceeded, LSI might be destroyed. Please apply neither voltage nor the temperature that exceeds the absolute maximum rating. Please execute physical measures for safety such as fuse when it is thought to exceed the absolute maximum rating, and examine it so that the condition to exceed the absolute maximum rating is not applied to LSI.
- (2) About GND Voltage  
In any state of operation must be the lowest voltage about the voltage of the terminal GND. Please actually confirm the voltage of each terminal is not a voltage that is lower than the terminal GND including excessive phenomenon.
- (3) About design of overheating malfunction preventive circuit  
Please design overheating malfunction preventive circuit with an enough margin in consideration of a permissible loss in the state of using actually.
- (4) About the short between terminals and the mounting by mistake  
Please note the direction and the gap of position of LSI enough about LSI when you mount on the substrate. LSI might be destroyed when mounting by mistake and energizing. Moreover, LSI might be destroyed when short-circuited by entering of the foreign substances between the terminal and GND, between terminals, between the terminal and the power supply of LSI.
- (5) About operation in strong electromagnetic field  
Use in strong electromagnetic field has the possibility of malfunctioning and evaluate it enough, please.
- (6) Please note not to be beyond the package permissible range, When SPVDD is set.

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