M35B32

32 Kbit, 256-byte page, fast program EEPROM memory accessed by SPI bus interface

Target specification

Features

- SPI bus compatible serial interface
- 32 Kbit of EEPROM divided into two sectors:
  - Data sector
  - Event sector
- Large page size: 256 bytes
- Fast programming:
  - Event sector: 256 bytes programmed in less than 1 ms
  - Data sector: 256 bytes written in less than 5 ms
- Low energy EEPROM in either Read, Write, Program or Erase modes
- 2.5 V to 5.5 V single supply voltage
- Operating temperature range:
  - –40°C to +85°C
  - –40°C to +125°C
- Operating frequency, f_C = 20 MHz
- Electronic signature: 20 10 0Ch
- Data cycling:
  - Data sector: more than 1 Million write cycles
  - Event sector: more than 10 000 write cycles
- Data retention:
  - Data sector: more than 40 years' data retention
  - Event sector: 1 year
- Packages
  - ECOPACK® (RoHS compliant)

SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

UFDFPN8 (MC)
2 x 3 mm

Contents

List of tables

List of figures

1 Description

The M35B32 is a 32-Kbit electrically erasable programmable memory (EEPROM) accessed through the SPI bus.

The M35B32 is able to save and store up to 256 bytes within a very short time with the help of the Event sector, this feature being convenient in cases of an unexpected power loss or if an urgent data storage is required. The fast storage is performed with a very low energy budget as the Program time lasts less than 1 ms and as the supply voltage can be as low as 2.5 V associated with a low Programming current (the M35B32 is based on EEPROM cells, energy-saving technology when compared to the Flash technology).

Memory organization

The M35B32 is split into two sectors:

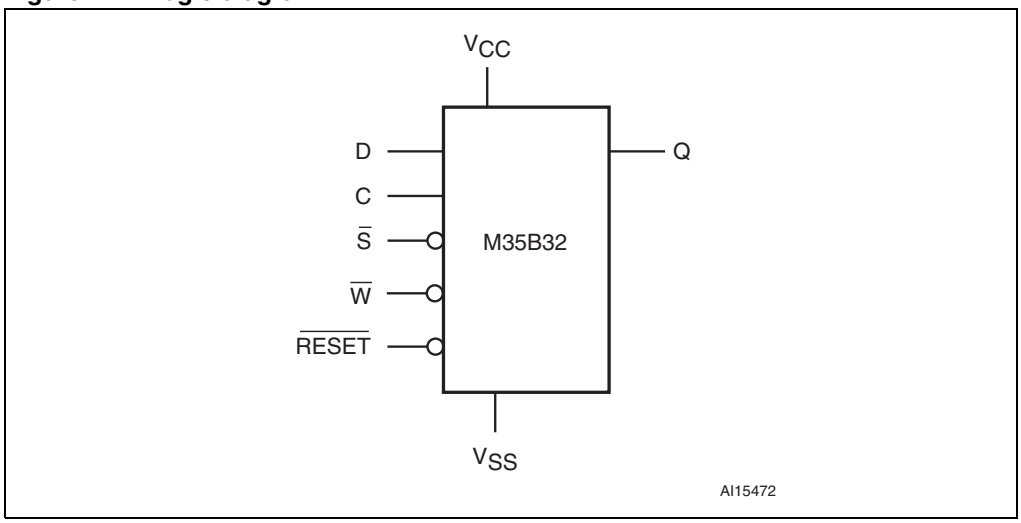
- the Data sector: standard EEPROM which can be written[a] by page (1 to 256 bytes at a time) with a standard write time and a standard retention time,
- the Event sector: data bytes which can be programmed[b] by page (1 to 256 bytes at a time) with a fast programming time and a limited retention time.

The time required to update data is significantly reduced by the Page size (256 bytes) as a page is updated in a single shot.

Both Data sector and Event sector can be erased either a page at a time (using the Page Erase instruction) or a sector at a time (using the Sector Erase instruction).

The size of each sector is defined by the user.

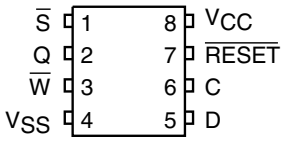
Figure 1. Logic diagram



a. Write cycle = 2 cycles = Erase + Program

b. Program cycle = single cycle (a Write cycle includes two cycles: Erase cycle + Program cycle)

Figure 2. 8-pin package connections



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{RESET}$	Reset	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 10*). These signals are described below.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Read, Program, Erase or Write cycle is in progress, the device will be in the Standby Power mode (this is not the Deep Power-down mode). Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Reset ($\overline{RESET}$)

The Reset ($\overline{RESET}$) input provides a hardware reset for the memory. In this mode, the device is in Standby mode, the WEL and WIP bits are reset (to 0) and the outputs are high impedance.

When Reset ($\overline{RESET}$) is driven high, the memory is in the normal operating mode. When Reset ($\overline{RESET}$) is driven low, the memory will enter the Reset mode[(c)].

c. If the M35A32 is executing a Write (pr program) cycle), the RESET pin driven active (low) does not stop an on going Program or Write cycle.

2.6 Write Protect ($\overline{W}$)

This input signal puts the device in the Hardware Protected mode, when Write Protect ($\overline{W}$) is driven low (V_{IL}), causing the Event sector to become read-only (by protecting them from write, program and erase operations). When Write Protect ($\overline{W}$) is driven high (V_{IH}), the 4 Kbytes of EEPROM memory can be accessed in Read and Write mode.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage. (See also *Section 7* for more)

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 3*, is the clock polarity when the bus master is in Standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. SPI modes supported

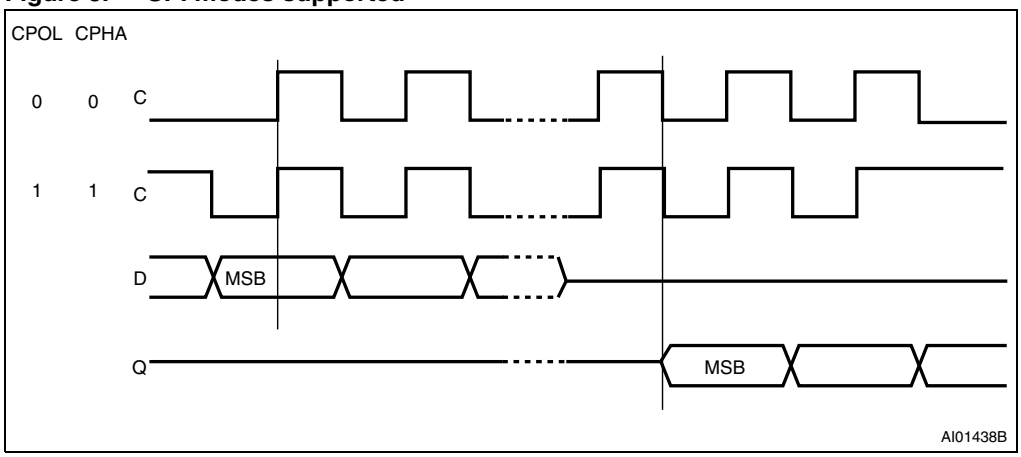
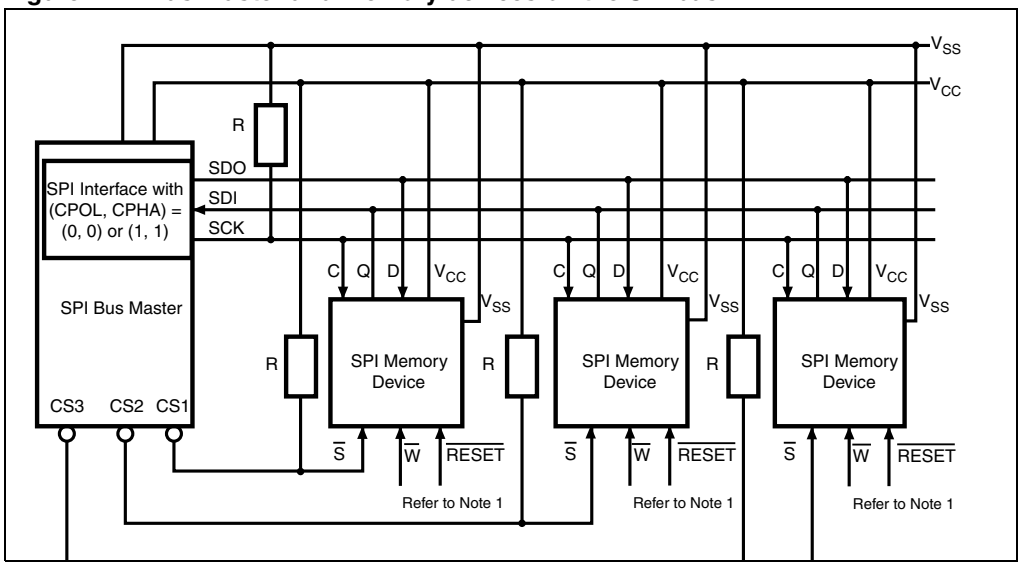


Figure 4. Bus master and memory devices on the SPI bus



Note: 1 The /W and /RESET inputs are CMOS inputs and have also to be driven high or low if/when the SPI bus master leaves the lines in high impedance. This has to be done with the help of pull up or pull down resistors (depending on the application requirements).

Figure 4 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, the other devices are high impedance.

A pull-up resistor connected on each /S input (represented in *Figure 4*) ensures that each slave device on the SPI bus is not selected if the bus master leaves the /S line in the high impedance state.

In applications where the bus master might enter a state where all inputs/outputs SPI lines are in high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high). This ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met.

4 Operating features

4.1 An easy way to modify data

The Page Write (PW) instruction provides a convenient way of modifying data (1 up to 256 contiguous bytes at a time), and simply requires the start address, and the new data in the instruction sequence.

4.2 A fast way to store data

The Page Program (PP) instruction provides a fast way of modifying the data (1 up to 256 contiguous bytes at a time) in the Event sector, provided that these data bytes were erased (by the completion of an earlier Page Erase instruction).

When addressing the Event sector (Sector 0, see *Figure 5*), the Page Program instruction is executed in a very short time (t_{FP}, see *Table 11*), that is about 5 times faster than when executing a Page Program (or Page Write) instruction in the Data sector.

To be correctly used, the Event sector has to be first erased. When an event occurs, data are programmed in the Event sector within a fast time. Later on, when the device receives less requests from the application, the contents of the Event sector can be copied/written into the Data sector (to benefit from the standard data retention time of 40 years), after what the Event sector content can be erased (using only one instruction: the Sector Erase instruction).

4.3 Polling during a write, program or erase cycle

A further improvement in the write, program or erase time can be achieved by not waiting for the worst case delay (t_{PW}, t_{PP}, t_{PE}, or t_{SE}). The write in progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous cycle is complete.

4.4 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M35B32 features the following data protection mechanisms:

- Power on reset can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the WEL bit (in the status register). This bit is returned to its reset state by the following events:
  - Power-up
  - Reset ($\overline{\text{RESET}}$) driven low
  - Write Disable (WRDI) instruction completion
  - Page Write (PW) instruction completion
  - Page Program (PP) instruction completion
  - Page Erase (PE) instruction completion
  - Sector Erase (SE) instruction completion
- The Hardware Protected mode is entered when Write Protect ($\overline{\text{W}}$) is driven low, causing the Event sector to become read-only. When Write Protect ($\overline{\text{W}}$) is driven high, the 4 Kbytes of EEPROM memory can be accessed in Read and Write mode.
- The Reset ($\overline{\text{RESET}}$) signal can be driven low to protect the contents of the memory during any critical time, not just during Power-up and Power-down. When driven active (low), the RESET pin does not stop an on going Program or Write cycle.

5 Memory organization

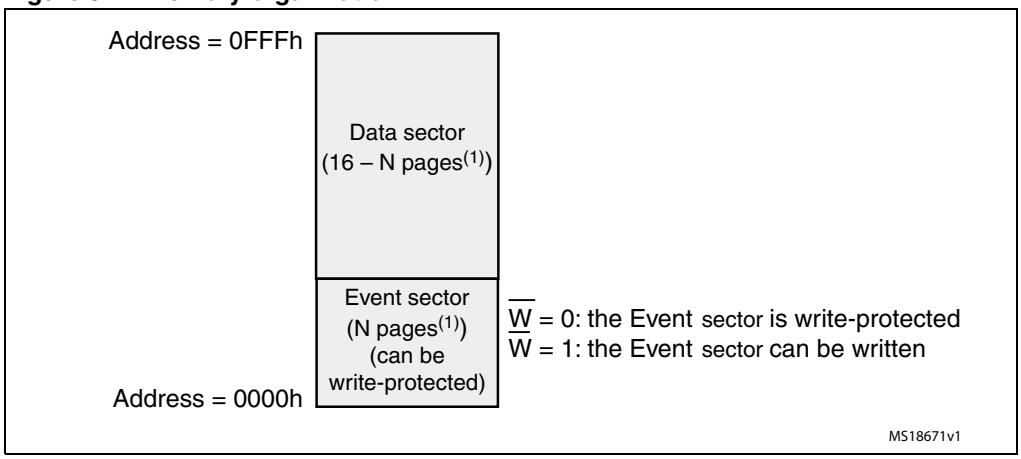
The memory is organized as pages (256 bytes each), with a specific mapping shown in *Figure 5*.

The M35B32 decodes addresses from 0000h up to 0FFFh. This makes an address range of 4 Kbytes organized as 16 pages of 256 bytes. The M35B32 can also be seen as two sectors (the Data sector and the Event sector) which boundary is defined by the BPi status register bits.

- The Data sector (standard EEPROM) is at the top,
- The Event sector (offering a fast programming time tFP) is at the bottom. The Event sector can be also write-protected with pin $\overline{W}$.

Both sectors can be erased in a single cycle, with the help of the Sector Erase instruction; however, each page can be erased using the Page Erase instructions (recommended for the Data sector).

Figure 5. Memory organization



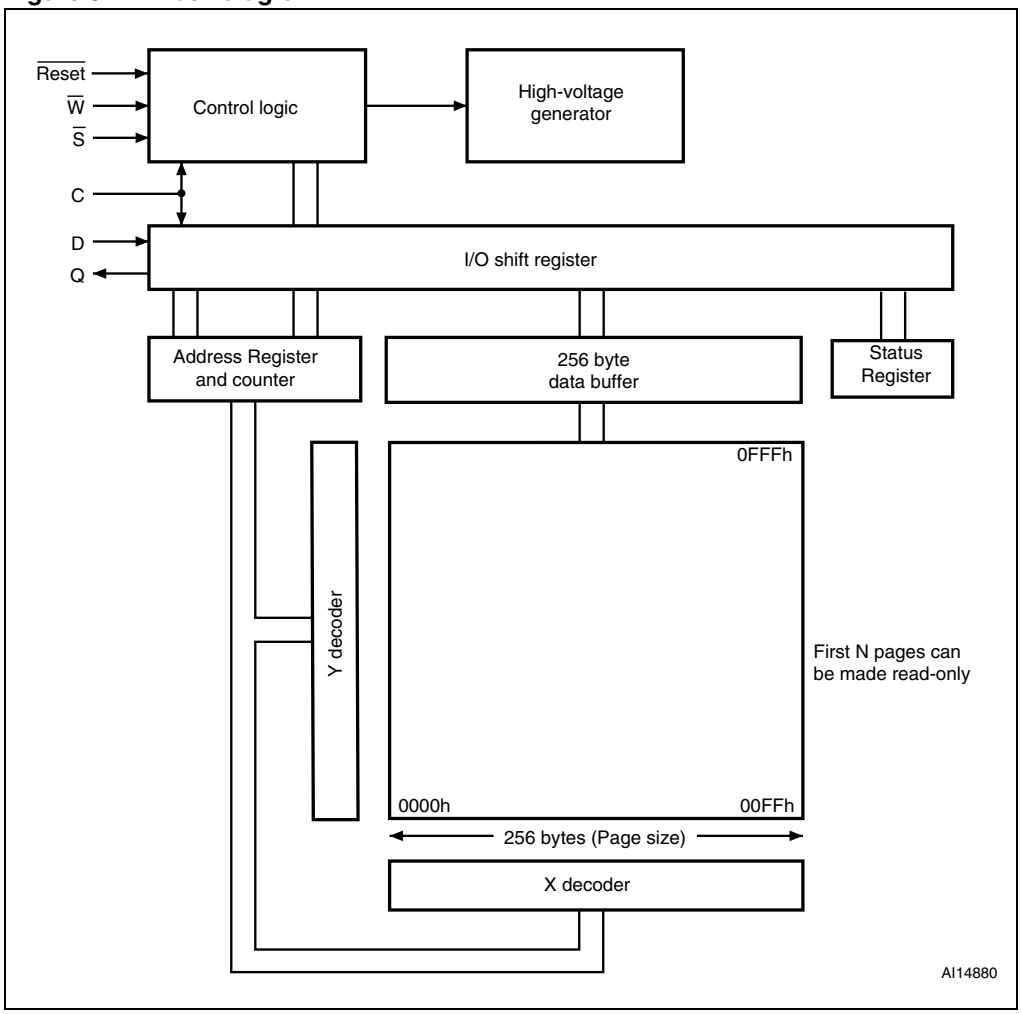
1. N is defined by the BPi bits (see *Section 6.4.3*).

Each page can be individually:

- programmed (bits are programmed from 1 to 0),
- erased (bits are erased from 0 to 1),
- written (bits are changed to either 0 or 1).

When the Page Program instruction addresses bytes in the Data sector, the instruction is executed with the programming time t_{PP}, when the Page Program instruction addresses bytes in the Event sector, the instruction is executed with the fast programming time t_{FP}.

Figure 6. Block diagram



6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in *Table 2*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ) or Read Status Register (RDSR) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven high after any bit of the data-out sequence is being shifted out.

In the case of a Page Write (PW), Page Program (PP), Page Erase (PE), Sector Erase (SE), Write Enable (WREN) or Write Disable (WRDI) instruction, Chip Select ($\overline{S}$) must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven high when the number of clock pulses after Chip Select ($\overline{S}$) being driven low is an exact multiple of eight.

All attempts to access the memory array during a Write cycle, Program cycle or Erase cycle are ignored, and the internal Write cycle, Program cycle or Erase cycle continues unaffected.

Table 2. Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDID	Read Identification	1001 1111	9Fh	0	0	1 to 3
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	1
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
PW	Page Write	0000 0010	02h	3	0	1 to 256
PP	Page Program	0000 1010	0Ah	3	0	1 to 256
PE	Page Erase	1101 1011	DBh	3	0	0
SE	Sector Erase	1101 1000	D8h	3	0	0

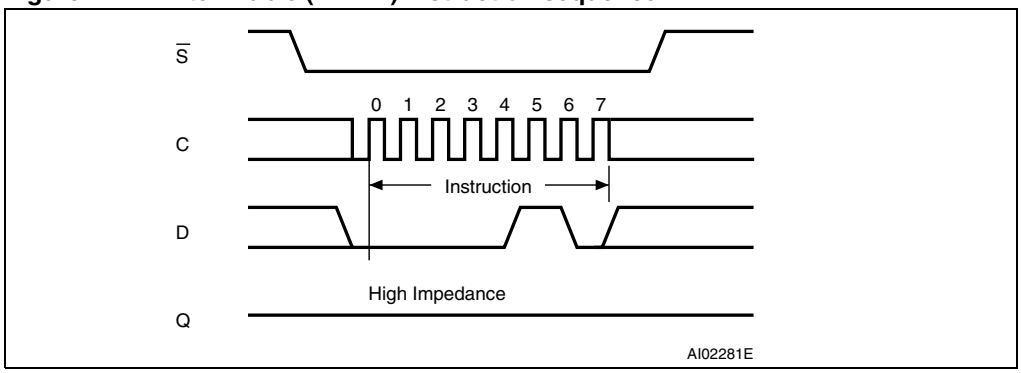
6.1 Write Enable (WREN)

The Write Enable (WREN) instruction (*Figure 7*) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Write (PW), Page Program (PP), Page Erase (PE), and Sector Erase (SE) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) low, sending the instruction code, and then driving Chip Select ($\overline{S}$) high.

Figure 7. Write Enable (WREN) instruction sequence



6.2 Write Disable (WRDI)

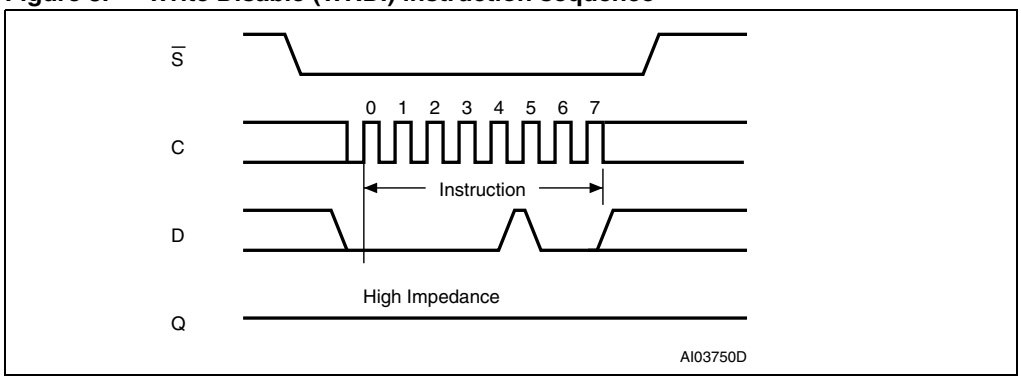
The Write Disable (WRDI) instruction (*Figure 8*) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) low, sending the instruction code, and then driving Chip Select ($\overline{S}$) high.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Write (PW) instruction completion
- Page Program (PP) instruction completion
- Page Erase (PE) instruction completion
- Sector Erase (SE) instruction completion

Figure 8. Write Disable (WRDI) instruction sequence



6.3 Read Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The manufacturer identification is assigned by JEDEC, and has the value 20h for STMicroelectronics. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (58h), and the memory capacity of the device in the second byte (0Ch).

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 9*.

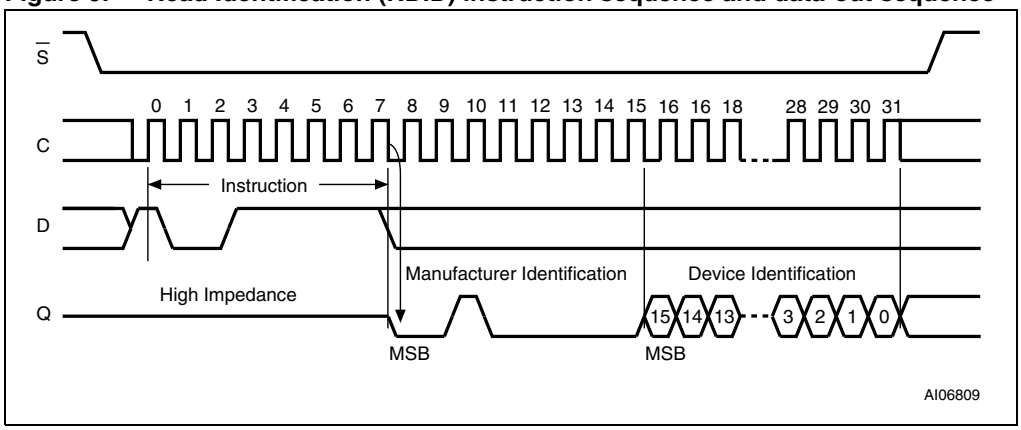
The Read Identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) high at any time during data output.

When Chip Select ($\overline{S}$) is driven high, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 3. Read Identification (RDID) data-out sequence

Manufacturer Identification	Device Identification	
	Memory type	Memory capacity
20h	10h	0Ch

Figure 9. Read Identification (RDID) instruction sequence and data-out sequence



6.4 Read Status Register (RDSR)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	BP3	BP2	BP1	BP0	WEL(1)	WIP(1)
		EEPROM bits				RAM bits	

1. WEL and WIP are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 10*.

The value read by the RDSR instruction depends on the logical signal applied on the $\overline{W}$ input pin:

- if $\overline{W}$=0: Status Register = [0, 0, 0, 0, 0, 0, WEL, WIP]
- if $\overline{W}$=1: Status Register = [0, 0, BP3, BP2, BP1, BP0, WEL, WIP]

The status bits of the Status Register are as follows:

6.4.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.4.2 WEL bit

The WEL bit is set to 1 after decoding a WREN instruction. When the WEL bit is set to 1, a Write, Program or Erase instruction is executed; when set to 0, a Write, Program or Erase instruction is not executed.

The WEL bit is reset to 0 after the completion of a Write, Program or Erase instruction, unless when /W is driven low when addressing the Event sector (see table4).

Table 4. Value of the WEL bit after decoding a Page Write, Page Program, Page Erase or Sector Erase instruction

Targeted M35B32 sector	$\overline{W}$ input = 0	$\overline{W}$ input = 1
Data sector: (16-N) pages(1)	WEL is reset to 0	WEL is reset to 0
Event sector: N pages(1)	WEL is **not** reset	

1. N is defined with BPi bits and (0 < N < 15): Page = 256 bytes.

6.4.3 BPi bits

BPi bits define the size of the Event sector = N pages (one page = 256 bytes), where N is the binary value of (BP3,BP2,BP1,BP0) (0 < N < 15).

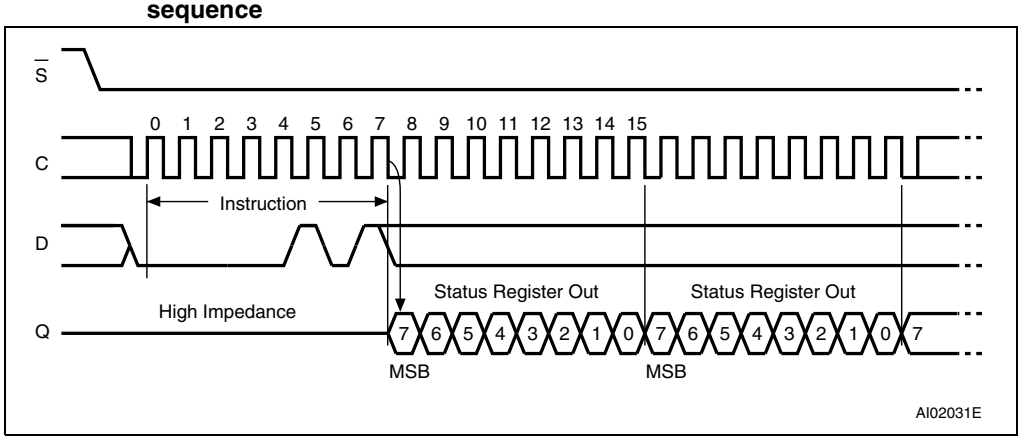
BPi bits also define the size of the write-protected area.

N	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BPi	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111

*Note: 1 The maximum size of the write-protected area is 15 pages (this means that the top page can**not** be write-protected).*

2 When $\overline{W}$=0, the BPi bits cannot be read and the Status Register is read as [0, 0, 0, 0, 0, 0, WEL, WIP].

Figure 10. Read Status Register (RDSR) instruction sequence and data-out sequence



6.5 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code and the data byte on Serial Data input (D).

The instruction sequence is shown in *Figure 11*.

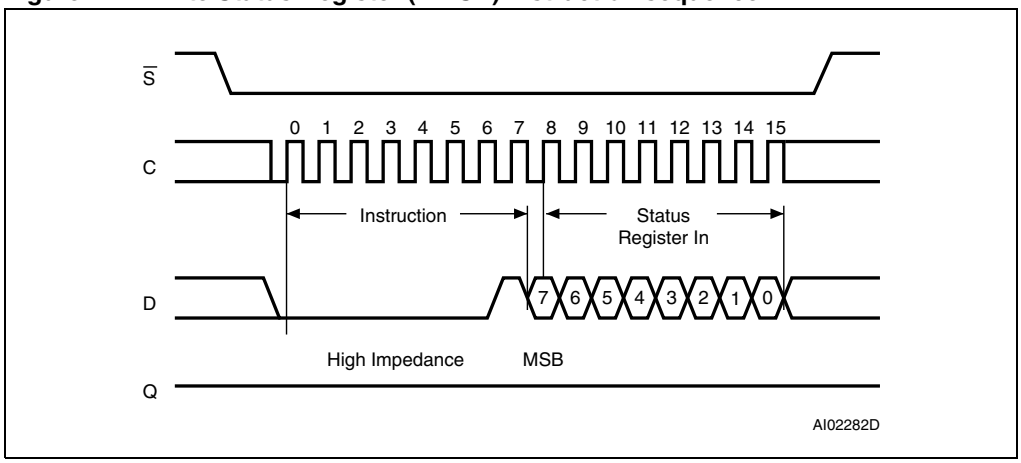
The Write Status Register (WRSR) instruction has no effect on b7, b6, b1 and b0 of the Status Register.

Chip Select ($\overline{S}$) must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read only.

- If the Write Protect pin ($\overline{W}$) is driven high, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction
- If the Write Protect pin ($\overline{W}$) is driven low, attempts to write the Status Register are not executed (even if the Write Enable Latch (WEL) bit was previously set with a previous Write Enable instruction). As a consequence, the size and the write protection status of the Event sector (which size is defined by the (BP3, BP2, BP1, BP0) bits of the Status Register) cannot be modified.

Figure 11. Write Status Register (WRSR) instruction sequence



6.6 Read Data Bytes (READ)

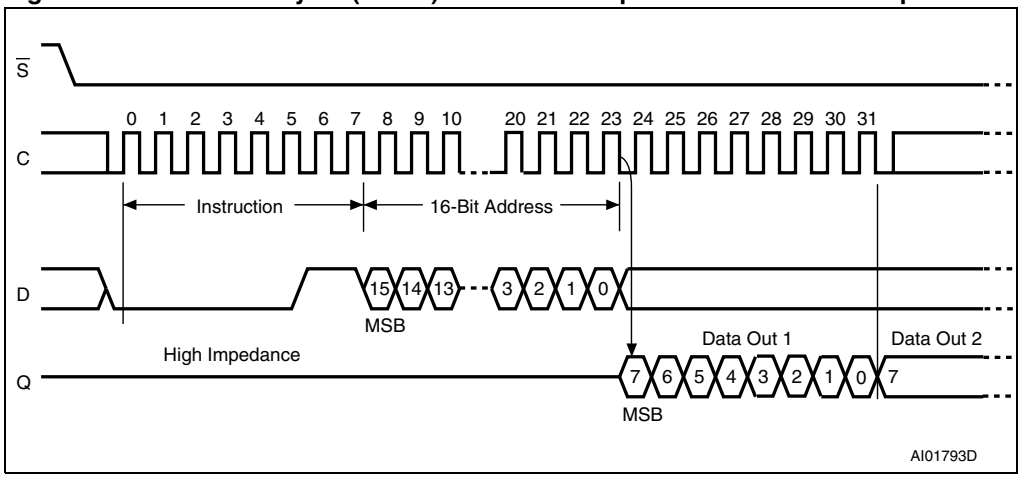
The device is first selected by driving Chip Select ($\overline{S}$) low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 2-byte address (A15-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 12*

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address (0FFFh) is reached, the address counter rolls over to 0000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) high. Chip Select ($\overline{S}$) can be driven high at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Read Data Bytes (READ) instruction sequence and data-out sequence



1. Address bits A15 to A12 are Don't Care.

6.7 Page Write (PW)

As shown in *Figure 13*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address bytes, and at least one data byte are then shifted in, on Serial Data Input (D). The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. In the case of *Figure 13*, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts from the rising edge of Chip Select ($\overline{S}$), and continues for a period t_{PW} (as specified in *Table 11*), at the end of which the Write in Progress (WIP) bit is reset to 0.

However, if Chip Select ($\overline{S}$) continues to be driven low, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 256 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

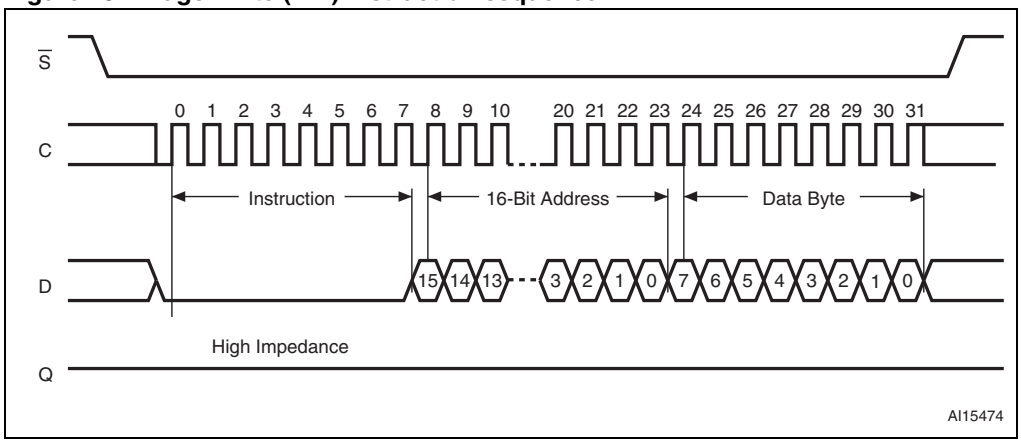
- If the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- If a write cycle is already in progress
- If the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit b0, of the last data byte that has been latched in)
- If the addressed page is in the region protected by the Block Protect (BP3, BP2, BP1, BP0) bits.

Note: The self-timed write cycle t_{PW} is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "1" and a programmed bit is read as "0".

A Page Write (PW) instruction applied to a page that is Hardware Protected is not executed.

Any Page Write (PW) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 13. Page Write (PW) instruction sequence



1. Address bits A15 to A12 are Don't Care
2. $1 \leq n \leq 256$

6.8 Page Program (PP)

The Page Program instruction has be used when addressing erased bytes (see *Note:* below).

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0, only). Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed. (This sets the Write Enable Latch (WEL) bit).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, two address bytes and at least one data byte on Serial Data Input (D). The transmitted data must NOT exceed the addressed page boundary as a wrap round would corrupt the data from the start address of the same page. Chip Select ($\overline{S}$) must be driven low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 14*.

Chip Select ($\overline{S}$) must be driven high after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven high, the self-timed Page Program cycle is initiated. The Page Program cycle lasts t_{PP} when the Data sector is addressed, or t_{FP} when the Event sector is addressed. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is at 1 during the self-timed Page Program cycle, and it is at 0 when the cycle is completed. The Write Enable Latch (WEL) bit is also reset (or not) once the self-timed Page Program cycle is complete, depending on the logical level applied on the $\overline{W}$ input pin and the value of the decoded address, as shown in *Table 4*.

A Page Program (PP) instruction applied to a page that is Hardware Protected is not executed.

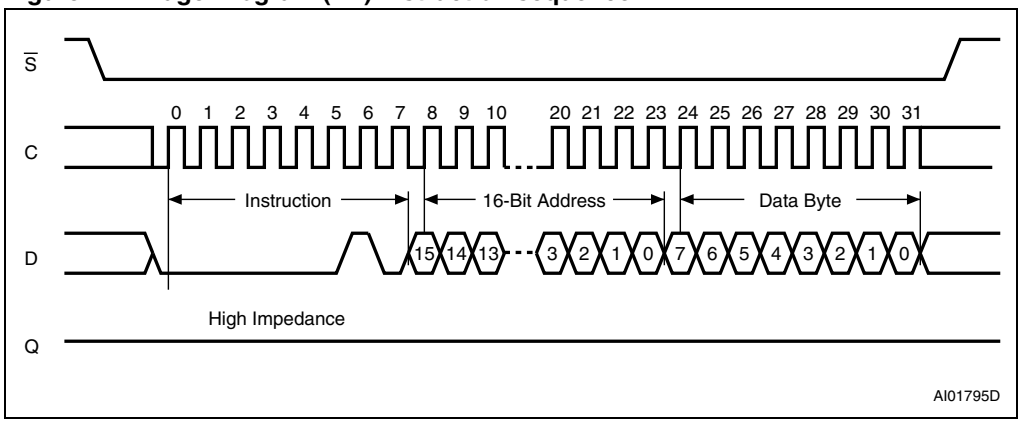
Any Page Program (PP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Note: The Program instruction does not include an Erase cycle (unlike the Page Write instruction, which includes two cycles: Erase+ Program). As a consequence, the Page Program instruction has to be used only when pointing to locations which were previously erased.

In addition, as the M35B32 offers the ECC feature (see Section 6.9), it is important to check, before programming data with the Page Program instruction, that the addressed bytes are inside an erased area defined as a multiple of four bytes.

Example: to program data inside locations [003h-011h], the minimum erased area has to be [000h-013h], because location 003h belongs to the four bytes [000h-003h] and location 011h belongs to the four bytes [010h-013h].

Figure 14. Page Program (PP) instruction sequence



1. $1 \leq n \leq 256$.
2. Address bits A15 to A12 are Don't Care.

6.9 ECC (error correction code) and write cycling

The M35B32 devices offer an ECC (error correction code) logic which compares each 4-byte word with its associated 6 EEPROM bits of ECC. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a read operation, the ECC detects it and replaces it with the correct value. The read reliability is therefore much improved by the use of this feature.

Note, however, that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC bits), that is, the addressed byte is cycled together with the other three bytes making up the word. It is therefore recommended to write data by word (4 bytes) at address 4*N (where N is an integer) in order to benefit from the larger amount of Write cycles.

Those devices are qualified at 1 million (1 000 000) write cycles, using a cycling routine that writes to the device by multiples of 4-byte packets.

6.10 Page Erase (PE)

The Page Erase (PE) instruction is mostly dedicated to the Event sector, as this sector must be erased before executing a Page Program instruction (fast programming time).

The Page Erase instruction resets to 1 (FFh) all bits inside the chosen page. Before it can be accepted, a Write Enable (WREN) instruction must have been executed previously. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Erase (PE) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, and two address bytes on Serial Data Input (D). Any address inside the Page is a valid address for the Page Erase (PE) instruction. Chip Select ($\overline{S}$) must be driven low for the entire duration of the sequence.

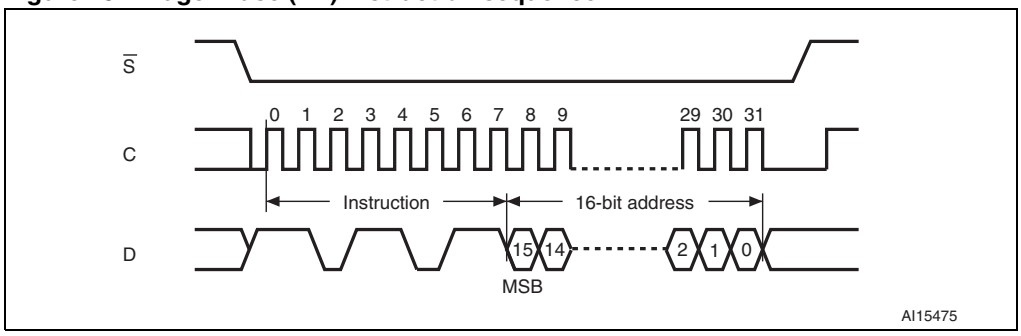
The instruction sequence is shown in *Figure 15*.

Chip Select ($\overline{S}$) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Page Erase (PE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven high, the self-timed Page Erase cycle (whose duration is t_{PE}) is initiated. While the Page Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is at 1 during the self-timed Page Erase cycle, and it is at 0 when the cycle is complete. The Write Enable Latch (WEL) bit is also reset (or not) once the self-timed Page Earse cycle is complete, depending on the logical level applied on the $\overline{W}$ input pin and the value of the decoded address, as shown in *Table 4*).

A Page Erase (PE) instruction applied to a page in Event sector that is Hardware Protected is not executed.

Any Page Erase (PE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 15. Page Erase (PE) instruction sequence



3. Address bits A15 to A12 are Don't Care.

6.11 Sector Erase (SE)

The M35B32 offers two sectors: the Data sector and the Event sector.

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector:

- when the transmitted address is inside the Event sector, the data in the Event sector are erased if the $\overline{W}$ pin is driven high
- when the transmitted address is inside the Data sector, the data in the top pages are erased (whatever the state of the $\overline{W}$ pin)
- when the transmitted address is above 1000h: no action

Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed.

After the Write Enable, the Sector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, and two address bytes on Serial Data Input (D). Any address inside the Sector is a valid address for the Sector Erase (SE) instruction. Chip Select ($\overline{S}$) must be driven low for the entire duration of the sequence.

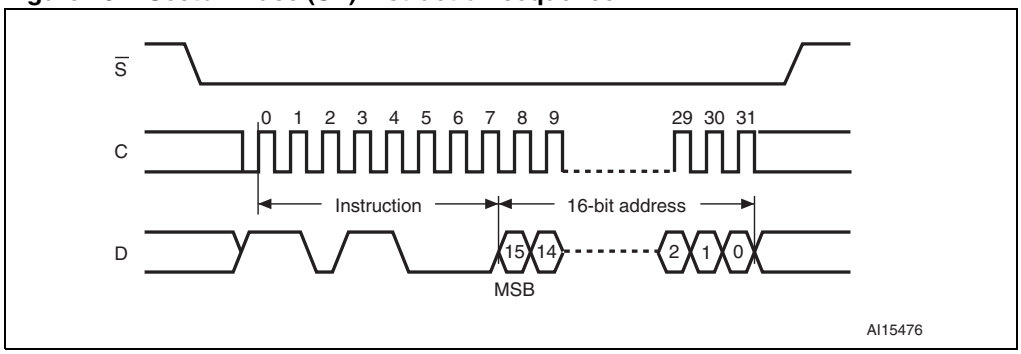
The instruction sequence is shown in *Figure 16*.

Chip Select ($\overline{S}$) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is at 1 during the self-timed Sector Erase cycle, and it is at 0 when the cycle is complete. The Write Enable Latch (WEL) bit is also reset (or not) once the self-timed Sector Erase cycle is complete, depending on the logical level applied on the $\overline{W}$ input pin and the value of the decoded address, as shown in *Table 4*.

A Sector Erase (SE) instruction applied to a sector that contains a page that is Hardware Protected is not executed.

Any Sector Erase (SE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 16. Sector Erase (SE) instruction sequence



1. Address bits A15 to A12 are Don't Care.

7 Power-up and power-down

7.1 Supply voltage (V_{CC})

7.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 6*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for write, program and erase instructions, until the completion of the internal write, program or erase cycle, respectively.

7.1.2 Power-up conditions

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage, it is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor.

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as this input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} rise time must not vary faster than 1 V/µs.

7.1.3 Internal reset during power up

In order to prevent inadvertent write operations during power-up (continuous rise of V_{CC}), a power on reset (POR) circuit is included. At power-up, the device does not respond to any instruction until the V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 6*).

Until V_{CC} has passed over the POR threshold, the device is reset, then the device is in the following state:

- Standby Power mode
- deselected (at next power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instruction can be started)
- Status register:
  - the Write Enable Latch (WEL) is reset to 0
  - the Write In Progress (WIP) is reset to 0

The BP3, BP2, BP1 and BP0 bits of the Status Register are unchanged from the previous power down (they are non-volatile bits).

7.1.4 Power-down

At power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the power on reset threshold voltage, the device is reset and stops responding to any instruction sent to it. During power-down, the device must be deselected (the Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC}) and in Standby Power mode (that is, there should be no internal Write cycle in progress).

As an extra protection, the Reset ($\overline{RESET}$) signal can be driven low for the whole duration of the power-up and power-down phases.

8 Initial delivery state

The device is delivered with the memory array with all bits set to 1. The BPi bits of the Status Register are programmed with (BP3,BP2,BP1,BP0) = (0, 0, 0, 0).

9 Maximum rating

Stressing the device outside the ratings listed in *Table 5* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_{IO}	Input and output voltage (with respect to Ground)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model) (2)		4000	V

1. Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 6. Operating conditions (range 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 7. Operating conditions (range 3)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	125	°C

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		5	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 17. AC measurement I/O waveform

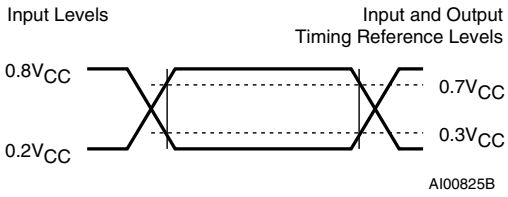


Table 9. Capacitance

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A=25°C.

Table 10. DC characteristics(1)

Symbol	Parameter	Test condition (in addition to those in *Table 6*)	Min.	Max.	Unit
I_{LI}	Input leakage current			± 2	µA
I_{LO}	Output leakage current			± 2	µA
I_{CC1}	Standby current (Standby and Reset modes)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		5	µA
I_{CC3}	Operating current (Read)	C = 0.1V_{CC} / 0.9.V_{CC} at 10 MHz, Q = open		4	mA
I_{CC4}	Operating current (Write or Program)	$\overline{S} = V_{CC}$		4(2)	mA
V_{IL}	Input low voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = -0.4 mA	0.8 V_{CC}		V

1. Preliminary data.
2. Characterized only, not tested in production.

Table 11. AC characteristics

Test conditions specified in *Table 6* and *Table 8*							
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
			V_{CC} = 2.5 to 5.5 V		V_{CC} = 4.5 to 5.5 V		
f_C	f_{SCK}	Clock frequency	D.C.	10	D.C.	20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30		15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30		15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		20		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30		15		ns
t_{CHSL}		$\overline{S}$ not active hold time	30		15		ns
t_{CH}(1)	t_{CLH}	Clock high time	40		20		ns
t_{CL}(1)	t_{CLL}	Clock low time	40		20		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	10		5		ns
t_{CHDX}	t_{DH}	Data in hold time	10		10		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		40		20	ns
t_{CLQV}(3)	t_V	Clock low to output valid		40		20	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		40		20	ns
t_{QHQL}(2)	t_{FO}	Output fall time		40		20	ns
t_{RLRH}(2)	t_{RST}	Reset pulse width	10		10		µs
t_{RHSL}	t_{REC}	Reset recovery time		3		3	µs
t_{SHRH}		Chip should have been deselected before Reset is de-asserted	10		10		ns
t_{WHSL}		Write Protect setup time	50		50		ns
t_{SHWL}		Write Protect hold time	100		100		ns
t_{PW}		Page Write cycle time		5		5	ms
t_{PP}		Page Program cycle time		5		5	ms
t_{FP}		Fast Page Program cycle time (when addressing the Event sector)		1		1	ms
t_{PE}		Page Erase cycle time		5		5	ms
t_{SE}		Sector Erase cycle time		5		5	ms
t_W		Write to Status Register cycle time		5		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.
3. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a Read setup time t_{SU} = 0 ns, t_{CL} can be equal to (or greater than) t_{CLQV}; in all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.

Figure 18. Serial input timing

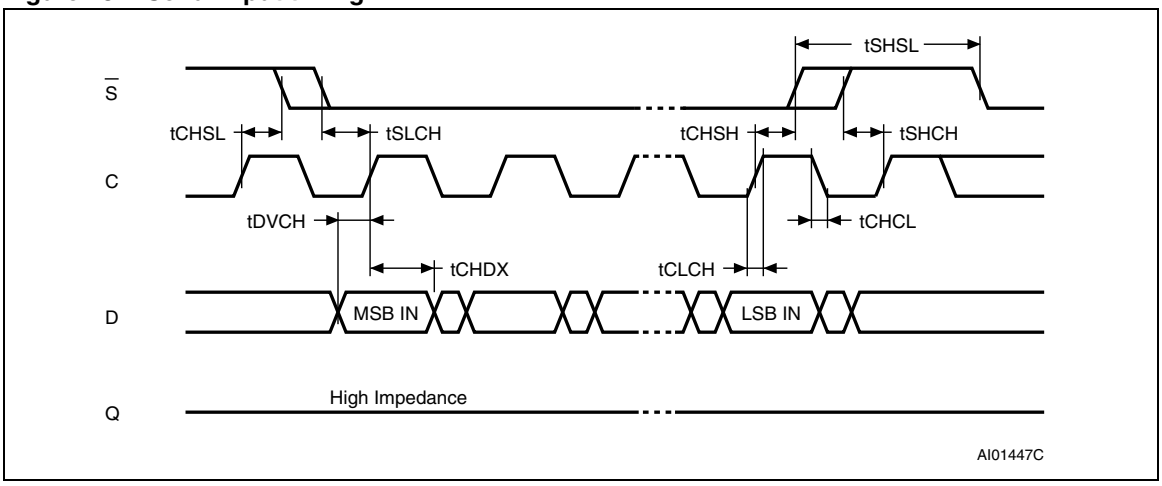


Figure 19. Write Protect setup and hold timing

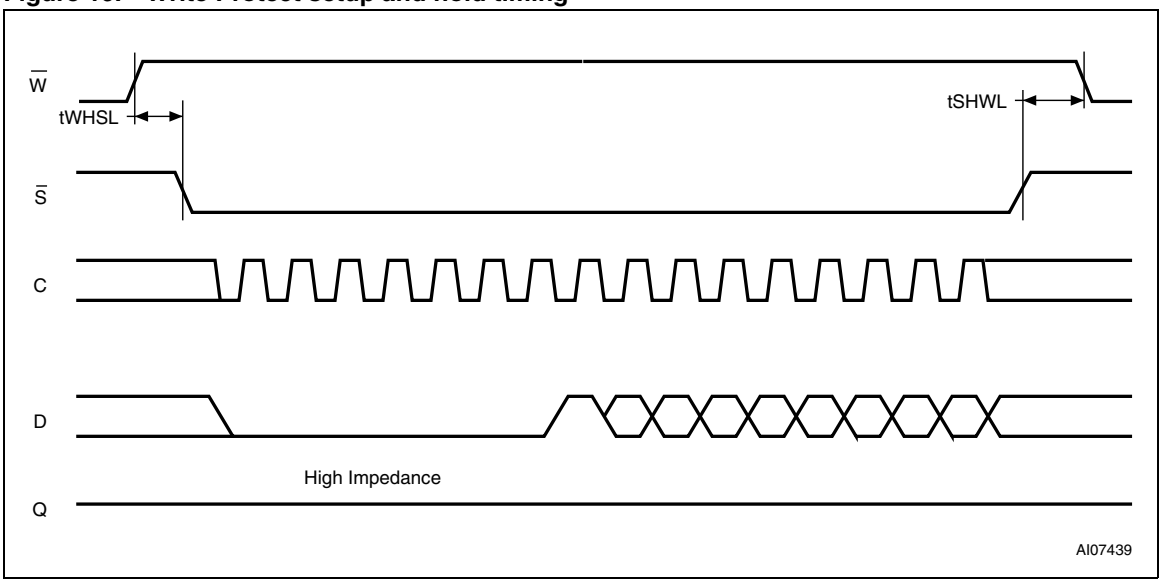


Figure 20. Output timing

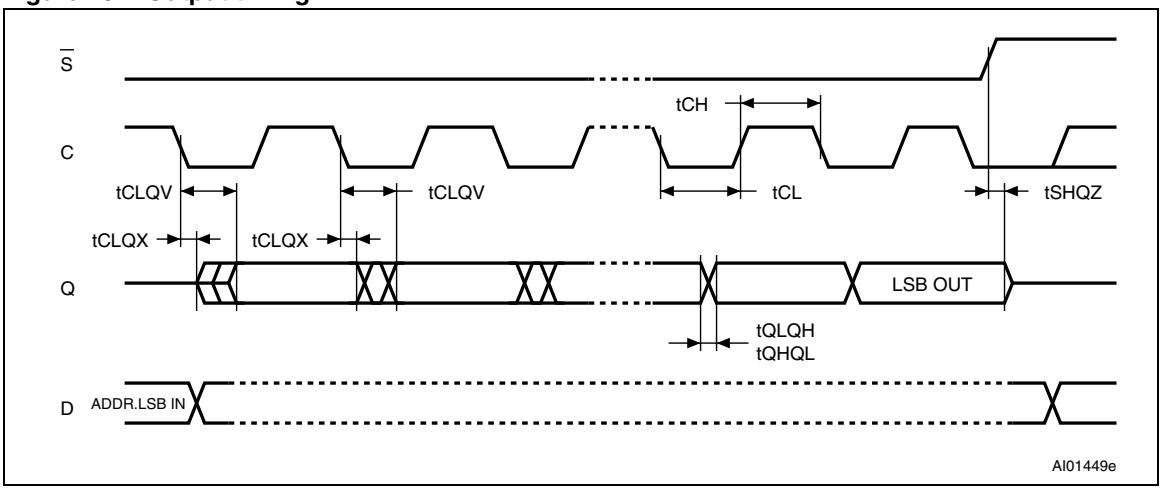
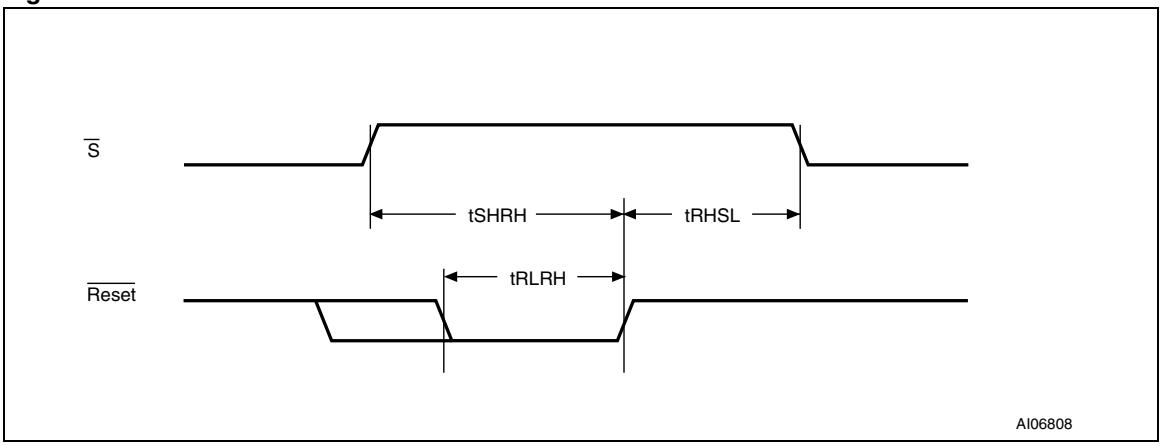


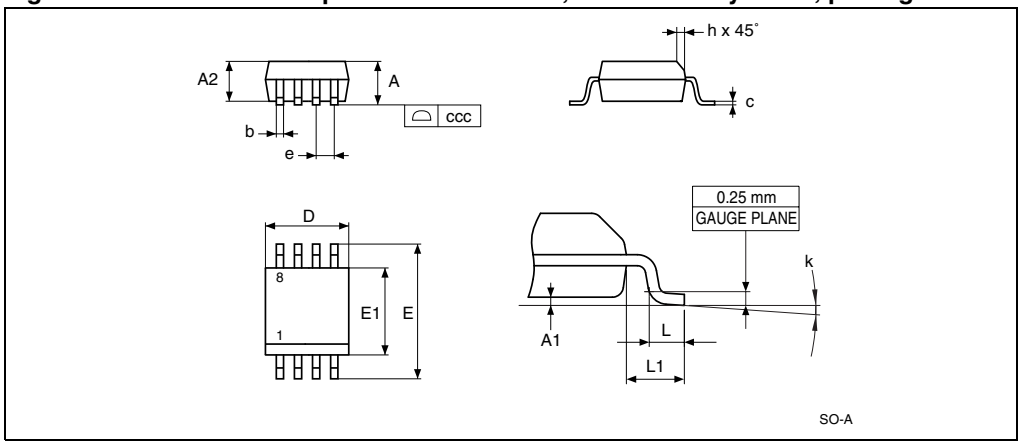
Figure 21. Reset AC waveforms



11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 22. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



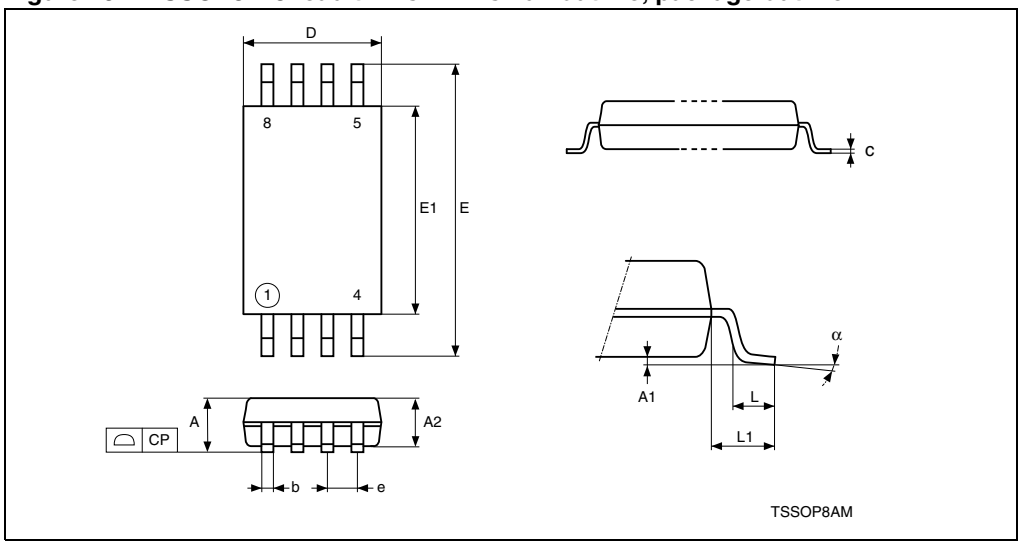
1. Drawing is not to scale.

Table 12. SO8N – 8-lead plastic small outline, 150 mils body width, mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 23. TSSOP8 – 8-lead thin shrink small outline, package outline



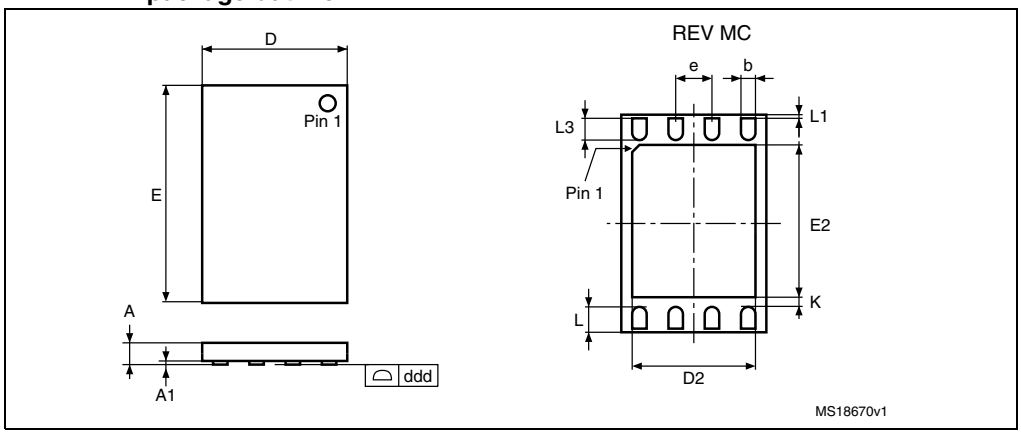
1. Drawing is not to scale.

Table 13. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.2			0.0472
A1		0.05	0.15		0.002	0.0059
A2	1	0.8	1.05	0.0394	0.0315	0.0413
b		0.19	0.3		0.0075	0.0118
c		0.09	0.2		0.0035	0.0079
CP			0.1			0.0039
D	3	2.9	3.1	0.1181	0.1142	0.122
e	0.65	-	-	0.0256	-	-
E	6.4	6.2	6.6	0.252	0.2441	0.2598
E1	4.4	4.3	4.5	0.1732	0.1693	0.1772
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 24. Ultra thin Fine pitch Dual Flat Package No lead (UFDFPN8), 2 × 3mm package outline



1. Drawing is not to scale.
1. The central pad (E2 × D2 area in the above illustration) is internally pulled to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.
1. The circle in the top view of the package indicates the position of pin 1.

Table 14. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0	0.050	0.0008	0	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)		1.20	1.6		0.0472	0.0630
e	0.500	-	-	0.0197	-	-
K	-	0.300	-	-	0.0118	-
L	-	0.300	0.500	-	0.0118	0.0197
L1	-	-	0.150	-		0.0059
L3		0.300	-	-	0.0118	-
ddd[2]	0.050	-	-	0.0020	-	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

12 Part numbering

Table 15. Ordering information scheme

Example: M35B32 – W MN 6 T G /K

Device type

M35B = Application-specific SPI serial access EEPROM

Device function

32 = 32 Kbits (4 Kb × 8)

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V

Package

MN = SO8 (150 mil width)

DW = TSSOP8

MC = UFDFPN8

Device grade

6 = Industrial temperature range, -40 to 85 °C. Device tested with standard test flow

3 = Device tested with high-reliability certified flow(1) automotive temperature range (–40 to 125 °C)

Option

blank = Standard packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process

K= F8H(2)

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The high reliability certified flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Used only for device grade 3.

For a list of available options (speed, package, etc.), please contact your nearest ST sales office.

13 Revision history

Table 16. Document revision history

Date	Version	Changes
15-Mar-2011	1	Initial release.
04-Apr-2011	2	Updated: – *Section : Typical application* – *Note b on page 6*
24-May-2011	3	Status of document changed from Internal to Public.

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