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Quad/x16/Octal T1/E1/J1 Framers

CX28392/8394/8398/8395

Fully–Featured T1/E1/J1 Framers

The highly integrated T1/E1/J1 framers from Mindspeed Technologies™ drive down per-port framer costs, support a scalable system roadmap, and provide a single 3.3 V chip for T1, E1 and J1 applications. They support current ANSI, ETSI, ITU-T, TTC-JT and Bellcore standards. Physical-layer support is provided for alarm generation and detection, error monitoring, per-channel trunk conditioning, and Facility Data Link (FDL) maintenance. Data link layer support is provided for signaling channels (LAPD/SS7) as well as robbed bit (T1) and time slot 16 (E1) Channel Associated Signaling buffers.

A serial Time Division Multiplex (TDM) system bus interface allows the backplane Pulse Code Modulation (PCM) data highway to operate at rates from 1.536 to 8.192 Mbps, with separate TDM buses or combinations of up to four ports multiplexed onto a single TDM bus.

Provision of both transmit and receive slip buffers means that the system interface may be connected to a common backplane for both T1 and E1 services. An additional benefit of this flexibility is that a gapped system interface may be used, at clock rates up to 8.192 MHz.

KEY FEATURES

- 2,4,8 or 16 T1/E1/J1 framers in one package
- T1: SF, ESF, SLC-96, T1DM,TTC JT (J1)
- E1: PCM–30, G.704, G.706, G.732, ETS 300 011, INS 500
- Dual HDLC controllers per framer
- Two–frame transmit and receive PCM slip buffers
- Single 3.3 V power supply

The parallel eight-bit microprocessor port supports Intel- or Motorola-style interfaces. Control and status registers may be memory-mapped and all interrupts from real-time events may be separately masked and latched.

An embedded serial port is included in the CN8394 and CN8398 as an extension of the parallel microprocessor interface and may be used to control external line interface units (LIUs) and other peripheral devices. The framers may be connected directly to most LIUs for non-multiplexed T1 or E1 connections, or to an external mux for higher-rate connections, such as DS3 and E3. Both unipolar (single-rail) non-return to zero (NRZ) and bipolar encoded line interface formats are supported.

Universal Framer for All Framing Types and Standards

All of the main framing formats are supported, including FT only, Superframe (SF), Extended Superframe (ESF) SLC-96™, T1DM, Doubleframe (FAS/NFAS), and FAS + CAS + MFAS. In addition, the Japanese TTC JT-G704 variants of T1 SF and ESF framing are supported, including optional inclusion of the F-bit in CRC-6 remainder calculation. Each of the framers may be independently configured for any of these framing formats, and any combination of frame formats may be simultaneously selected.

Integrated, Automatic Alarms and Maintenance

Support for alarms and maintenance includes on-chip Carrier Failure Alarm (CFA) with dual-slope integration, fully automatic E1 ISDN RAI generation, automatic Performance Report Message (PRM) generation, Bit Oriented and Message Oriented Protocol (BOP and MOP) controllers, and support for Synchronization Status Messages (SSM). A line-synchronized one-second timer is available for scheduling all maintenance message transmission as an automatic, polled or interrupt-driven resource.

Extensive test and diagnostic functions include a full set of loopbacks, payload or unframed PRBS test pattern generation and detection, BER meter, and forced error insertion. Forced single error insertion allows the insertion of several types of errors including framing pattern errors, multiframe pattern errors, PRBS test pattern errors, Change of Frame Alignment (COFA), Cyclic Redundancy Check (CRC) errors, and Line Code Violation (LCV) errors.

Product	Number of T1/E1 Ports	Package	Interface
CX28392	2	128-pin TQFP	Bipolar or single-rail NRZ
CX28394	4	128-pin TQFP	Bipolar or single-rail NRZ
CX28398	8	208-pin PQFP 27mm BGA	Bipolar or single-rail NRZ
CX28395	16	27mm BGA	Single-rail NRZ only
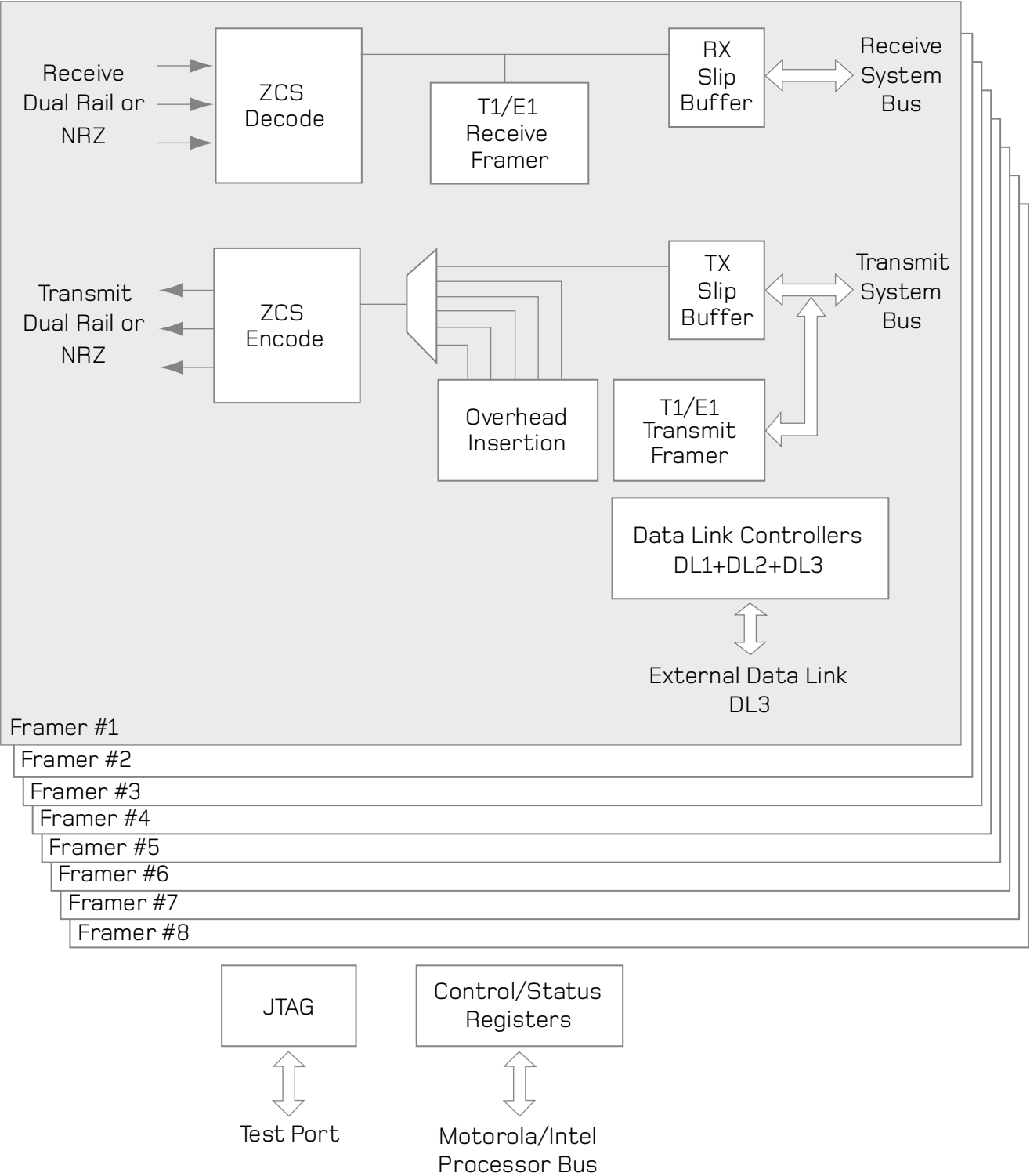
CX28398 functional block diagram

Product Highlights

Frame Alignment

- **Framed formats**
  - Independent transmit and receive framing modes
  - T1: FT/SF/ESF/SLC/T1DM/TTC-JT
  - 1:FAS/MFAS/FAS+CAS/MFAS+CAS
  - Independent framing modes for each port
  - Supports frame alignment in presence of TTC JT yellow alarm and modified CRC-6 procedure in T1 modes
- **Unframed mode**

Signaling

- **T1: two-, four-, or 16-state robbed bit ABCD signaling**
- **E1: Channel Associated Signaling (CAS)**
- **Common Channel Signaling (CCS) in any time slot**
- **Per-channel receive signaling stack**
- **Signaling state change interrupt**
- **Automatic and manual signaling freeze**
- **Debounce signaling (2-bit integration)**
- **Unicode detection**
- **Signaling reinsertion on PCM system bus**
- **Separate I/O for system bus signaling**
- **Per-channel transparent**

Loopbacks

- **Remote loopback toward line**
  - Retains BPV transparency (CN8394/8398 only)
- **Payload loopback**
- **Per-channel DS0 remote loopback**
- **Local loopback toward system**
  - Framer digital loopback
  - Per-channel DS0 local loopback
- **Inband loopback code detection/generation**
- **Simultaneous local and remote line loopbacks**

Processor Interface

- **Parallel 8-bit bus**
- **Data strobes (Motorola™) or address latch enable (Intel®)**
- **Multiplexed or non-multiplexed address/data bus**

Out-Of-Service Testing and Maintenance

- **Pseudo-Random Bit Sequence (PRBS):**
  - Independent transmit and receive
  - 2^{11}; 2^{15}; 2^{20}; 2^{23} patterns
  - Framed or unframed mode
  - Optional 7/14 zero limit
  - Bit Error Counter (BERR)
- **Single error insertion**
  - PRBS error
  - Framing error
  - CRC error
  - BPV/LCV error (CN8394/8398 only)
  - COFA error

System Bus Interface (SBI)

- **System bus data rates:**
  - 1,536 Kbps (T1 without F-bits)
  - 1,544 Kbps (T1)
  - 2,048 Kbps (E1)
  - 4,096 Kbps (2E1)
  - 8,192 Kbps (4E1)
- **Clock operation at 1x or 2x data rate**
- **Selectable I/O clock edges**
- **Bit and time slot frame sync offsets**
- **Embedded T1 framing transport per G.802**
- **Receive and transmit slip buffers**
  - Bypass, 2-frame, or 64-bit depth
  - Slip detection with directional status
  - Slip buffer phase status
  - Per-channel idle code insertion
  - Processor-accessible data buffers
- **Direct connection to line interface units (LIUs)**
  - CN8380

- **Direct connection to upper-layer devices**
  - Link layer: Bt8474
  - ATM layer: CN8228
- **Supported system bus formats:**
  - ATT Concentration Highway Interface (CHI)
  - Multi-Vendor Integration Protocol (MVIP)
  - Mitel ST-bus

In-Service Performance Monitoring

- **One-second timer I/O to synchronize reporting**
- **Receive error detectors with accumulators**
  - Bipolar/Line Code Violations (LCV) (CN8394/8398 only)
  - Excessive Zeros (EXZ) (CN8394/8398 only)
  - Loss of Frame (RLOF)
  - Framing Errors (FERR)
  - CRC Errors (CERR)
  - Far End Block Errors (FEBE)
  - Severely Errored Frames (SEF)
  - Change of Frame Alignment (COFA)
- **Transmit error detectors**
- **Receive alarm detectors**
- **Controlled Frame Slip (RFSLIP)**
- **Uncontrolled Frame Slip (RUSLIP)**
- **Automatic and on-demand transmit alarms:**
  - AIS following RLOS and/or TLOC
  - Automatic AIS clock switching
  - YEL following FRED
  - MYEL following MRED
  - FEBE following CERR
  - Carrier Frame Alarm (CFA) dual-slope integration
  - RAI following FRED
  - RAI following MRED in CRC-4 mode with 100 ms reframe timeout

Data Links

- **Two full-featured data link controllers (DL1 and DL2):**
  - 64-octet transmit and receive FIFOs
  - HDLC Message Oriented Protocol (MOP)
  - Unformatted data transfer
  - Unformatted circular buffer
  - End of message/buffer interrupt
  - Near full/empty interrupts at selected depth
- **Access any bit combination in any time slot:**
  - ISDN D-channels at 16, 32 or 64 Kbps
  - National/spare bits (SA-bits) in 4 Kbps increments
  - CCS/SS7
  - T1DM R-bits
- **Access T1 F-bits in even, odd or all frames:**
  - Automatic Performance Report Message (PRM) generator
  - ESF Facility Data Link (FDL)
  - Unformatted SLC-96 overhead
  - Bit-Oriented Protocol (BOP) priority code word generation and detection
- **Separate I/O for external data link (DL3) (CN8394/8398 only)**

Applications

- **Multi-line T1/E1 channel service unit/data service unit (CSU/DSU)**
- **Digital Access Cross-Connect System (DACS)**
- **T1/E1 multiplexer (MUX)**
- **PBXes and PCM channel banks**
- **ISDN Primary Rate Access (PRA)**
- **Frame Relay Switches and Access Devices (FRADS)**
- **SONET/SDH add/drop multiplexers**

Package

- **208-pin PQFP and 27 x 27 mm BGA (CN8398)**
- **128-pin TQFP (CN8394)**
- **27 x 27mm BGA (CN8395)**

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