Traffic Manager Data Sheet

89TTM552

Preliminary Information*

Description

The 89TTM55x Traffic Manager chipset consists of a 89TTM552 aggregate-flow device and a 89TTM553 per-flow device. The 89TTM55x Traffic Manager manages bandwidth resources by shaping traffic to defined rate profiles and by precisely controlling the allocation of bandwidth and acceptance of new traffic during times of network congestion. The 89TTM55x provides a full suite of configurable algorithms that support quality of service differentiation for any data protocol, at line rates of 10 Gbps.

The 89TTM552, which can operate as a standalone device, is a 10 Gbps simplex device providing the following features:

- *An aggregate-flow (AFQ) scheduler that can be used for class-based, virtual pipe, or flow scheduling for up to 4K queues.*
- *A logical port scheduler (1K port queues).*
- *Output queuing for channel-based backpressure from a framer or fabric (1K OQs).*
- *Supports up to 256 MB external data buffering.*
- *Sophisticated congestion management features to manage buffer resources.*
- *Spatial multicast labeling for the switch fabric and logical multi-casting.*
- *Packet segmentation and reassembly across fabric or SPI4.2 channels.*
- *AAL-5 segmentation and reassembly.*

The 89TTM552 can be used in standalone mode to handle congestion management and scheduling of traffic where three levels of hierarchy and 4K queues (AFQs) are sufficient.

The 89TTM552 can perform simultaneous scheduling of a large number of flows, each at an individual rate of fine granularity, and with many user-configurable features allowing maximum flexibility and performance. It has congestion management mechanisms that manage shared traffic buffering resources. If buffer memory approaches its limit because data arrives at a queue faster than it can depart, the 89TTM552 performs per-queue congestion management. It can also intelligently discard lower priority traffic as it arrives until memory resources become available.

The 89TTM552 controls traffic forwarding, manages the shared buffer resources with multi-level thresholding, maintains the various queues, and generates queue service selections (scheduling for departures) using bandwidth management algorithms developed by IDT. Using industry-standard 16-bit LVDS Rx and Tx interfaces, the 89TTM552 receives and transmits data as packets or cells.

The 89TTM552 manages its data storage internally. It has fixed blocks of memory for storing and forwarding data, and for managing memory resources according to quality of service parameters. Each block, or cell, contains up to 64 bytes of data payload from a packet. The 89TTM552 can process up to 35 Mcps/Mpps for both arrivals and departures. The 89TTM552 and 89TTM553 both operate up to 175 MHz.

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The 89TTM552 connects seamlessly to IDT's 89TSF family of switch fabric products. It can also operate seamlessly with network processors and switch fabrics that use one of its 16-bit LVDS interface protocols. The 89TTM552 can also directly transmit to third-party framers/PHYs that have SPI4.2 interfaces.

The 89TTM553 consists of a flow-based available-rate scheduler with a weighted fair queuing (WFQ) engine and adds support for further hierarchical scheduling with queues for up to 1M flows. Both devices, the 89TTM552 and 89TTM553, are used when additional hierarchical scheduling and a large number of simultaneous flows are required. See Figure 1 for a functional diagram of the 89TTM55x chipset.

89TTM552 Interfaces

The 89TTM552 has a 16-bit LVDS receive interface and a 16-bit LVDS transmit interface. These two interfaces can be configured independently to operate in one of the following 4 modes.

Note: In the following 2 modes, up to 16 channels or output queues are supported.[1]

- *OI Forum SPI-4p2 (System Packet Interface, Level 4, Phase 2). SPI-4p2 (or SPI4.2) is a physical interface standard for the transfer of data between a network processing device and a framer. It is anticipated that this mode will be used on the 89TTM552's interface to a network processor or a framer.*
- *NPF Streaming Interface (NPE-NPE).*
  It is anticipated that this mode will be used on 89TTM552's interface to an NPU.

Note: In the following 2 modes, up to 1024 channels or output queues are supported.

- *NPF Streaming Interface (NPE-Fabric).*
  It is anticipated that this mode will be used on 89TTM552's interface to a switch fabric.
- *CSIX over LVDS.*
  It is anticipated that this mode will be used to interface to a switch fabric (including the 89TSF552/89TSF500 fabric).

The interfaces are 16 bits wide, in each direction, and transfer data at up to 1.0 GHz. The interface between the 89TTM552 and 89TTM553 consists of two unidirectional, source-synchronous buses. The interface is a DDR proprietary interface. Each interface includes a clock (175 MHz) and parity.

A 32-bit CPU interface provides system access to the 89TTM552's registers, internal memory, and external memory. A 16-bit CPU interface provides system access to the 89TTM553's registers, internal memory, and external memory. See Figure 2 for an example of a full-duplex 10 Gbps system configuration.

89TTM55x Features

- **Deterministic performance at 10 Gbps wire-speed (35 Mcps) regardless of the number of flows, traffic size, and patterns.**
- **Up to 256 megabytes of external memory buffer space (equivalent to a 210 ms buffer at 10 Gbps).**
- **Support (Rx and Tx) for industry-standard SPI-4 phase 2, NPF Streaming Interface, and CSIX over LVDS.**
- **Hierarchical queuing and precise scheduling:**
  - *Traffic management flexibility.*
  - *Support for up to 4K aggregate flow queues (AFQs), 2K arrival reassembly queues (ARQs), 1K port queues (PQs) and 1K output queues/channels (OQs) with no external memory required. Configurable AFQ-to-port assignments.*
  - *Support for up to 1M discrete flows (FLQs), with queuing for each flow, using external memory. Configurable mapping of FLQs into aggregate flow queues.*
  - *Two-level FLQ scheduling mode that supports up to 128K or 256K virtual pipe or subscriber queues with up to 8 or 4 CoS priority queues each.*
  - *Accurate byte-rate shaping at the FLQ, AFQ and port levels.*
- **Multiple levels of buffer congestion management.**
  - *Hierarchical queue structure and thresholding.*
  - *Congestion indication.*
  - *Dynamic adjustment of thresholds during periods of congestion.*
  - *Packet discard (PD).*
  - *Weighted random early discard (WRED).*
  - *Local congestion indication (CI).*
- **Configurable forwarding based on classification index.**
- **Two ports for obtaining event-based statistics.**
- **Configurable on-chip diagnostic statistics.**
- **Bandwidth management rate guarantee and shaping mechanisms for each flow, each aggregate flow and each port queue.**
  - *Priority and weighted bandwidth distribution mechanisms across groups of flows and aggregate flows.*
  - *Schedules rates as low as 2 kbps for each flow.*
  - *One- and two-level byte-rate FLQ scheduling: maximum and minimum rates, and strict priority and weighted fair queuing (WFQ) for each FLQ. Per-flow byte-rate shaping.*
  - *AFQ scheduling with byte-rate shaping: minimum and maximum rates with VBR MBS and PCR enforcement. Excess distribution using weighted fair queuing (WFQ) and PRR.*
  - *Port queues: maximum rates with byte-rate scheduling.*
- **Wire-speed logical multicasting.**
  - *Four classes of service.*
  - *Programmable service rate (minimum and excess bandwidth distribution).*
  - *Programmable thresholds.*
  - *Branch connections can be added and deleted during live traffic.*
  - *Traffic management features on all multicast roots and branches.*
- **Multicast label generation for spatial multicast support.**
- **Integrated wire-speed AAL-5 segmentation and reassembly (AAL-5 CPCS SAR) in the datapath.**
- **32-bit processor interface running at up to 66 MHz with**

[1] External logic may be required if using a SPI4.2 channel configuration that is not a power-of-2. Refer to Operation with Unsupported SPI-4 Channel Configuration on page 11-6 in Chapter 11 of the 89TTM55x User Manual, available by contacting IDT.

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integrated AAL-5 SAR and DMA engine for data insertion and extraction.

- *Four classes of service.*
- *Integrated AAL-5-compliant and packet-based SAR.*
- *Programmable service rate.*
- *Programmable queue thresholds.*
- *Use of descriptors and DMA support for maximum performance.*
- *32-bit data bus transfer at up to 66 MHz.*

- **Algorithms implemented in hardware; software intervention required for initialization and configuration only.**
- **Error protection on all external RAM and BIST on all internal RAM.**
- **Inter-operable with the IDT ZTM200 traffic manager.**

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89TTM55x Diagrams

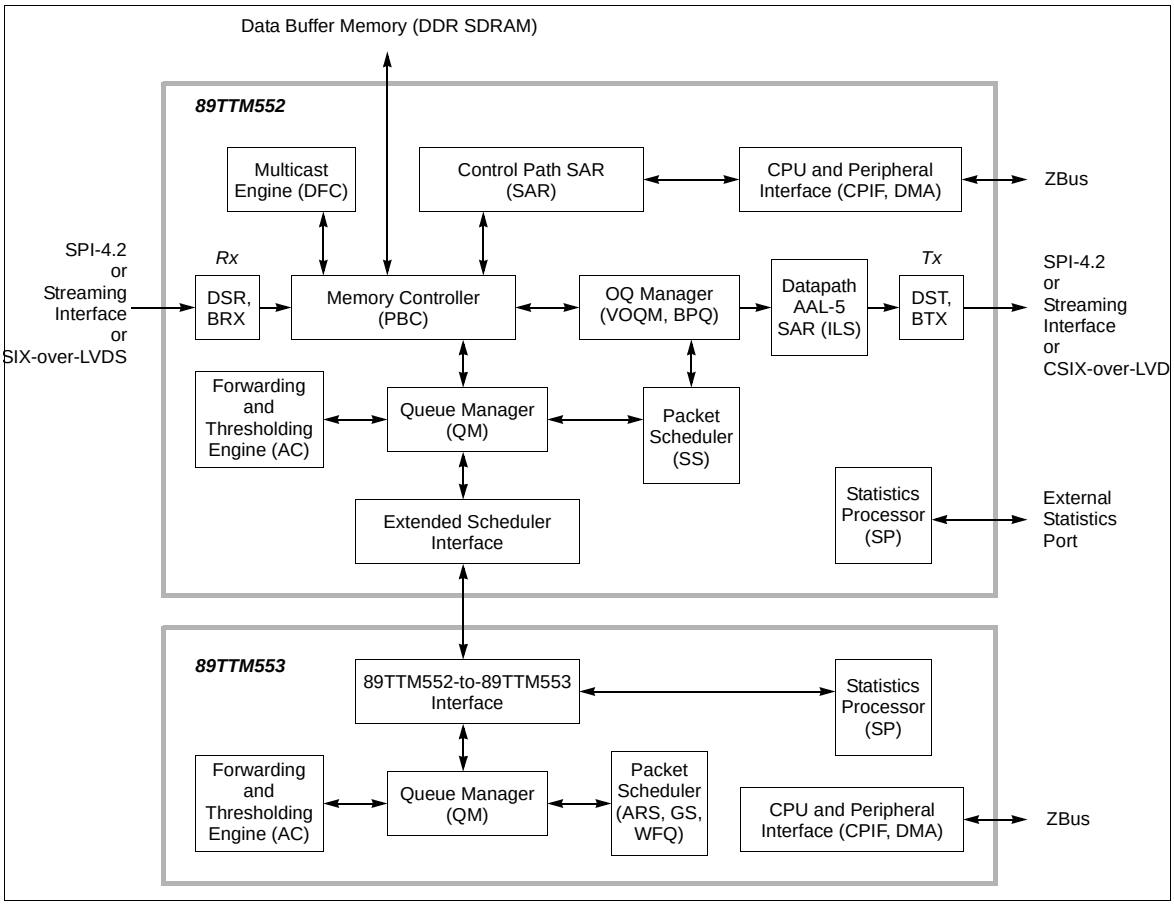

Figure 1 89TTM55x Functional Block Diagram

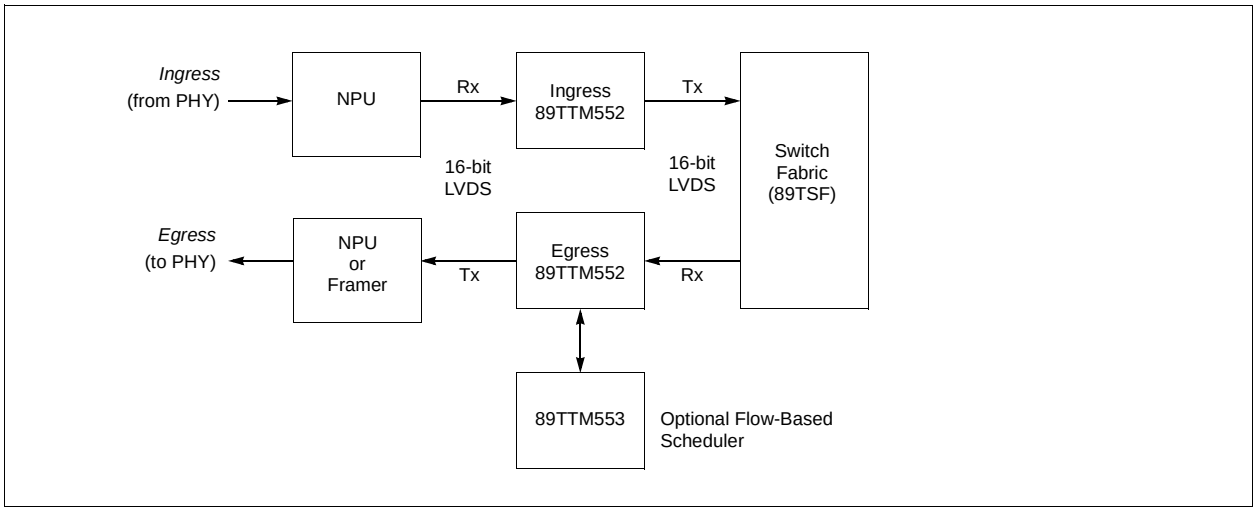

Figure 2 Example of a Full-duplex 10 Gbps System Configuration

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89TTM552 Pin Description

Note: Information in this section is subject to change. Contact your IDT FAE before making design decisions.

In this data sheet, direction is indicated as follows: I for In, O for Out, B for Bidirectional, and P for power.

Signal Name	I/O Type	Dir.[1]	Freq.	Remarks
FLQS_DIN[21:0], FLQS_DIN_PRTY	1.5V HSTL Class 1	I	175 MHz	'External scheduler control in' serial interface (22 signal lines + 1 parity line)
FLQS_CLKIN	1.5V HSTL Class 1	I	175 MHz	External scheduler clock in
FLQS_TIC_IN	1.5V HSTL Class 1	I	33.33 MHz	External scheduler cell time tick in
FLQS_DOUT[17:0], FLQS_DOUT_PRTY	1.5V HSTL Class 1	O	175 MHz	'External scheduler control out' serial interface (18 signal lines + 1 parity line)
FLQS_CLKOUT	1.5V HSTL Class 1	O	175 MHz	External scheduler clock out
FLQS_TIC_OUT	1.5V HSTL Class 1	O	33.33 MHz	External scheduler cell time tick out
FLQS_VREF[1:0]	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 1 89TTM552 / 89TTM553 "External Flow Scheduler" Control Interface[2]

1. The 89TTM553 shares these lines, and the I/O direction is, of course, the opposite of these.

2. These lines multiplex many logical signals over 5 clocks.

Signal Name	I/O Type	Dir.	Freq.	Remarks
PP_D, PP_PRTY	1.5V HSTL Class 1	I	175 MHz	Protocol processor data and parity from external protocol processor device
PP_CLK	1.5V HSTL Class 1	I	175 MHz	Source-synchronous protocol processor port clock from external protocol processor device
PP_TIC	1.5V HSTL Class 1	I	33.33 MHz	Protocol processor port cell time tick from external protocol processor device
PP_VREF	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 1 External Protocol Processor Port Interface

The 89TTM552 operates the BRx and BTX interfaces with LVDS. The flexible interface can operates in either SPI-4.2, CSIX-over-LVDS, or NPF SI modes. The NPU/system receive interface has 16-bit data, 4-bit status for LVDS and 2-bit status for LVTTL.

Signal Name	I/O Type	Dir.	Freq.	Remarks
RX_CLKP, RX_CLKN	LVDS[1]	I	500 MHz	Rx data clock
RX_SOFP, RX_SOFN	LVDS	I	500 MHz	Rx control input
RX_DP[15:0], RX_DN[15:0]	LVDS	I	500 MHz	Rx data bus input (16-bit)
RX_PRTYP, RX_PRTYN	LVDS	I	500 MHz	Rx parity over Rx data bus
RX_STAT_CLKP, RX_STAT_CLKN	LVDS	O	500 MHz	Rx status clock output

Table 2 Receive Traffic Interface (BRx) (Part 1 of 2)

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Signal Name	I/O Type	Dir.	Freq.	Remarks
RX_STAT_SOFP, RX_STAT_SOFN	LVDS	O	500 MHz	Rx status control output
RX_STAT_DP[3:0], RX_STAT_DN[3:0]	LVDS	O	500MHz	Rx status bus output
RX_STAT_PRTYP, RX_STAT_PRTYN	LVDS	O	500 MHz	Rx status parity over Rx status bus
RX_SPI4_STAT_CLK	3.3V LVTTL, 16mA drive	O	1/4 of 500 MHz	Rx SPI-4 status clock
RX_SPI4_STAT_D[1:0]	3.3V LVTTL, 16mA drive	O	—	Rx SPI-4 status outputs
RX_VREF[1:0]	1.25V	—	—	Reference voltage for LVDS transmitter termination voltage. Nominally set at 1.25V

Table 2 Receive Traffic Interface (BRx) (Part 2 of 2)

1. Note that the PIC buffer interface requires a 2.6V power supply. That means, separate power supplies are needed for the NPU/System Rx & Tx (LVDS) interfaces and the PIC buffer (SSTL2) interface.

The BTx transmit interface has 16-bit data, 4-bit status for LVDS and 2-bit status for LVTTL.

Signal Name	I/O Type	Dir.	Freq.	Remarks
TX_CLKP, TX_CLKN	LVDS[1]	O	500 MHz	Tx data clock
TX_SOFP, TX_SOFN	LVDS	O	500 MHz	Tx control output
TX_DP[15:0], TX_DN[15:0]	LVDS	O	500 MHz	Tx data bus output (16-bit)
TX_PRTYP, TX_PRTYN	LVDS	O	500 MHz	Tx parity over Tx data bus
TX_STAT_CLKP, TX_STAT_CLKN	LVDS	I	500 MHz	Tx status clock input
TX_STAT_SOFP, TX_STAT_SOFN	LVDS	I	500 MHz	Tx status control input
TX_STAT_DP[3:0], TX_STAT_DN[3:0]	LVDS	I	500 MHz	Tx status bus input
TX_STAT_PRTYP, TX_STAT_PRTYN	LVDS	I	500 MHz	Tx status parity over Tx status bus
TX_SPI4_STAT_CLK	3.3V LVTTL, 100K internal pullup	I	125 MHz	Tx SPI-4 status clock (1/4 of 500 MHz)
TX_SPI4_STAT_D[1:0]	3.3V LVTTL, 100K internal pullup	I	—	Tx SPI-4 status input
TX_VREF[5:0]	1.25V	—	—	Reference voltage for LVDS transmitter termination voltage. Nominally set at 1.25V

Table 3 Transmit Traffic Interface (BTx)

1. Note that the PIC buffer interface requires a 2.6V power supply. That means, separate power supplies are needed for the NPU/System Rx & Tx (LVDS) interfaces and the PIC buffer (SSTL2) interface.

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Signal Name	I/O Type	Dir.	Freq.	Remarks
LLST_CLK_CP (C), LLST_CLK_CN (C#)	1.5V HSTL Class 1	I	175 MHz	LL QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
LLST_CLK_KP (K), LLST_CLK_KN (K#)	1.5V HSTL Class 1	O	175 MHz	LL QDR SRAM output clock: This clock pair times the address and control outputs to the rising edge of K, and times the data outputs on the rising edge of K and K#.
LLST_ADDR[21:0]	1.5V HSTL Class 1	O	175 MHz	LL QDR SRAM address outputs:
LLST_RD_N	1.5V HSTL Class 1	O	175 MHz	LL QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
LLST_WR_N	1.5V HSTL Class 1	O	175 MHz	LL QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
LLST_DIN[17:0]	1.5V HSTL Class 1	I	175 MHz	LL QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations
LLST_DOUT[17:0]	1.5V HSTL Class 1	O	175 MHz	LL QDR SRAM data outputs: Output data is synchronized to the K and K# during write operations
LLST_VREF[1:0]	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 4 Linked-List QDR SRAM

Signal Name	I/O Type	Dir.	Freq.	Remarks
MC_CLK_CP (C), MC_CLK_CN (C#)	1.5V HSTL Class 1	I	175 MHz	MC QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
MC_CLK_KP (K), MC_CLK_KN (K#)	1.5V HSTL Class 1	O	175 MHz	MC QDR SRAM output clock: This clock pair times the address and control outputs to the rising edge of K, and times the data outputs on the rising edge of K and K#.
MC_ADDR[21:0]	1.5V HSTL Class 1	O	175 MHz	MC QDR SRAM address outputs:
MC_RD_N	1.5V HSTL Class 1	O	175 MHz	MC QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
MC_WR_N	1.5V HSTL Class 1	O	175 MHz	MC QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
MC_DIN[17:0]	1.5V HSTL Class 1	I	175 MHz	MC QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations

Table 5 Multicast / Parent-Child QDR SRAM (Part 1 of 2)

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Signal Name	I/O Type	Dir.	Freq.	Remarks
MC_DOUT[17:0]	1.5V HSTL Class 1	O	175 MHz	MC QDR SRAM data outputs: Output data is synchronized to the K and K# during write operations
MC_BW_N[1:0]	1.5V HSTL Class 1	O	175 MHz	MC QDR SRAM byte write enable: This is used with MC_WR_N when writing to the QDR SRAM. By using these byte write enable signals, MC logic can write to half of a QDR RAM entry when programming the logical multicast branch table. MC_BW_N[0] controls MC_DOUT[8:0]. MC_BW_N[1] controls MC_DOUT[17:9].
MC_VREF[1:0]	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 5 Multicast / Parent-Child QDR SRAM (Part 2 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
SAR_CLK_CP (C), SAR_CLK_CN (C#)	1.5V HSTL Class 1	I	175 MHz	ILS QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
SAR_CLK_KP (K), SAR_CLK_KN (K#)	1.5V HSTL Class 1	O	175 MHz	ILS QDR SRAM output clock: This clock pair times the address and control outputs to the rising edge of K, and times the data outputs on the rising edge of K and K#.
SAR_ADDR[21:0]	1.5V HSTL Class 1	O	175 MHz	ILS QDR SRAM address outputs:
SAR_RD_N	1.5V HSTL Class 1	O	175 MHz	ILS QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
SAR_WR_N	1.5V HSTL Class 1	O	175 MHz	ILS QDR SRAM synchronous write output (active low): WHen asserted, a write cycle is initiated to the external QDR SRAM devices.
SAR_DIN[8:0]	1.5V HSTL Class 1	I	175 MHz	ILS QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations
SAR_DOUT[8:0]	1.5V HSTL Class 1	O	175 MHz	ILS QDR SRAM data outputs: Output data is synchronized to the K and K# during write operations
SAR_VREF	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 6 In-Line SAR (ILS) QDR SRAM

Signal Name	I/O Type	Dir.	Freq.	Remarks
DRAM_CLKP[2:0]	2.6V SSTL2 CMOS[1]	O	175 MHz	DRAM clock, group 0 & group 1 Important: See the footnote.
DRAM_CLKN[2:0]	2.6V SSTL2 CMOS	O	175 MHz	DRAM $\overline{\text{clock}}$ (“clock bar”)
DRAM0_ADDR[12:0]	2.6V SSTL2 CMOS	O	175 MHz	Group 0 SDRAM address
DRAM0_BNK[1:0]	2.6V SSTL2 CMOS	O	175 MHz	Group 0 SDRAM bank address
DRAM0_CAS_N	2.6V SSTL2 CMOS	O	175 MHz	Group 0 column address strobe (active low)

Table 7 PIC Buffer (DDR SDRAM) (Part 1 of 2)

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Signal Name	I/O Type	Dir.	Freq.	Remarks
DRAM0_CKE	2.6V SSTL2 CMOS	O	—	Group 0 clock enable
DRAM0_CS_N	2.6V SSTL2 CMOS	O	—	Group 0 chip select (active low)
DRAM0_D[71:0]	2.6V SSTL2 CMOS	B	175 MHz	Group 0 data
DDAM0_DQS[8:0]	2.6V SSTL2 CMOS	B	175 MHz	Group 0 DDR data strobes: Output with write data, input with read data
DRAM0_RAS_N	2.6V SSTL2 CMOS	O	175 MHz	Group 0 row address strobe (active low)
DRAM0_WE_N	2.6V SSTL2 CMOS	O	—	Group 0 write enable (active low)
DRAM1_ADDR[12:0]	2.6V SSTL2 CMOS	O	175 MHz	Group 1 SDRAM address
DRAM1_BNK[1:0]	2.6V SSTL2 CMOS	O	175 MHz	Group 1 SDRAM bank address
DRAM1_CAS_N	2.6V SSTL2 CMOS	O	175 MHz	Group 1 column address strobe (active low)
DRAM1_CKE	2.6V SSTL2 CMOS	O	—	Group 1 clock enable
DRAM1_CS_N	2.6V SSTL2 CMOS	O	—	Group 1 chip select (active low)
DRAM1_D[71:0]	2.6V SSTL2 CMOS	B	175 MHz	Group 1 data
DDAM1_DQS[8:0]	2.6V SSTL2 CMOS	B	175 MHz	Group 1 DDR data strobes: Output with write data, input with read data
DRAM1_RAS_N	2.6V SSTL2 CMOS	O	175 MHz	Group 1 row address strobe (active low)
DRAM1_WE_N	2.6V SSTL2 CMOS	O	—	Group 1 write enable (active low)
DRAM_VREF[7:0]	1.3V	I	—	SSTL_2 reference voltage. Connect to (Vddq/2) 1.3 volts.

Table 7 PIC Buffer (DDR SDRAM) (Part 2 of 2)

1. Note that the PIC buffer interface requires a 2.6V power supply. That means, separate power supplies are needed for the NPU/System Rx & Tx (LVDS) interfaces and the PIC buffer (SSTL2) interface.

Signal Name	I/O Type	Dir.	Freq.	Remarks
STAT_ARR[17:0], STAT_ARR_PRTY	1.5V HSTL Class 1	O	175 MHz	Arrival statistics port data and parity
STAT_DEP[12:0], STAT_DEP_PRTY	1.5V HSTL Class 1	O	175 MHz	Departure statistics port data and parity
STAT_CLK	1.5V HSTL Class 1	O	175 MHz	Source-synchronous statistic port clock to external statistic controller device
STAT_TIC	1.5V HSTL Class 1	O	175 / 5 MHz	Statistic port cell time tick to external statistic controller device
STAT_VREF	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 8 Statistics Interface

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Signal Name	I/O Type	Dir.	Freq.	Remarks
ZBUS_CLK	3.3V, no internal pullup	I	33 or 66 MHz	ZBus clock input (up to 66 MHz)
ZBUS_GNT_N	3.3V, 100K internal pullup	I	33 or 66 MHz	ZBus grant (active low)
ZBUS_DEVID[4:0]	3.3V, 100K internal pullup	B	33 or 66 MHz	Used for ZBus device identification
ZBUS_INT_N[2:0]	3.3V, 16 mA drive	O	33 or 66 MHz	ZBus device interrupt (active low)
ZBUS_DIR	3.3V, 16 mA drive	O	33 or 66 MHz	ZBus write/read flag
ZBUS_REQ_N	3.3V, 16 mA drive	O	33 or 66 MHz	ZBus master cycle request (active low)
ZBUS_AD[31:0]	3.3V LVTTL, 16mA drive, 100K internal pullup	B	33 or 66 MHz	ZBus 32-bit multiplexed address/data bus
ZBUS_PRTY[1:0]	3.3V LVTTL, 16mA drive, 100K internal pullup	B	33 or 66 MHz	ZBus parity over address/data; one parity bit for 16 bits
ZBUS_AVALID_N	3.3V LVTTL, 16mA drive, 100K internal pullup	B	33 or 66 MHz	ZBus address valid flag (active low)
ZBUS_DVALID_N	3.3V LVTTL, 16mA drive, 100K internal pullup	B	33 or 66 MHz	ZBus data valid flag (active low)

Table 9 Processor Interface (ZBus)

Signal Name	I/O Type	Dir.	Freq.	Remarks
PLL_RST	3.3V, 100K internal pulldown	I	—	PLL reset. A special initialization sequence is required.
PLL_DIV_RST	3.3V, 100K internal pulldown	I	—	PLL post-divider reset. A special initialization sequence is required.
PLL_CFG_OVR	3.3V, 100K internal pulldown	I	—	PLL latch-on-reset override input. When **high**, the PLLs' configurations can be latched through ZBUS_AD when RESET_N deactivates. A special initialization sequence is required.
PLL_SYS_REFCLK	3.3V	I	100 MHz	Chip core PLL reference clock.
PLL_DDR_BYPCLK	3.3V, 100K internal pullup	I	—	Core DDR bypass clock source. *For IDT use only. Do not connect.*
PLL_SYS_LCK	3.3V, 16mA drive	O	—	Core PLL VCO lock indicator. *For IDT use only. Do not connect.*
PLL_SYS_MON	3.3V, 16mA drive	O	—	Core PLL clock monitor output. *For IDT use only. Do not connect.*
PLL_RX_REFCLK		I	100 MHz	SPI4 Rx PLL reference clock

Table 10 PLL (Part 1 of 2)

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Signal Name	I/O Type	Dir.	Freq.	Remarks
PLL_RX_LCK	3.3V, 16mA drive	O	—	SPI4 Rx PLL VCO lock indicator. For IDT use only. Do not connect.
PLL_RX_RST	3.3V 100K internal pulldown	I	—	SPI4 Rx PLL reset/powerdown. Tie inactive when using register-based (i.e., non-LOR) DSX PLL configuration.
PLL_TX_REFCLK		I	100 MHz	SPI4 Tx PLL reference clock.
PLL_TX_LCK	3.3V, 16mA drive	O	—	SPI4 Tx PLL VCO lock indicator. For IDT use only. Do not connect.
PLL_TX_RST	3.3V 100K internal pulldown	I	—	SPI4 Tx PLL reset/powerdown. Tie inactive when using register-based (i.e., non-LOR) DSX PLL configuration.

Table 10 PLL (Part 2 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
SCAN_MODE_N	3.3V, 100K internal pullup	I	—	Scan mode input (active low). *For IDT use only. Do not connect.*
SCAN_SHIFT_N	3.3V, 100K internal pullup	I	—	Scan shift input (active low). *For IDT use only. Do not connect.*
TCK	3.3V, 100K internal pullup	I	—	JTAG (IEEE 1149.1) clock input.
TDI	3.3V, 100K internal pullup	I	—	JTAG (IEEE 1149.1) test data input.
TDO	3.3V, 100K internal pullup	O	—	JTAG (IEEE 1149.1) test data output.
TMS	3.3V, 100K internal pullup	I	—	JTAG (IEEE 1149.1) test mode select
TRST_N	3.3V, 100K internal pullup	I	—	JTAG (IEEE 1149.1) test reset input. (If JTAG is used, and JTAG pins are being driven by some logic, we recommend driving trstn_i low whenever JTAG is not in operation. If JTAG is not used, trstn_i can be permanently tied low.

Table 11 Test and Debug

Signal Name	I/O Type	Dir.	Freq.	Remarks
RESET_N	3.3V, 100K internal pullup	I	Async	Chip reset input (active low)
IDDQ_N	3.3V, no internal pullup	I	N/A	IDDQ input (active low). Attach to a 4.7K resistor to 3.3V.
TURBO_DATA[3:0]	3.3V, 16mA drive	O	175/2 MHz	89TTM552 to 89TSF502 “turbo mode” interface
TURBO_CLK	3.3V, 16mA drive	O	175/2 MHz	Source-synchronous turbo mode clock to the 89TSF502
VDD15	—	P	—	1.5V I/O power for HSTL-2 I/Os: Isolated output buffer supply set nominally to 1.5V

Table 12 Miscellaneous Signals (Part 1 of 2)

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Signal Name	I/O Type	Dir.	Freq.	Remarks
VDD18	—	P	—	1.8V core power
VDD26	—	P	—	2.6V I/O power for SSTL2 I/Os: Isolated output buffer supply set nominally to 2.6V
VDD33	—	P	—	3.3V I/O power for LVTTL I/Os
VDD33(VDDP)	—	P	—	3.3V LVDS receiver power
VDDO_25V_LVDS_DSR	—	P	—	2.5V I/O power for DSR LVDS I/Os
VDDO_25V_LVDS_DST	—	P	—	2.5V I/O power for DST LVDS I/Os
GND	—	P	—	Ground
PLL_TX_VSSA	—	P	—	3.3V analog ground for Tx LVDS PLLs
PLL_TX_VDDA	—	P	—	3.3V analog power for Tx LVDS PLLs
PLL_TX_VDD	—	P	—	1.8V digital power for Tx LVDS PLLs
PLL_RX_VSSA	—	P	—	3.3V analog ground for Rx LVDS PLLs
PLL_RX_VDDA	—	P	—	3.3V analog power for Rx LVDS PLLs
PLL_RX_VDD	—	P	—	1.8V digital power for Rx LVDS PLLs
PLL_SYS_VSSA	—	P	—	3.3V analog ground for core clock PLL
PLL_SYS_VDDA	—	P	—	3.3V analog power for core clock PLL
PLL_SYS_VDD	—	P	—	1.8V digital power for core clock PLL

Table 12 Miscellaneous Signals (Part 2 of 2)

89TTM552 Electrical Specifications

Some data are TBD and will be published as they become available.

The specifications are subject to change without notice.

Absolute Maximum Ratings

The absolute maximum ratings are the maximum conditions that the device can withstand without sustaining permanent damage. Exceeding any of these conditions could result in permanent damage to the device. Normal operation should not be expected at these conditions. In addition, exposure to absolute maximum rated conditions (or near absolute maximum rated conditions) for extended periods may affect device reliability.

Operation of the device is not guaranteed at the absolute maximum ratings, but rather at the operating conditions outlined in DC Characteristics on page 1-13 and AC Characteristics on page 1-15.

Symbol	Parameter	Min	Max	Units	Conditions
T_{JMAX}	Junction temperature under bias		105	°C	
$T_{STORAGE}$	Storage temperature		150	°C	
	Storage temperature range	–40	85	°C	Long term storage
T_{SOLDER}	Soldering temperature		215	°C	
T_{REWORK}	Rework temperature		204	°C	

Table 13 Absolute Maximum Ratings

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Operating Ranges

Symbol	Parameter	Min	Typical	Max	Units	Conditions
T_J	Operating junction temperature range	0	—	85	°C	
I_{V15}	Input current for 1.5V power supply	—	700	—	mA	
I_{V18}	Input current for 1.8V power supply	—	3.8	—	A	
I_{V25}	Input current for 2.5V power supply	—	400	—	mA	
I_{V26}	Input current for 2.6V power supply	—	600	—	mA	
I_{V33}	Input current for 3.3V power supply	—	100	—	mA	
VDD_{15}	1.5V HSTL supply	1.425	1.5	1.575	V	±5%
VDD_{18}	1.8V Core supply	1.71	1.8	1.89	V	±5%
VDDO_25V_LVDS (DSR and DST)	2.5V LVDS supply	2.375	2.5	2.625	V	±5%
VDD_{26}	2.6V SSTL supply	2.47	2.6	2.73	V	±5%
VDD_{33}	3.3V LVTTL supply	3.135	3.3	3.465	V	±5%
VRF_{LVDS}[1]	1.25V LVDS reference voltage	1.1875	1.25	1.3125	V	±5%
VRF_{HSTL}[2]	0.75V HSTL reference voltage	0.7125	0.75	0.7875	V	±5%
VRF_{SSTL}[3]	1.25V SSTL reference voltage	1.235	1.3	1.365	V	±5%
Power Dissipation		—	10.78	11.32	W	Max. values use the maximum voltages and current listed in this table and typical values use the typical voltages and current.

Table 14 Operating Ranges

1. This operating range applies to the following pins: RX_VREF0, RX_VREF1, TX_VREF0, TX_VREF1, TX_VREF2, TX_VREF3, TX_VREF4, TX_VREF
2. This operating range applies to the following pins: SAR_VREF, LLST_VREF0, LLST_VREF1, FLQS_VREF0, FLQS_VREF1, MC_VREF0, MC_VREF1, PP_VREF, STAT_VREF
3. This operating range applies to the following pins: DRAM_VREF0, DRAM_VREF1, DRAM_VREF2, DRAM_VREF3, DRAM_VREF4, DRAM_VREF5, DRAM_VREF6, DRAM_VREF7

DC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 14.

Symbol	Parameter	Min	Typical	Max	Conditions
V_{ILHSTL} (1.5v HSTL)	Input low voltage for 1.5V HSTL inputs (VREF = 0.75V)	—	VREF – 0.1	V	
V_{IHHSTL} (1.5v HSTL)	Input high voltage for 1.5V HSTL inputs (VREF = 0.75V, VDDQ = 1.5V)	VREF+ 0.1	VDDQ+0.3	V	
V_{ILSSTL} (2.5v SSTL/ CMOS)	Input low voltage for 2.5V SSTL/CMOS inputs (VREF = 1.25V)	—	VREF – 0.18	V	
V_{IHSSTL} (2.5v SSTL/ CMOS)	Input high voltage for 2.5V SSTL/CMOS inputs (VREF = 1.25V)	VREF + 0.18	—	V	

Table 15 DC Parameters (Part 1 of 2)

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Symbol	Parameter	Min	Typical	Max	Conditions
V_{IL33} (3.3v LVTTL)	Input low voltage for 3.3V LVTTL inputs	—	0.8	V	
V_{IH33} (3.3v LVTTL)	Input high voltage for 3.3V LVTTL inputs	2.0	—	V	
V_{OLHSTL}	Output low voltage for 1.5V HSTL outputs	—	0.4	V	1.5v HSTL classI w/8mA Drive)
V_{OHHSTL}	Output high voltage for 1.5V HSTL outputs (VDDQ = 1.5V)	VDDQ-0.4	—	V	1.5v HSTL classI w/ 8mA Drive)
V_{OLSSTL}	Output low voltage for 2.5V SSTL/CMOS outputs	—	0.54	V	2.5v SSTL classII w/15.2mA Drive
V_{OHSSTL}	Output high voltage for 2.5V SSTL/CMOS outputs	1.90	—	V	2.5v SSTL classII w/15.2mA Drive
V_{OL33}	Output low voltage for 3.3V CMOS outputs (16mA pads)	—	0.5	V	3.3v LVTTL w/ 16mA Drive
V_{OH33}	Output high voltage for 3.3V CMOS outputs (16mA pads)	2.4	—	V	3.3v LVTTL w/ 16mA Drive
I_{ILHSTL} (1.5v HSTL)	Input Leakage low current for 1.5V HSTL Inputs	-10	10	uA	
I_{IHHSTL} (1.5v HSTL)	Input Leakage high current for 1.5V HSTL Inputs	-10	10	uA	
I_{ILSSTL} (2.5v SSTL)	Input Leakage low current for SSTL Inputs	-10	10	uA	
I_{IHSSTL} (2.5v SSTL)	Input Leakage high current for SSTL Inputs	-10	10	uA	
I_{IL33} (3.3v pads w/o Pull Up/Down)	Input Leakage low current for 3.3V Inputs	-10	10	uA	
I_{IH33} (3.3v pads w/o Pull Up/Down)	Input Leakage high current for 3.3V Inputs	-10	10	uA	
I_{IL33PU} (3.3v pads w/ Pull Up)	Input Leakage low current for 3.3V with Pull-Up Inputs	-200	-10	uA	
I_{IH33PU} (3.3v pads w/ Pull Up)	Input Leakage high current for 3.3V with Pull-Up Inputs	-10	+10	uA	
I_{IL33PD} (3.3v pads w/ Pull Down)	Input Leakage low current for 3.3V with Pull-Down Inputs	-10	+10	uA	
I_{IH33PD} (3.3v pads w/ Pull Down)	Input Leakage high current for 3.3V with Pull-Down Inputs	10	200	uA	

Table 15 DC Parameters (Part 2 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Conditions
V_I	Input voltage range, V_{IA} or V_{IB}	0	—	2400	mV	$\|V_{GPD}\| < 925$ mV [1]
V_{IDTH}	Input differential threshold	–100	—	+100	mV	$\|V_{GPD}\| < 925$ mV
V_{HYST}	Input differential hysteresis	25	—	—	mV	
R_{IN}	Receiver differential input impedance	80	98	120	Ω	
V_{OH}	Output voltage high, V_{OA} or V_{OB}	—	—	1475	mV	R_{LOAD} = 100 Ω ±1%

Table 16 LVDS DC Parameters (Part 1 of 2)

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Symbol	Parameter	Min	Typical	Max	Units	Conditions
V_{OL}	Output voltage low, V_{OA} or V_{OB}	925	—	—	mV	R_{LOAD} = 100 Ω ±1%
$\|V_{OD}\|$	Output differential voltage	250	—	400	mV	R_{LOAD} = 100 Ω ±1%
V_{OS}	Output offset voltage	1125	—	1275	mV	R_{LOAD} = 100 Ω ±1%
$\|DV_{OD}\|$	Change in $\|V_{OD}\|$ between ‘0’ and ‘1’	—	—	25	mV	R_{LOAD} = 100 Ω ±1%
DV_{OS}	Change in V_{OS} between ‘0’ and ‘1’	—	—	25	mV	R_{LOAD} = 100 Ω ±1%
I_{SA}, I_{SB}	Output current	—	—	40	mA	Driver shorted to ground
I_{SAB}	Output current	—	—	12	mA	Drivers shorted together

Table 16 LVDS DC Parameters (Part 2 of 2)

1. V_{GPD} is the ground potential difference between the transmitter and the receiver

AC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 14.

Symbol	Parameter	Min	Typical	Max	Units
f_{SYS}	Frequency for system (core) clock reference	—	100	—	MHz
T_{JSYS}	Jitter requirements for system clock	—	—	80	ps
D_{SYS}	Percentage duty for system clock	45	50	55	%
f_{TX}	Frequency for transmit clock reference	75	100	125	MHz
T_{JTX}	Jitter requirement for transmit clock reference	—	—	50[1]	ps, pk-pk
D_{DTX}	Percentage duty for transmit clock reference	40	50	60	%
f_{RX}	Frequency for receive clock reference	75	100	125	MHz
T_{JRX}	Jitter requirement for receive clock reference	—	—	50[1]	ps, pk-pk
D_{RX}	Percentage duty for receive clock reference	40	—	60	%
f_{ZB}	Frequency for ZBus clock	33	33	66	MHz
D_{ZB}	Percentage duty for ZBus clock	45	50	55	%

Table 17 System Clock Timing

1. Tight input jitter specifications are required to meet low frequency jitter specifications on the clock output. If low frequency output jitter performance is not required, this spec can be relaxed.

Symbol	Parameter	Min	Typical	Max	Units
T_{KQOV}	K/$\overline{K}$ rising edge to address/data output valid	—	—	1.6[1]	ns
T_{KQOX}	K/$\overline{K}$ rising edge to address/data output invalid	0.8[1]	—	—	ns
T_{CQIS}	C/$\overline{C}$ rising edge to data input setup	–0.2	—	—	ns
T_{CQIH}	C/$\overline{C}$ rising edge to data input hold	—	—	1.6	ns

Table 18 QDR SSRAM Interface Timing

1. The parameter is specified at 89TTM55x core clock frequency of 175 MHz.

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Symbol	Parameter	Min	Typical	Max	Units
T_{SCQV}	Statistics clock to output valid	—	—	3.3[1]	ns
T_{SCQX}	Statistics clock to output invalid	2.3[1]	—	—	ns

Table 19 Statistics Interface Timing

1. The parameter is specified at 89TTM55x core clock frequency of 175 MHz.

Symbol	Parameter	Min	Typical	Max	Units
T_{DCAV}	DDR clock to address/control valid	—	—	4.5 [1]	ns
T_{DCAX}	DDR clock to address/control invalid	1.2[1]	—	—	ns
T_{DCQST}	DDR clock to DQS transition	-0.6	—	0.6	ns
T_{DCQSLZ}	DDR clock to DQS Low-Z	0	—	1.8	ns
T_{DCQSHZ}	DDR clock to DQS High-Z	0	—	1.8	ns
T_{DCQLZ}	DDR clock to DQ Low-Z	0	—	1.8	ns
T_{DCQHZ}	DDR clock to DQ High-Z	0	—	1.8	ns
T_{QSCQV}	DQS clock to DQ output valid	—	—	2.4[1]	ns
T_{QSCQX}	DQS clock to DQ output invalid	1.1[1]	—	—	ns
T_{QSCIS}	DQS clock to DQ input setup	–0.3	—	—	ns
T_{QSCIH}	DQS clock to DQ input hold	—	—	1.6	ns

Table 20 DDR Interface Timing

1. The parameter is specified at 89TTM55x core clock frequency of 175 MHz.

Symbol	Parameter	Min	Typical	Max	Units	Conditions
f_D	Output clock signal frequency	311	—	500	MHz	
D_{COC}	Output clock signal duty percentage	45	—	55	%	500 MHz
J_{CLK}	Output clock signal jitter	—	—	0.10	UI	500 MHz [1]
t_F	V_{OD} fall time, 80% to 20%	—	—	0.30	UI	T = 1ns R_{LOAD} = 100 Ω ± 1%
t_R	V_{OD} rise time, 20% to 80%	—	—	0.30	UI	T = 1ns R_{LOAD} = 100 Ω ± 1%
t_{SKEW1}	$\lvert t_{pHLA} - t_{pLHB} \rvert$ or $\lvert t_{pHLB} - t_{pLHA} \rvert$, Differential skew	—	—	50	ps	Any differential pair on package
t_{SKEW2}	$\lvert t_{pdiff[m]} - t_{pdiff[n]} \rvert$ Channel-to-channel skew	—	—	200	ps	Any 2 signals on package

Table 21 LVDS AC Parameters

1. Jitter is measured peak-to-peak from fclock/1000 to fclock. Low frequency jitter is determined by the jitter of the clock reference.

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Symbol	Parameter	Min	Typical	Max	Units	Conditions
f_S	Status channel clock frequency	75	—	125	MHz	
D_{COC}	Status clock duty percentage	40	—	60	%	
t_{SKEW}	Status clock to output data skew[1]		—	500	ps	
t_{SSCLK}	Status channel input setup time	2	—	—	ns	
t_{HSCLK}	Status channel input hold time	0	—	—	ns	

Table 22 SPI-4 LVTTL AC Parameters

1. Clock-data alignment is selectable in 1/4 cycle steps; skew is relative to this alignment

Symbol	Parameter	Min	Typical	Max	Units
T_{KQV}	Zbus clock high to output valid	—	—	8.3	ns
T_{KQX}	Zbus clock high to output invalid	2.5	—	—	ns
T_{KQLZ}	Zbus clock high to output low-Z	1.0	—	6.0	ns
T_{KQHZ}	Zbus clock high to output high-Z	1.0	—	6.0	ns
T_S	Input setup time from system clock	3.0	—	—	ns
T_H	Input hold time from system clock	0	—	—	ns

Table 23 Zbus Interface Timing

AC Test Conditions

Input Rise/Fall Time	1 V / ns (20% / 80%)
Output timing measurement reference level (V_{REF}) for 3.3V interfaces	(VDDQ/2) V
Output load	As shown in Figure 3

Table 24 AC Test Conditions

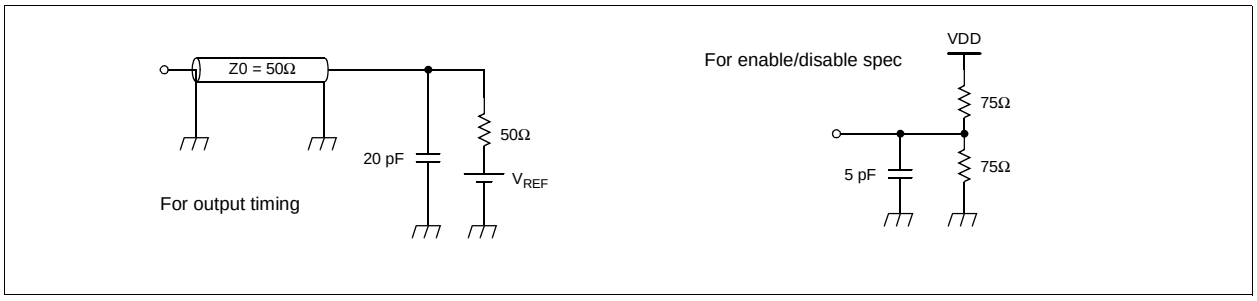

Figure 3 AC Test Load

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89TTM552 Thermal Considerations

This section describes the temperature and heat sink calculations for flip-chip BGA devices.

Symbol	Parameter	Value	Units	Conditions
$Ø_{JA}$	Thermal resistance, junction to ambient (no heat sink)	9.0	°C / W	Still air.
		5.5	°C / W	200 FPM.
		4.5	°C / W	500 FPM
$Ø_{JB}$	Estimated thermal resistance, junction to board	2.2	°C / W	
$Ø_{JC}$	Thermal resistance, junction to case	0.19	°C / W	

Table 25 89TTM552 Thermal Characteristics

The thermal circuit is as shown below.

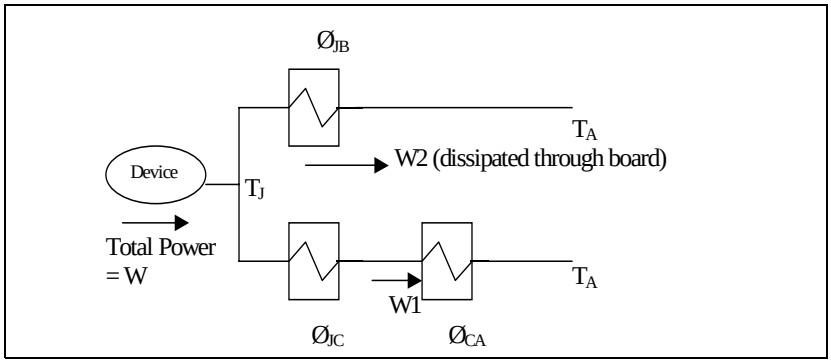

Figure 4 89TTM552 Thermal Circuit

For flip-chip BGA devices, there are two paths for heat dissipation: one through the package balls to the board and other through the package case to air. The device specifications provide $Ø_{JB}$ and $Ø_{JC}$ numbers. The $Ø_{CA}$ number comes from the heat sink manufacturer and depends on type of heat sink (area, height, fin type, etc.) and the airflow across the heat sink. The device specifications also provide the maximum operating junction temperature (T_J) that will not degrade the device reliability. The system designer should ensure that the device maximum junction temperature is not exceeded under any operating condition. One method of accomplishing this is to calculate the maximum ambient temperature (T_A) that can be tolerated based on the above device parameters. The formula is shown below.

$$T_A = T_J - W \times \frac{Ø_{JB} \times (Ø_{JC} + Ø_{CA})}{Ø_{JB} + Ø_{JC} + Ø_{CA}}$$

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The following graph depicts the ambient temperature (T_A) versus $Ø_{CA.}$

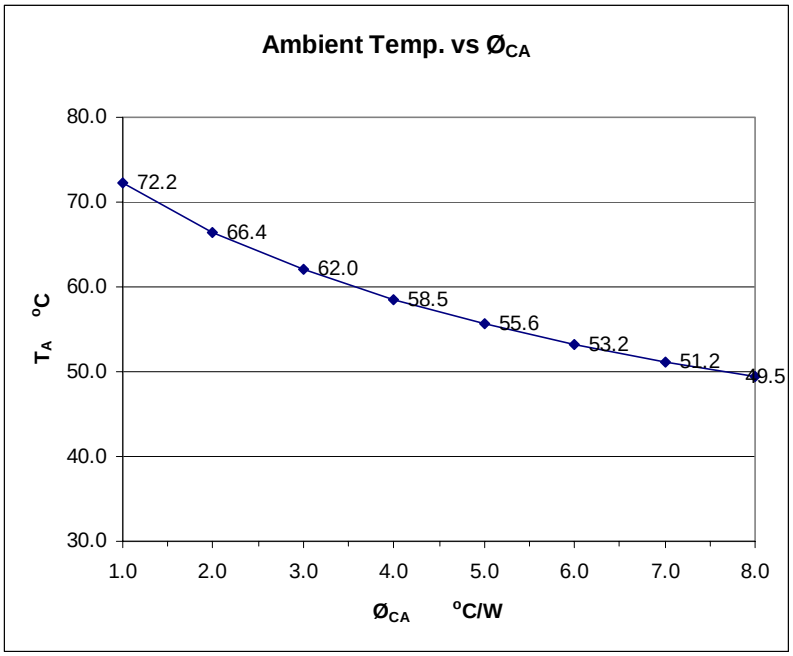

Figure 5 89TTM552 Ambient Temperature Curve

For system designers, specification of the maximum device junction temperature (operating) is critical, since it allows them to select a heat sink that meets the maximum ambient temperature requirements of their system.

The other parameter that is device package-specific is $Ø_{JA}$, without a heat sink, and is specified for various air-flow conditions. This is the intrinsic thermal resistance of the package (junction to case + case to ambient) and is mainly specified as a reference parameter. (This is when a heat sink is not present and the top surface of the package is essentially acting as the heat sink). However, in devices that have high power dissipation, heat sink usage is highly desirable. Consequently, system designers may have limited use for this parameter.

89TTM552 Reset Sequence

A PLL reset sequence must be followed when resetting the 89TTM552 to ensure that clocks are stable when the chip comes out of reset. This section describes the reset sequence for the 89TTM552 device.

The 89TTM552 uses data presented on the ZBus data and parity pins to determine the clock frequencies when the chip is in reset. The PLL_CFG_OVR pin controls this feature. When left high, the PLL will determine its clock frequency by sampling these values on the ZBus pins. The feature is not necessary if the default clock frequencies are desired. (The default frequency for the core clock is 133 MHz and 500 MHz for transmit and receive LVDS interfaces when a 100 MHz clock reference is used.) When default frequencies are desired, the PLL_CFG_OVR should be held low and it is not necessary to drive the ZBus data and parity lines during the reset.

Core, LVDS Receive and Transmit PLL Frequency Setting

The reset sequence is summarized as follows:

1. Assert chip reset.
2. Drive LOR (latch on reset) values on ZBus (described below) and enable configuration override on all PLLs. (Configuration override remains ON forever).
3. Reset PLLs.
4. Release reset on PLLs.
5. Release chip reset.
6. Release LOR value on ZBus.

The following values must be driven on ZBUS_AD[ ] and ZBUS_PRTY before the reset sequences in order to set the chip operation frequency properly. Note that the setting is based on a *100MHz* reference input clock (PLL_SYS_REFCLK pin).

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ZB_PRTY[1:0] = 0x3, must be driven “HIGH” for the entire reset sequence cycles

ZB_AD[31:0] = bits are set as:

		Core/system clock frequency
bit[12:0] =	0x154F =	187.50MHz
	0x1527 =	175.00MHz
	0x153a =	166.67MHz
	0x1526 =	150.00MHz
	0x1538 =	133.33MHz
	0x1525 =	125.00MHz

		LVDS RX clock frequency
bit[21:13] =	0x080 =	500.00MHz
	0x060 =	400.00MHz
	0x1C0 =	350.00MHz
	0x1A0 =	300.00MHz
	0x180 =	250.00MHz
	0x160 =	200.00MHz

		LVDS TX clock frequency
bit[30:22] =	0x080 =	500.00MHz
	0x060 =	400.00MHz
	0x1C0 =	350.00MHz
	0x1A0 =	300.00MHz
	0x180 =	250.00MHz
	0x160 =	200.00MHz

bit[31] = 0x1, keep “HIGH” for entire cycles

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Reset Sequence Timing Diagram

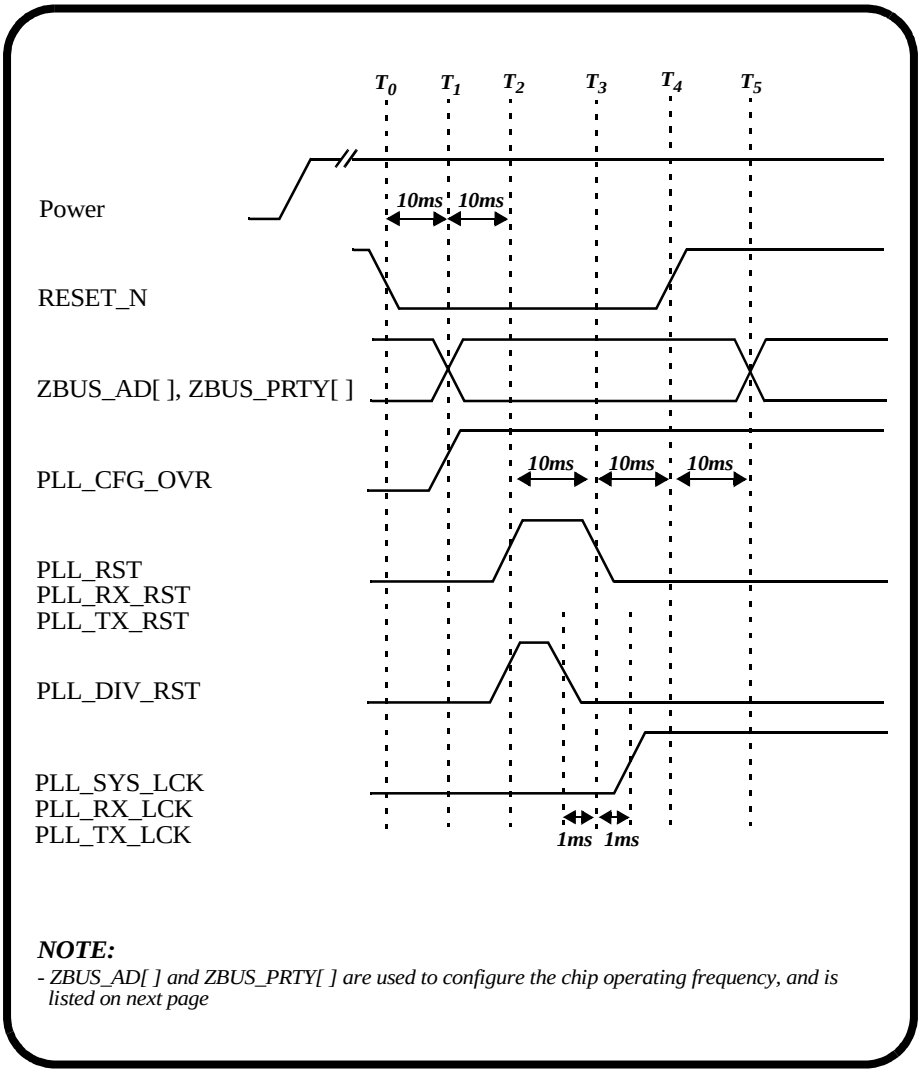

Figure 6 89TTM552 Reset Sequence Timing Diagram

Pin List I/O Description

The 89TTM552 Pin List on page 22 uses the following I/O notations:

I	Input
O	Output
B	Bidirectional
P	Power

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89TTM552 Pin List

Pin	Signal	Type
A2	FLQS_DIN12	I
A3	FLQS_DIN05	I
A4	FLQS_DIN09	I
A5	STAT_DEP09	O
A6	STAT_DEP06	O
A7	SAR_DIN08	I
A8	SAR_DIN05	I
A9	SAR_DIN02	I
A10	SAR_DOUT08	O
A11	SAR_DOUT05	O
A12	SAR_DOUT01	O
A13	SAR_WR_N	O
A14	SAR_RD_N	O
A15	SAR_ADDR16	O
A16	SAR_ADDR19	O
A17	SAR_ADDR13	O
A18	SAR_ADDR10	O
A19	SAR_ADDR09	O
A20	SAR_ADDR07	O
A21	SAR_ADDR03	O
A22	SAR_ADDR00	O
A23	LLST_ADDR10	O
A24	LLST_ADDR08	O
A25	VDD15	P
A26	VDD15	P
A27	MC_DOUT17	O
A28	VDD15	P
A29	MC_DOUT08	O
A30	MC_DOUT05	O
A31	MC_DOUT02	O
A32	MC_ADDR21	O
A33	MC_ADDR20	O
A34	MC_ADDR16	O
A35	VDD33(VDDP)	P
A36	TIC_1	O
A37	MC_ADDR09	O
B1	FLQS_DIN11	I
B2	FLQS_DIN10	I
B3	FLQS_DIN13	I
B4	FLQS_DIN04	I
B5	FLQS_DIN01	I
B6	STAT_DEP04	O
B7	SAR_DIN07	I
B8	SAR_DIN06	I
B9	SAR_DIN04	I
B10	SAR_DIN00	I
B11	SAR_DOUT07	O
B12	SAR_DOUT04	O
B13	SAR_DOUT00	O
B14	SAR_CLK_KP	O
B15	SAR_ADDR18	O
B16	SAR_ADDR15	O
B17	SAR_ADDR17	O
B18	SAR_ADDR11	O
B19	SAR_ADDR08	O
B20	SAR_ADDR04	O
B21	SAR_ADDR02	O
B22	LLST_ADDR12	O
B23	LLST_ADDR07	O
B24	GND	P
B25	GND	P
B26	GND	P
B27	GND	P
B28	GND	P
B29	GND	P
B30	GND	P
B31	GND	P
B32	GND	P
B33	GND	P
B34	GND	P
B35	TIC_2	O
B36	MC_ADDR14	O
B37	MC_ADDR12	O
C1	FLQS_DIN16	I
C2	FLQS_DIN14	I
C3	VDD15	P
C4	FLQS_DIN06	I
C5	FLQS_DIN03	I
C6	FLQS_DIN_PRTY	I
C7	FLQS_TIC_IN	I
C8	FLQS_CLKIN	I
C9	SAR_DIN03	I
C10	SAR_DIN01	I
C11	SAR_DOUT06	O
C12	SAR_DOUT03	O

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Pin	Signal	Type
C13	SAR_DOUT02	O
C14	SAR_CLK_KN	O
C15	SAR_ADDR20	O
C16	SAR_ADDR21	O
C17	SAR_ADDR14	O
C18	SAR_ADDR12	O
C19	SAR_ADDR06	O
C20	SAR_ADDR05	O
C21	SAR_ADDR01	O
C22	GND	P
C23	GND	P
C24	VDD15	P
C25	VDD15	P
C26	VDD33(VDDP)	P
C27	VDD15	P
C28	VDD15	P
C29	VDD15	P
C30	VDD33(VDDP)	P
C31	VDD33(VDDP)	P
C32	VDD33(VDDP)	P
C33	VDD15	P
C34	VDD15	P
C35	VDD33(VDDP)	P
C36	MC_ADDR11	O
C37	MC_ADDR10	O
D1	FLQS_DIN17	I
D2	FLQS_DIN15	I
D3	GND	P
D4	GND	P
D5	VDD33(VDDP)	P
D6	VDD33(VDDP)	P
D7	VDD15	P
D8	GND	P
D9	VDD15	P
D10	VDD33(VDDP)	P
D11	LLST_DIN08	I
D12	VDD15	P
D13	VDD33(VDDP)	P
D14	VDD33(VDDP)	P
D15	VDD15	P
D16	VDD15	P
D17	VDD15	P
D18	GND	P

Pin	Signal	Type
D19	VDD15	P
D20	VDD15	P
D21	VDD33(VDDP)	P
D22	VDD33(VDDP)	P
D23	VDD33(VDDP)	P
D24	GND	P
D25	GND	P
D26	GND	P
D27	GND	P
D28	GND	P
D29	GND	P
D30	GND	P
D31	GND	P
D32	GND	P
D33	GND	P
D34	VDD15	P
D35	VDD33(VDDP)	P
D36	MC_ADDR06	O
D37	MC_ADDR08	O
E1	FLQS_DIN18	I
E2	FLQS_DIN19	I
E3	FLQS_VREF0	P
E4	VDD15	P
E5	STAT_ARR11	O
E6	LLST_CLK_CN	I
E7	STAT_ARR09	O
E8	LLST_DIN14	I
E9	STAT_ARR02	O
E10	STAT_ARR00	O
E11	GND	P
E12	LLST_DIN06	I
E13	LLST_DIN04	I
E14	LLST_DOUT16	O
E15	LLST_DOUT15	O
E16	LLST_DIN00	I
E17	LLST_DOUT03	O
E18	LLST_DOUT09	O
E19	LLST_ADDR21	O
E20	LLST_ADDR17	O
E21	LLST_ADDR15	O
E22	LLST_ADDR11	O
E23	LLST_ADDR09	O
E24	LLST_ADDR05	O

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Pin	Signal	Type
E25	PP_VREF	P
E26	PP_D	I
E27	PP_CLK	I
E28	MC_CLK_KP	O
E29	MC_DOUT15	O
E30	MC_DOUT12	O
E31	MC_DOUT06	O
E32	MC_DOUT04	O
E33	MC_BW_N1	O
E34	GND	P
E35	GND	P
E36	MC_ADDR07	O
E37	MC_ADDR03	O
F1	FLQS_DIN20	I
F2	FLQS_DIN21	I
F3	FLQS_VREF1	P
F4	VDD15	P
F5	STAT_ARR16	O
F6	STAT_ARR14	O
F7	LLST_DIN16	I
F8	LLST_DIN17	I
F9	GND	P
F10	LLST_DIN12	I
F11	GND	P
F12	SAR_CLK_CN	I
F13	LLST_DIN07	I
F14	LLST_DOUT17	O
F15	LLST_DOUT12	O
F16	LLST_DOUT10	O
F17	LLST_DOUT04	O
F18	LLST_DOUT01	O
F19	LLST_ADDR18	O
F20	GND	P
F21	LLST_ADDR19	O
F22	LLST_ADDR16	O
F23	LLST_ADDR04	O
F24	LLST_ADDR03	O
F25	LLST_ADDR00	O
F26	PP_PRTY	I
F27	MC_RD_N	O
F28	MC_DOUT16	O
F29	MC_DOUT11	O
F30	MC_DOUT07	O

Pin	Signal	Type
F31	MC_DOUT01	O
F32	MC_ADDR18	O
F33	MC_ADDR15	O
F34	VDD15	P
F35	VDD33(VDDP)	P
F36	MC_ADDR02	O
F37	MC_ADDR01	O
G1	FLQS_DOUT16	O
G2	FLQS_DOUT_PRTY	O
G3	FLQS_DOUT17	O
G4	VDD15	P
G5	STAT_TIC	O
G6	FLQS_DIN08	I
G7	FLQS_DIN02	I
G8	STAT_ARR_PRTY	O
G9	STAT_ARR07	O
G10	LLST_DIN13	I
G11	LLST_DIN11	I
G12	STAT_ARR01	O
G13	LLST_CLK_KP	O
G14	LLST_DIN05	I
G15	LLST_DIN02	I
G16	LLST_DOUT11	O
G17	LLST_DOUT08	O
G18	LLST_DOUT02	O
G19	LLST_DOUT05	O
G20	LLST_ADDR20	O
G21	LLST_ADDR13	O
G22	LLST_ADDR14	O
G23	LLST_ADDR06	O
G24	LLST_ADDR02	O
G25	LLST_ADDR01	O
G26	PP_TIC	I
G27	MC_WR_N	O
G28	MC_DOUT14	O
G29	MC_DOUT09	O
G30	MC_DOUT03	O
G31	MC_BW_N0	O
G32	MC_ADDR05	O
G33	MC_ADDR13	O
G34	VDD15	P
G35	VDD33(VDDP)	P
G36	MC_ADDR00	O

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Pin	Signal	Type
G37	MC_DIN17	I
H1	FLQS_DOUT14	O
H2	FLQS_DOUT13	O
H3	FLQS_DOUT15	O
H4	GND	P
H5	STAT_CLK	O
H6	FLQS_DIN07	I
H7	STAT_ARR12	O
H8	STAT_ARR08	O
H9	STAT_ARR06	O
H10	LLST_DIN15	I
H11	STAT_ARR05	O
H12	STAT_ARR03	O
H13	LLST_RD_N	O
H14	SAR_CLK_CP	I
H15	LLST_DIN03	I
H16	LLST_DIN01	I
H17	LLST_DOUT14	O
H18	LLST_DOUT07	O
H19	LLST_DOUT00	O
H20	ZBUS_PRTY01	B
H21	ZBUS_DEVID01	I
H22	ZBUS_AVALID_N	B
H23	ZBUS_AD31	B
H24	ZBUS_AD28	B
H25	ZBUS_AD24	B
H26	MC_CLK_KN	O
H27	MC_DOUT13	O
H28	MC_DOUT10	O
H29	MC_DOUT00	O
H30	MC_ADDR19	O
H31	MC_ADDR17	O
H32	TDI	I
H33	VDD15	P
H34	GND	P
H35	MC_DIN16	I
H36	MC_DIN14	I
H37	MC_DIN15	I
J1	FLQS_DOUT07	O
J2	FLQS_DOUT11	O
J3	FLQS_DOUT10	O
J4	STAT_DEP10	O
J5	STAT_DEP00	O

Pin	Signal	Type
J6	STAT_DEP08	O
J7	STAT_ARR17	O
J8	STAT_ARR10	O
J9	LLST_CLK_CP	I
J10	FLQS_DIN00	I
J11	STAT_ARR04	O
J12	LLST_DIN10	I
J13	LLST_WR_N	O
J14	LLST_DIN09	I
J15	LLST_CLK_KN	O
J16	LLST_DOUT13	O
J17	LLST_DOUT06	O
J18	ZBUS_GNT_N	I
J19	ZBUS_DEVID03	I
J20	ZBUS_DEVID04	I
J21	ZBUS_PRTY00	B
J22	ZBUS_CLK	I
J23	ZBUS_AD29	B
J24	ZBUS_AD27	B
J25	ZBUS_AD25	B
J26	ZBUS_AD23	B
J27	ZBUS_AD19	B
J28	ZBUS_AD18	B
J29	ZBUS_AD08	B
J30	GND	P
J31	GND	P
J32	TMS	I
J33	MC_ADDR04	O
J34	GND	P
J35	MC_DIN13	I
J36	MC_DIN12	I
J37	MC_DIN11	I
K1	FLQS_DOUT09	O
K2	FLQS_DOUT04	O
K3	FLQS_DOUT08	O
K4	GND	P
K5	FLQS_CLKOUT	O
K6	STAT_DEP07	O
K7	STAT_DEP05	O
K8	STAT_VREF	P
K9	GND	P
K10	VDD18	P
K11	VDD18	P

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Pin	Signal	Type
K12	VDD18	P
K13	VDD18	P
K14	VDD18	P
K15	VDD18	P
K16	VDD18	P
K17	VDD18	P
K18	GND	P
K19	ZBUS_DEVID02	I
K20	ZBUS_DEVID00	I
K21	ZBUS_DVALID_N	B
K22	ZBUS_AD30	B
K23	ZBUS_AD22	B
K24	ZBUS_AD26	B
K25	ZBUS_AD20	B
K26	ZBUS_AD14	B
K27	ZBUS_AD15	B
K28	ZBUS_AD11	B
K29	ZBUS_AD07	B
K30	ZBUS_AD05	B
K31	GND	P
K32	MC_CLK_CN	I
K33	IDDQ_N	I
K34	GND	P
K35	MC_DIN10	I
K36	MC_DIN08	I
K37	MC_DIN09	I
L1	FLQS_DOUT03	O
L2	FLQS_DOUT05	O
L3	FLQS_DOUT06	O
L4	GND	P
L5	FLQS_TIC_OUT	O
L6	STAT_DEP_PRTY	O
L7	STAT_ARR13	O
L8	STAT_DEP03	O
L9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L13	GND	P
L14	GND	P
L15	GND	P
L16	GND	P
L17	GND	P

Pin	Signal	Type
L21	GND	P
L22	GND	P
L23	GND	P
L24	GND	P
L25	GND	P
L26	GND	P
L27	GND	P
L28	VDD18	P
L29	ZBUS_AD06	B
L30	ZBUS_AD04	B
L31	GND	P
L32	MC_CLK_CP	I
L33	SCAN_SHIFT_N	I
L34	GND	P
L35	MC_DIN07	I
L36	MC_DIN06	I
L37	MC_DIN04	I
M1	FLQS_DOUT01	O
M2	FLQS_DOUT00	O
M3	FLQS_DOUT02	O
M4	VDD33(VDDP)	P
M5	STAT_DEP12	O
M6	STAT_ARR15	O
M7	STAT_DEP11	O
M8	STAT_DEP01	O
M9	GND	P
M10	VDD18	P
M11	GND	P
M12	VDD15	P
M13	VDD15	P
M14	VDD15	P
M15	VDD15	P
M16	VDD15	P
M17	VDD15	P
M21	VDD15	P
M22	VDD15	P
M23	VDD15	P
M24	VDD15	P
M25	VDD15	P
M26	VDD15	P
M27	GND	P
M28	VDD18	P
M29	ZBUS_AD02	B

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Pin	Signal	Type
M30	ZBUS_AD01	B
M31	GND	P
M32	SCAN_MODE_N	I
M33	MC_VREF0	P
M34	GND	P
M35	MC_DIN05	I
M36	MC_DIN03	I
M37	MC_DIN02	I
N1	TX_STAT_DN03	I
N2	TX_STAT_SOFN	I
N3	TX_STAT_SOFP	I
N4	VDD33(VDDP)	P
N5	FLQS_DOUT12	O
N6	STAT_DEP02	O
N7	TURBO_DATA03	O
N8	TURBO_DATA02	O
N9	GND	P
N10	VDD18	P
N11	LLST_VREF0	P
N27	GND	P
N28	VDD18	P
N29	ZBUS_DIR	O
N30	ZBUS_INT_N00	O
N31	GND	P
N32	MC_VREF1	P
N33	TCK	I
N34	GND	P
N35	MC_DIN00	I
N36	MC_DIN01	I
N37	PLL_DIV_RST	I
P1	TX_STAT_DP03	I
P2	TX_STAT_DN02	I
P3	TX_STAT_DP02	I
P4	GND	P
P5	TX_SPI4_STAT_D01	I
P6	TURBO_CLK	O
P7	TURBO_DATA00	O
P8	TURBO_DATA01	O
P9	GND	P
P10	VDD18	P
P11	LLST_VREF1	P
P27	VDD33	P
P28	VDD18	P

Pin	Signal	Type
P29	ZBUS_AD00	B
P30	ZBUS_INT_N02	O
P31	TDO	O
P32	TRST_N	I
P33	RESET_N	I
P34	GND	P
P35	PLL_SYS_MON	O
P36	PLL_SYS_LCK	O
P37	PLL_RX_RST	I
R1	TX_STAT_DP01	I
R2	TX_STAT_CLKN	I
R3	TX_STAT_CLKP	I
R4	GND	P
R5	TX_SPI4_STAT_D00	I
R6	PLL_TX_RST	I
R7	TX_SPI4_STAT_CLK	I
R8	PLL_TX_LCK	I
R9	GND	P
R10	VDD18	P
R11	SAR_VREF	P
R27	VDD33	P
R28	VDD18	P
R29	ZBUS_INT_N01	O
R30	ZBUS_REQ_N	O
R31	PLL_RST	I
R32	PLL_RX_LCK	O
R33	PLL_CFG_OVR	I
R34	RX_VREF0	P
R35	RX_STAT_SOFN	O
R36	RX_STAT_SOFP	O
R37	RX_STAT_DP03	O
T1	TX_STAT_DN01	I
T2	TX_STAT_DN00	I
T3	TX_STAT_DP00	I
T4	GND	P
T5	VDDO_25V_LVDS_DST	P
T6	GND	P
T7	VDD18	P
T8	GND	P
T9	GND	P
T10	VDD18	P
T11	GND	P
T16	VDD18	P

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Pin	Signal	Type
T17	VDD18	P
T18	VDD18	P
T19	VDD18	P
T20	VDD18	P
T21	VDD18	P
T22	VDD18	P
T27	VDD33	P
T28	VDD18	P
T29	ZBUS_AD03	B
T30	ZBUS_AD09	B
T31	PLL_DDR_BYPCLK	I
T32	RX_SPI4_STAT_D01	O
T33	RX_SPI4_STAT_D00	O
T34	RX_VREF1	P
T35	RX_STAT_DN02	O
T36	RX_STAT_DP02	O
T37	RX_STAT_DN03	O
U1	TX_SOFN	O
U2	TX_STAT_PRTYN	I
U3	TX_STAT_PRTYP	I
U4	GND	P
U5	VDDO_25V_LVDS_DST	P
U6	GND	P
U7	VDD18	P
U8	GND	P
U9	GND	P
U10	VDD18	P
U11	GND	P
U16	GND	P
U17	GND	P
U18	GND	P
U19	GND	P
U20	GND	P
U21	GND	P
U22	GND	P
U27	VDD33	P
U28	VDD18	P
U29	ZBUS_AD10	B
U30	ZBUS_AD17	B
U31	RX_SPI4_STAT_CLK	O
U32	GND	P
U33	PLL_SYS_VDDA	P
U34	VDDO_25V_LVDS_DSR	P
U35	RX_STAT_CLKN	O
U36	RX_STAT_CLKP	O
U37	RX_STAT_DP01	O
V1	TX_SOFP	O
V2	TX_DN15	O
V3	TX_DP15	O
V4	GND	P
V5	PLL_TX_REFCLK	I
V6	PLL_TX_VDDA	P
V7	GND	P
V8	VDD18	P
V9	GND	P
V10	VDDO_25V_LVDS_DST	P
V16	VDD18	P
V17	VDD18	P
V18	VDD18	P
V19	VDD18	P
V20	VDD18	P
V21	VDD18	P
V22	VDD18	P
V28	VDDO_25V_LVDS_DSR	P
V29	ZBUS_AD13	B
V30	ZBUS_AD12	B
V31	PLL_SYS_REFCLK	I
V32	PLL_SYS_VDD	P
V33	PLL_SYS_VSSA	P
V34	VDDO_25V_LVDS_DSR	P
V35	RX_STAT_DP00	O
V36	RX_STAT_DN00	O
V37	RX_STAT_DN01	O
W1	TX_DP13	O
W2	TX_DN14	O
W3	TX_DP14	O
W4	GND	P
W5	PLL_TX_VDD	P
W6	PLL_TX_VSSA	P
W7	GND	P
W8	VDD18	P
W9	GND	P
W10	VDDO_25V_LVDS_DST	P
W16	GND	P
W17	GND	P
W18	GND	P

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Pin	Signal	Type
W19	GND	P
W20	GND	P
W21	GND	P
W22	GND	P
W28	VDDO_25V_LVDS_DSR	P
W29	ZBUS_AD21	B
W30	ZBUS_AD16	B
W31	VDD33	P
W32	VDD33	P
W33	GND	P
W34	VDDO_25V_LVDS_DSR	P
W35	RX_STAT_PRTYN	O
W36	RX_STAT_PRTYP	O
W37	RX_SOFN	I
Y1	TX_DN13	O
Y2	TX_DN12	O
Y3	TX_DP12	O
Y4	GND	P
Y5	VDDO_25V_LVDS_DST	B
Y6	GND	P
Y7	GND	P
Y8	VDD18	P
Y9	GND	P
Y10	VDDO_25V_LVDS_DST	P
Y16	VDD18	P
Y17	VDD18	P
Y18	VDD18	P
Y19	VDD18	P
Y20	VDD18	P
Y21	VDD18	P
Y22	VDD18	P
Y28	VDDO_25V_LVDS_DSR	P
Y29	GND	P
Y30	VDD18	P
Y31	VDD18	P
Y32	GND	P
Y33	GND	P
Y34	VDD18	B
Y35	RX_DN15	I
Y36	RX_DP15	I
Y37	RX_SOFP	I
AA1	TX_DN10	O
AA2	TX_DP11	O

Pin	Signal	Type
AA3	TX_DN11	O
AA4	VDD18	P
AA5	VDD0_25V_LVDS_DST	P
AA6	GND	P
AA7	VDD18	P
AA8	GND	P
AA9	VDD26	P
AA10	GND	P
AA11	VDD33	P
AA16	GND	P
AA17	GND	P
AA18	GND	P
AA19	GND	P
AA20	GND	P
AA21	GND	P
AA22	GND	P
AA27	PLL_RX_VDDA	P
AA28	PLL_RX_VSSA	P
AA29	VDD26	P
AA30	VDD18	P
AA31	VDD18	P
AA32	GND	P
AA33	PLL_RX_REFCLK	I
AA34	VDDO_25V_LVDS_DSR	P
AA35	RX_DN14	I
AA36	RX_DP14	I
AA37	RX_DN13	I
AB1	TX_DP10	O
AB2	TX_DN09	O
AB3	TX_DP09	O
AB4	VDD18	P
AB5	TX_VREF0	P
AB6	GND	P
AB7	VDD18	P
AB8	GND	P
AB9	VDD26	P
AB10	GND	P
AB11	VDD33	P
AB16	VDD18	P
AB17	VDD18	P
AB18	VDD18	P
AB19	VDD18	P
AB20	VDD18	P

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Pin	Signal	Type
AB21	VDD18	P
AB22	VDD18	P
AB27	PLL_RX_VDD	P
AB28	GND	P
AB29	VDD26	P
AB30	VDD18	P
AB31	VDD18	P
AB32	GND	P
AB33	VDD18	B
AB34	VDD18	P
AB35	RX_DN12	I
AB36	RX_DP12	I
AB37	RX_DP13	I
AC1	TX_CLKN	O
AC2	TX_DP08	O
AC3	TX_DN08	O
AC4	TX_VREF1	P
AC5	TX_VREF	P
AC6	GND	P
AC7	VDD18	P
AC8	GND	P
AC9	VDD26	P
AC10	GND	P
AC11	VDD18	P
AC27	VDD18	P
AC28	GND	P
AC29	VDD26	P
AC30	VDD18	P
AC31	VDD18	P
AC32	GND	P
AC33	GND	P
AC34	VDD18	P
AC35	RX_DN11	I
AC36	RX_DP11	I
AC37	RX_DN10	I
AD1	TX_CLKP	O
AD2	TX_DN07	O
AD3	TX_DP07	O
AD4	VDD18	P
AD5	TX_VREF2	P
AD6	GND	P
AD7	VDD18	P
AD8	GND	P

Pin	Signal	Type
AD9	VDD26	P
AD10	GND	P
AD11	VDD18	P
AD27	VDD18	P
AD28	GND	P
AD29	VDD26	P
AD30	VDD18	P
AD31	VDD18	P
AD32	GND	P
AD33	VDD18	P
AD34	VDD18	P
AD35	RX_DP09	I
AD36	RX_DN09	I
AD37	RX_DP10	I
AE1	TX_DN05	O
AE2	TX_DN06	O
AE3	TX_DP06	O
AE4	TX_VREF3	P
AE5	GND	P
AE6	VDD26	P
AE7	GND	P
AE8	VDD26	P
AE9	VDD26	P
AE10	GND	P
AE11	VDD18	P
AE27	VDD18	P
AE28	GND	P
AE29	VDD26	P
AE30	VDD26	P
AE31	VDD18	P
AE32	GND	P
AE33	VDD26	P
AE34	VDD18	P
AE35	RX_DP08	I
AE36	RX_DN08	I
AE37	RX_CLKP	I
AF1	TX_DP05	O
AF2	TX_DN04	O
AF3	TX_DP04	O
AF4	TX_VREF4	P
AF5	GND	P
AF6	VDD26	P
AF7	GND	P

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Pin	Signal	Type
AF8	VDD26	P
AF9	VDD26	P
AF10	GND	P
AF11	VDD18	P
AF27	VDD18	P
AF28	GND	P
AF29	VDD26	P
AF30	VDD26	P
AF31	VDD18	P
AF32	GND	P
AF33	VDD26	P
AF34	VDD26	P
AF35	RX_DP07	I
AF36	RX_DN07	I
AF37	RX_CLKN	I
AG1	TX_DP02	O
AG2	TX_DN03	O
AG3	TX_DP03	O
AG4	VDD26	P
AG5	VDD26	P
AG6	VDD26	P
AG7	GND	P
AG8	VDD26	P
AG9	VDD26	P
AG10	GND	P
AG11	VDD18	P
AG12	VDD26	P
AG13	VDD26	P
AG14	VDD26	P
AG15	VDD26	P
AG16	VDD26	P
AG17	VDD26	P
AG21	VDD26	P
AG22	VDD26	P
AG23	VDD26	P
AG24	VDD26	P
AG25	VDD26	P
AG26	VDD26	P
AG27	VDD18	P
AG28	GND	P
AG29	VDD26	P
AG30	VDD26	P
AG31	VDD18	P

Pin	Signal	Type
AG32	DRAM1_ADDR12	O
AG33	DRAM1_ADDR11	O
AG34	VDD26	P
AG35	RX_DP06	I
AG36	RX_DN06	I
AG37	RX_DN05	I
AH1	TX_DN02	O
AH2	TX_DN01	O
AH3	TX_DP01	O
AH4	VDD26	P
AH5	VDD26	P
AH6	DRAM0_WE_N	O
AH7	GND	P
AH8	VDD26	P
AH9	VDD26	P
AH10	GND	P
AH11	VDD26	P
AH12	VDD26	P
AH13	VDD26	P
AH14	VDD26	P
AH15	VDD26	P
AH16	VDD26	P
AH17	VDD26	P
AH18	VDD26	P
AH19	VDD26	P
AH20	VDD26	P
AH21	VDD26	P
AH22	VDD26	P
AH23	VDD26	P
AH24	VDD26	P
AH25	VDD26	P
AH26	VDD26	P
AH27	VDD26	P
AH28	GND	P
AH29	VDD26	P
AH30	VDD26	P
AH31	VDD18	P
AH32	DRAM1_ADDR10	O
AH33	DRAM1_ADDR09	O
AH34	VDD26	P
AH35	RX_DP04	I
AH36	RX_DN04	I
AH37	RX_DP05	I

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Pin	Signal	Type
AJ1	TX_PRTYP	O
AJ2	TX_DP00	O
AJ3	TX_DN00	O
AJ4	VDD26	P
AJ5	DRAM0_RAS_N	O
AJ6	DRAM0_CS_N	O
AJ7	GND	P
AJ8	VDD26	P
AJ9	VDD26	P
AJ10	GND	P
AJ11	VDD26	P
AJ12	GND	P
AJ13	GND	P
AJ14	GND	P
AJ15	GND	P
AJ16	GND	P
AJ17	GND	P
AJ18	GND	P
AJ19	GND	P
AJ20	GND	P
AJ21	GND	P
AJ22	GND	P
AJ23	GND	P
AJ24	GND	P
AJ25	GND	P
AJ26	GND	P
AJ27	VDD26	P
AJ28	GND	P
AJ29	VDD26	P
AJ30	VDD26	P
AJ31	VDD18	P
AJ32	DRAM1_ADDR08	O
AJ33	DRAM1_ADDR07	O
AJ34	VDD26	P
AJ35	RX_DN03	I
AJ36	RX_DP03	I
AJ37	RX_DN02	I
AK1	TX_PRTYN	O
AK2	DRAM0_BNK01	O
AK3	DRAM0_CAS_N	O
AK4	VDD26	P
AK5	DRAM0_CKE	O
AK6	VDD26	P

Pin	Signal	Type
AK7	GND	P
AK8	GND	P
AK9	VDD26	P
AK10	GND	P
AK11	GND	P
AK12	GND	P
AK13	GND	P
AK14	GND	P
AK15	GND	P
AK16	GND	P
AK17	GND	P
AK18	VDD26	P
AK19	VDD26	P
AK20	VDD26	P
AK21	GND	P
AK22	GND	P
AK23	GND	P
AK24	GND	P
AK25	GND	P
AK26	GND	P
AK27	GND	P
AK28	GND	P
AK29	VDD26	P
AK30	VDD18	P
AK31	VDD18	P
AK32	DRAM1_ADDR06	O
AK33	DRAM1_ADDR05	O
AK34	VDD26	P
AK35	RX_DP01	I
AK36	RX_DN01	I
AK37	RX_DP02	I
AL1	DRAM0_BNK00	O
AL2	DRAM0_D07	B
AL3	DRAM0_D06	B
AL4	GND	P
AL5	VDD26	P
AL6	VDD26	P
AL7	DRAM0_D31	B
AL8	DRAM0_D34	B
AL9	DRAM0_DQS03	B
AL10	DRAM0_D27	B
AL11	DRAM0_D22	B
AL12	DRAM0_D20	B

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Pin	Signal	Type
AL13	DRAM0_D16	B
AL14	DRAM0_D17	B
AL15	VDD26	P
AL16	VDD26	P
AL17	VDD26	P
AL18	GND	P
AL19	GND	P
AL20	GND	P
AL21	VDD26	P
AL22	VDD26	P
AL23	VDD26	P
AL24	VDD26	P
AL25	DRAM1_D24	B
AL26	DRAM1_DQS02	B
AL27	DRAM1_D20	B
AL28	GND	P
AL29	GND	P
AL30	DRAM1_DQS01	B
AL31	DRAM1_D01	B
AL32	DRAM1_ADDR04	O
AL33	DRAM1_ADDR03	O
AL34	VDD26	P
AL35	RX_DP00	I
AL36	RX_DN00	I
AL37	RX_PRTYP	I
AM1	DRAM0_D05	B
AM2	DRAM0_D04	B
AM3	DRAM0_DQS00	B
AM4	GND	P
AM5	VDD26	P
AM6	DRAM0_D32	B
AM7	DRAM0_DQS04	B
AM8	DRAM0_D28	B
AM9	DRAM0_D26	B
AM10	DRAM0_D24	B
AM11	DRAM0_D23	B
AM12	DRAM0_D19	B
AM13	DRAM0_D18	B
AM14	DRAM0_D13	B
AM15	DRAM0_DQS01	B
AM16	DRAM0_D09	B
AM17	DRAM0_D11	B
AM18	DRAM1_D39	B

Pin	Signal	Type
AM19	DRAM1_D37	B
AM20	DRAM1_D35	B
AM21	DRAM1_D32	B
AM22	DRAM1_D30	B
AM23	DRAM1_D28	B
AM24	DRAM1_D23	B
AM25	DRAM1_D22	B
AM26	DRAM1_D25	B
AM27	DRAM1_D18	B
AM28	DRAM1_D15	B
AM29	DRAM1_D13	B
AM30	DRAM1_D10	B
AM31	DRAM1_D11	B
AM32	DRAM1_D00	B
AM33	DRAM1_DQS00	B
AM34	VDD26	P
AM35	DRAM1_ADDR01	O
AM36	DRAM1_ADDR02	O
AM37	RX_PRTYN	I
AN1	DRAM0_D02	B
AN2	DRAM0_D03	B
AN3	DRAM0_D00	B
AN4	GND	P
AN5	DRAM0_D35	B
AN6	DRAM0_D36	B
AN7	DRAM0_D30	B
AN8	DRAM0_D33	B
AN9	DRAM0_D29	B
AN10	DRAM0_D25	B
AN11	DRAM0_DQS02	B
AN12	DRAM0_D21	B
AN13	DRAM0_D12	B
AN14	DRAM0_D14	B
AN15	DRAM0_D15	B
AN16	DRAM0_D10	B
AN17	DRAM0_D08	B
AN18	DRAM1_D38	B
AN19	DRAM1_D36	B
AN20	DRAM1_DQS04	B
AN21	DRAM1_D34	B
AN22	DRAM1_D31	B
AN23	DRAM1_D29	B
AN24	DRAM1_DQS03	B

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Pin	Signal	Type
AN25	DRAM1_D27	B
AN26	DRAM1_D17	B
AN27	DRAM1_D21	B
AN28	DRAM1_D19	B
AN29	DRAM1_D14	B
AN30	DRAM1_D12	B
AN31	DRAM1_D08	B
AN32	DRAM1_D09	B
AN33	DRAM1_D02	B
AN34	VDD26	P
AN35	DRAM1_D07	B
AN36	DRAM1_D06	B
AN37	DRAM1_ADDR00	O
AP1	DRAM0_D01	B
AP2	DRAM0_D37	B
AP3	DRAM0_D39	B
AP4	GND	P
AP5	GND	P
AP6	GND	P
AP7	GND	P
AP8	VDD26	P
AP9	VDD26	P
AP10	GND	P
AP11	GND	P
AP12	GND	P
AP13	DRAM_VREF0	P
AP14	DRAM_VREF1	P
AP15	DRAM_VREF2	P
AP16	VDD26	P
AP17	VDD26	P
AP18	VDD26	P
AP19	VDD26	P
AP20	VDD26	P
AP21	VDD26	P
AP22	VDD26	P
AP23	DRAM_VREF3	P
AP24	DRAM_VREF4	P
AP25	VDD26	P
AP26	VDD26	P
AP27	GND	P
AP28	GND	P
AP29	GND	P
AP30	GND	P

Pin	Signal	Type
AP31	GND	P
AP32	GND	P
AP33	GND	P
AP34	GND	P
AP35	DRAM1_D03	B
AP36	DRAM1_D05	B
AP37	DRAM1_D04	B
AR1	DRAM_CLKN02	O
AR2	DRAM_CLKP02	O
AR3	GND	P
AR4	DRAM0_D70	B
AR5	DRAM0_D67	B
AR6	DRAM0_D65	B
AR7	DRAM0_ADDR11	O
AR8	DRAM_VREF5	P
AR9	DRAM0_ADDR06	O
AR10	DRAM0_ADDR04	O
AR11	DRAM0_D63	B
AR12	DRAM0_D61	B
AR13	DRAM0_D59	B
AR14	DRAM0_D54	B
AR15	DRAM0_D52	B
AR16	DRAM0_DQS06	B
AR17	DRAM0_D48	B
AR18	DRAM0_D44	B
AR19	DRAM_CLKN01	O
AR20	DRAM1_D68	B
AR21	DRAM1_D69	B
AR22	DRAM1_D64	B
AR23	DRAM1_D26	B
AR24	DRAM1_DQS07	B
AR25	DRAM1_D59	B
AR26	DRAM1_D54	B
AR27	DRAM1_D53	B
AR28	DRAM1_D50	B
AR29	DRAM1_D49	B
AR30	DRAM_VREF6	P
AR31	DRAM_VREF7	P
AR32	DRAM1_D46	B
AR33	DRAM1_D47	B
AR34	DRAM1_D42	B
AR35	VDD26	P
AR36	DRAM_CLKN00	O

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Pin	Signal	Type
AR37	DRAM_CLKP00	O
AT1	VDD26	P
AT2	VDD26	P
AT3	DRAM0_D69	B
AT4	DRAM0_DQS08	B
AT5	DRAM0_D66	B
AT6	DRAM0_ADDR12	O
AT7	DRAM0_ADDR09	O
AT8	DRAM0_ADDR07	O
AT9	DRAM0_ADDR03	O
AT10	DRAM0_ADDR01	O
AT11	DRAM0_D62	B
AT12	DRAM0_DQS07	B
AT13	DRAM0_D57	B
AT14	DRAM0_D55	B
AT15	DRAM0_D51	B
AT16	DRAM0_D50	B
AT17	DRAM0_D45	B
AT18	DRAM0_D42	B
AT19	DRAM_CLKP01	O
AT20	DRAM1_D70	B
AT21	DRAM1_DQS08	B
AT22	DRAM1_D67	B
AT23	DRAM1_D63	B
AT24	DRAM1_D61	B
AT25	DRAM1_D58	B
AT26	DRAM1_D57	B
AT27	DRAM1_D52	B
AT28	DRAM1_DQS06	B
AT29	DRAM1_D48	B
AT30	DRAM1_WE_N	O
AT31	DRAM1_CS_N	O
AT32	DRAM1_CAS_N	O
AT33	DRAM1_D45	B
AT34	DRAM1_DQS05	B
AT35	DRAM1_D41	B
AT36	VDD26	P
AT37	VDD26	P
AU1	DRAM0_D38	B
AU2	DRAM0_D71	B
AU3	DRAM0_D68	B
AU4	DRAM0_D64	B
AU5	DRAM0_ADDR10	O

Pin	Signal	Type
AU6	DRAM0_ADDR08	O
AU7	DRAM0_ADDR05	O
AU8	DRAM0_ADDR02	O
AU9	DRAM0_ADDR00	O
AU10	DRAM0_D60	B
AU11	DRAM0_D58	B
AU12	DRAM0_D56	B
AU13	DRAM0_D53	B
AU14	DRAM0_D49	B
AU15	DRAM0_D47	B
AU16	DRAM0_D46	B
AU17	DRAM0_DQS05	B
AU18	DRAM0_D43	B
AU19	DRAM0_D41	B
AU20	DRAM0_D40	B
AU21	DRAM1_D71	B
AU22	DRAM1_D33	B
AU23	DRAM1_D66	B
AU24	DRAM1_D65	B
AU25	DRAM1_D62	B
AU26	DRAM1_D60	B
AU27	DRAM1_D56	B
AU28	DRAM1_D55	B
AU29	DRAM1_D51	B
AU30	DRAM1_D16	B
AU31	DRAM1_RAS_N	O
AU32	DRAM1_CKE	O
AU33	DRAM1_BNK01	O
AU34	DRAM1_BNK00	O
AU35	DRAM1_D44	B
AU36	DRAM1_D43	B
AU37	DRAM1_D40	B

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89TTM552 Package

The package is an ASE HFCBGA-HP, having 1192 pins, with 1 mm pitch; a 37 ×37 pin array; and a 40 × 40 mm enclosure.Figure 7 shows the package geometry.

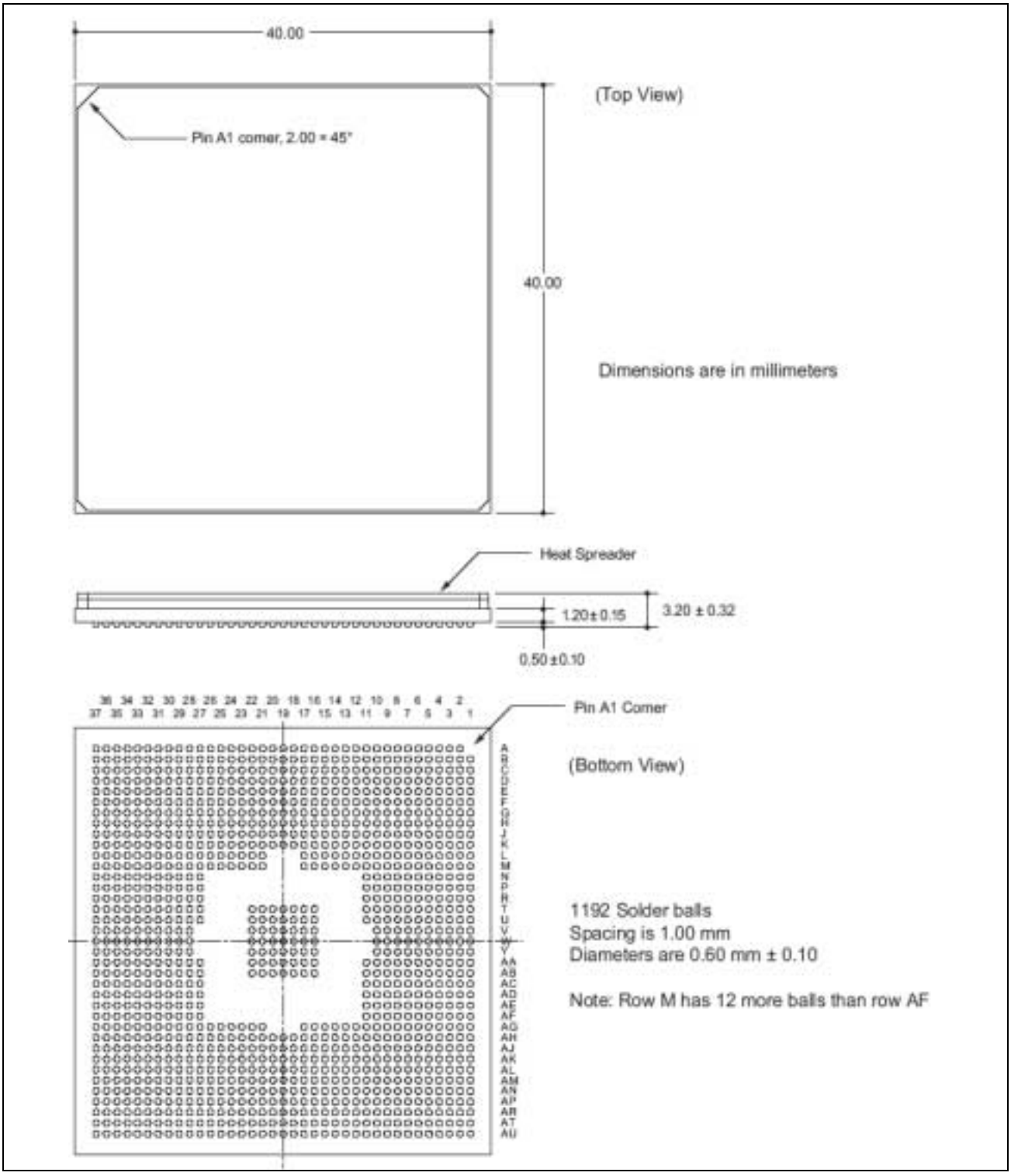

Figure 7 89TTM552 Package Diagram

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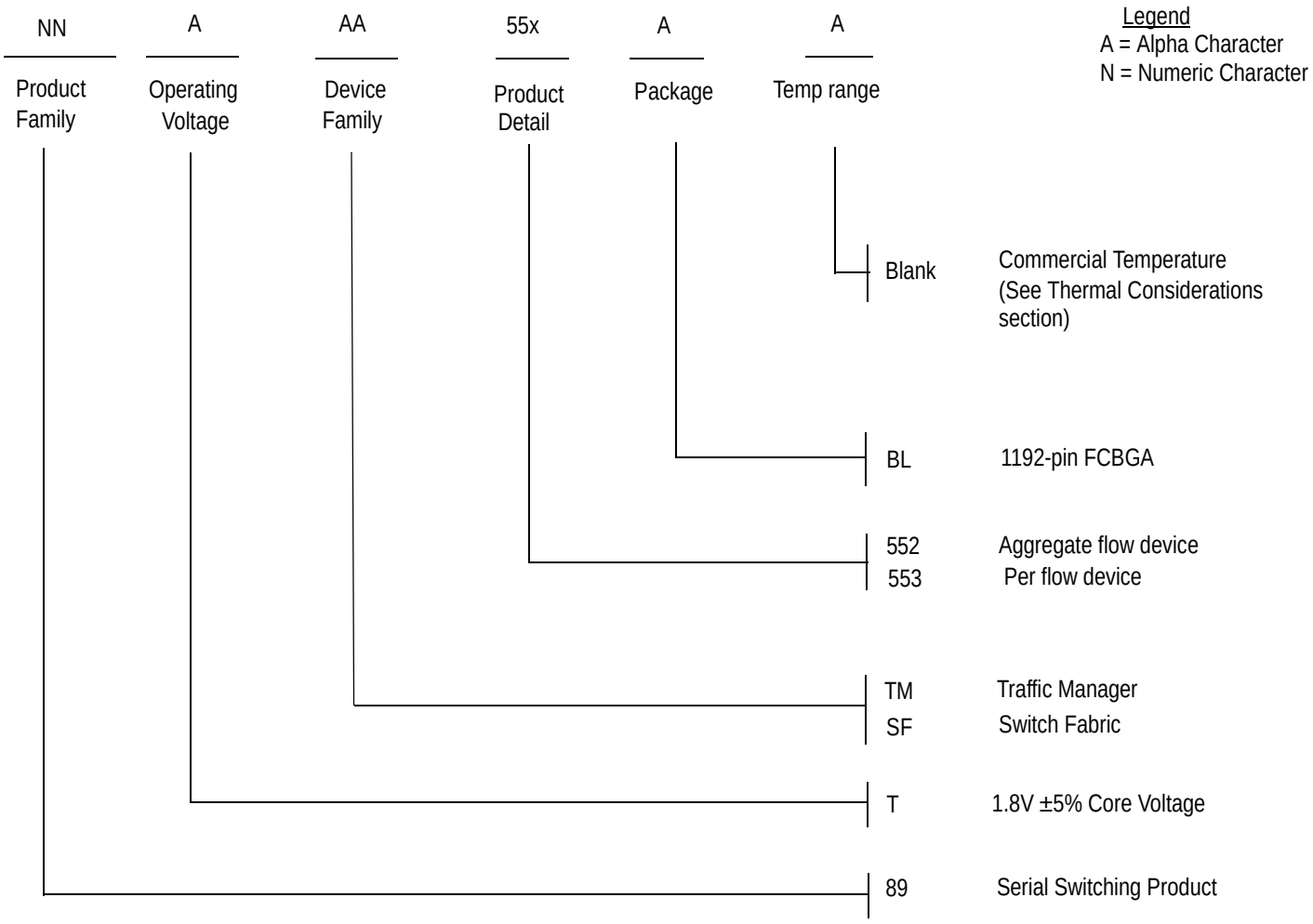

Valid Combinations

89TTM552BL	1192-pin FCBGA package, Commercial Temperature

Revision History

November 23, 2004: Initial publication by IDT.

March 3, 2005: In Table 10, changed frequency for three REFCLK signals from 125 to 100 MHz.

March 11, 2005: In Table 10, for signal PLL_CFG_OVR, “low” was changed to “high” in the Remarks column. Also in Table 10, the following signals were changed to read “pulldown”: PLL_RST, PLL_DIV_RST, PLL_CFG_OVR, PLL_RX_RST, PLL_TX_RST.

April 7, 2005: On page 1, added information to clarify support of 89TTM552 Interfaces.

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