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IMA–32 Inverse Multiplexing for ATM

M28529

32 Port IMA Solutions for T1/E1 and DSL Applications

Mindspeed's M28529 is a general purpose IMA device suitable for both T1/E1 and DSL applications.

The device offers the following industry leading features:

- A low power single chip IMA solution
- Integrated differential delay memory
- Support for 32 T1/E1 or DSL links
- ATM Forum AF-PHY-0086.001 v1.1 and compatible with v1.0

KEY FEATURES

- Single chip 32-port IMA solution
- Integrated differential delay memory
- Industry leading software and support
- 1 to 32 links/group
- Up to 32 IMA groups possible
- ATM forum AF-PHY-0086.001 v1.1 and compatible with v1.0
- 64 Kbps to 8.192Mbps link data rates (in 8 Kbps granularity)

IMA technology has been in the market since 1998 and both the hardware and software have been extensively tested in the field in all types of applications. End products include: access concentrators, DSLAM's, 3G wireless, multi-service platforms, and T1/E1 and DSL line cards. By integrating the transmission convergence function, the device can provide UTOPIA 2 or serial line connectivity to T1/E1 framers and DSL transceivers. Combine this with Mindspeed's IMA software for a simple fast way to add IMA to any system.

Block Diagram

The block diagram in figure 1 shows all the key functional blocks of the design: the ATM layer interface; micro processor interface; the IMA engine; transmission convergence (TC) block; multiplexed options for the physical layer interface; and the SRAM block.

IMA Engine

The IMA block is capable of up to 32 groups maximum. The size of any group can range from one to 32 links. It is possible to bypass the IMA block on a per port basis so that any combination of IMA enabled links or non-IMA links is also possible. The IMA engine supports link data rates up to 8.192 Mbps.

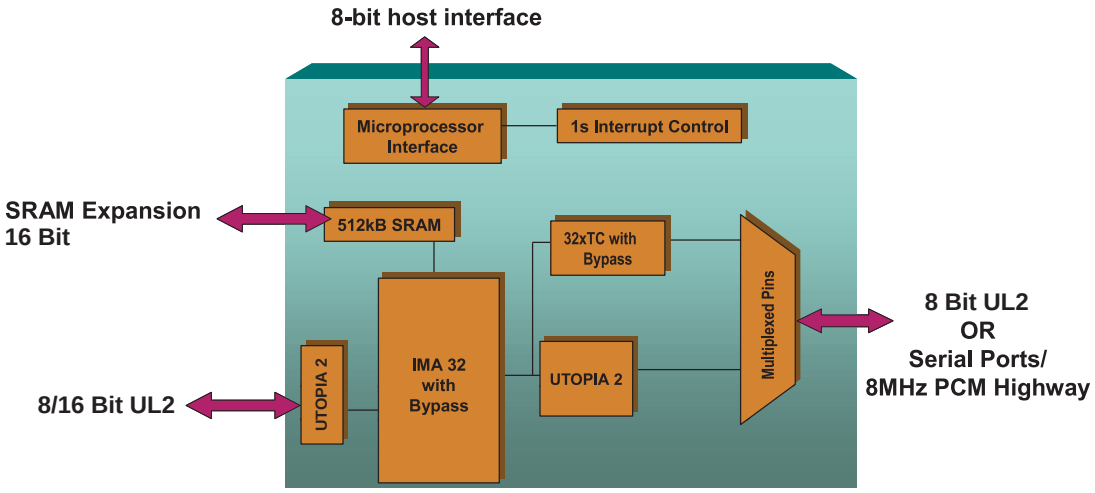

Figure 1: M28529 Block Diagram

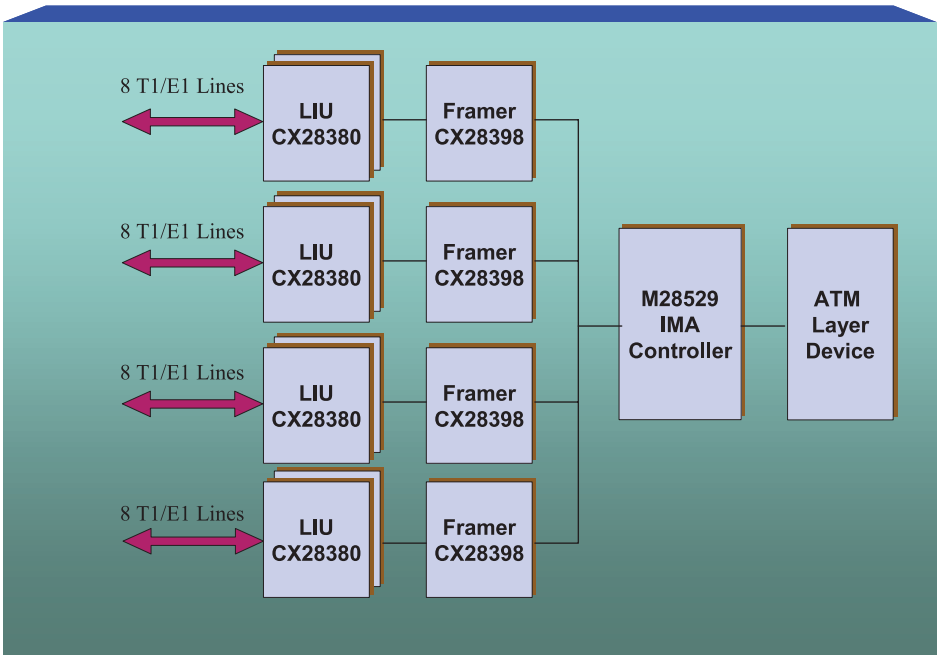

Figure 2: 32 Port T1/E1 Solution 1

Integrated Differential Delay Memory

Typical differential delay requirements vary from 25 ms to 100 ms depending on the application. The M28529's integrated SRAM is sized to handle up to 100 ms of differential delay in 16 port applications and 50 ms of differential delay in 32 port applications. The device also includes a buffer drain to dynamically adjust the amount of differential delay buffering used as IMA groups are dynamically changed. An optional memory expansion port supports up to 275 ms of differential delay in 32 port applications.

Transmission Convergence

This block supports UNI and NNI applications. Cell alignment is recovered from the HEC and can be generated on transmission if required. Idle cells can be passed or rejected on the receive side. In the transmit direction idle cells can be inserted when no traffic is available. The cell delineation block supports data rates up to 8.192 Mbps.

Timing Circuit

A key feature to support DSL is the timing circuit; it is required for UTOPIA based DSL connectivity and is capable of reproducing all the data rates that are possible with DSL technology. Programmable dividers in this circuit allow for flexible rate reference clocks. A variety of clocking methods are available for CPE applications and networking equipment.

ATM Layer Interface

The ATM layer interface is an industry standard multi-PHY UTOPIA 2 interface. The data bus width is selectable between 8 or 16 bits with a maximum 50 MHz data rate.

Physical Layer Interface

The physical layer interface can be configured depending on the type of physical device. If TC is required; the serial line interface ports can be used. Alternatively, an 8 MHz PCM highway is also provided for connection to backplane or framers. If the TC function is done in the physical device, then an 8 or 16 bit UTOPIA 2 port can be used. This makes the device very flexible since T1/E1 framers typically require a serial interface and both (serial and UTOPIA 2) interfaces are common on DSL devices.

Host Interface

Host control is established through a simple 8 bit synchronous/asynchronous microprocessor interface. The interface can operate up to 33 MHz with open drain interrupt outputs.

IMA Software

The IMA software has been proven in the field in many applications. The software driver requires very little host overhead since the Mindspeed solution provides an optimal partitioning of hardware and software functions.

The software is only required to run a non-real-time task approximately every 250 ms and does not require interrupts. The software is composed of subsystem components: configuration, diagnostics, IMA group, failure monitoring, and performance monitoring. An embedded debug monitor and hardware simulator are also provided. The simulator allows for software testing without the presence of a target circuit board.

Complete Chipset Solutions

Mindspeed offers complete chipsets from the UTOPIA interface to the line. Examples of these chipsets are shown in figure 2 and figure 3 for both T1/E1 applications as well as G.shdsl. A Mindspeed sales representative can help with even more devices and chipset options.

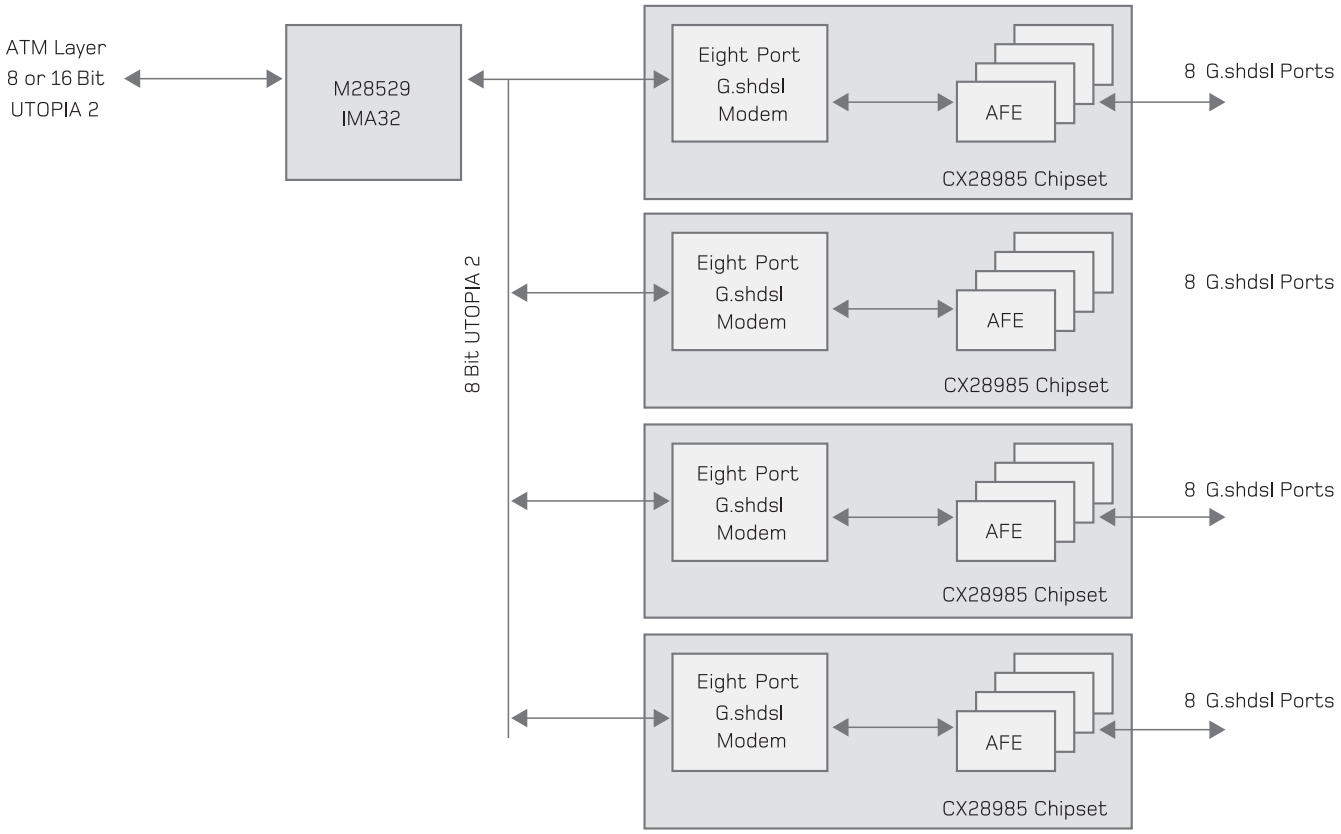

Figure 3: 32 Port G.shdsl Chipset

Product Features

IMA Block supports

- ATM forum AF-PHY-0086.001 v1.1 and compatible with v1.0
- 32 facilities
- Up to 32 groups
- Up to 32 links per group
- Differential delay variation up to 275 ms
- Handles link failures and recovery
- Handles available bandwidth
- Both synchronous and non-synchronous links
- IMA data cell rate implementation (IDCR)
- IMA bypass

Integrated differential delay memory

- 512 Kbytes of internal SRAM
- Between 50 ms and 200 ms of differential delay depending on port count
- Buffer utilization changes dynamically depending on differential delay requirements
- Expansion port for external SRAM and 275 ms of differential delay on 32 ports

Transmission Convergence (TC)

- Supports UNI and NNI
- Recovers cell alignment from HEC
- HEC error correction and detection
- Passes or rejects idle cells
- Generates cell status, cell and error counts
- Inserts idle cells when no traffic is available
- Inserts headers and generates HEC
- I.432 UNI compliant

Software Driver

- OS ANSI-C code
- Configuration management
- Diagnostics for control and testing functions
- Failure monitoring with alarm integration
- Performance monitoring
- Compatible with IMA MIB
- Embedded debug monitor/hardware simulator

ATM Layer Interface

- UTOPIA 2 slave
- Multi-PHY capability
- 8 or 16 bit data path
- Up to 50 MHz data rate

Timing Circuit

- Programmable dividers to reproduce DSL clock rates
- Every group can have a different rate
- Supports asymmetric data rates for ADSL
- T1/E1/J1 support

Utopia 2 Physical Layer Interface

- 8 bit data path
- UTOPIA 2 master for controlling multiple physical layer devices

Control and Status

- 8-bit microprocessor interface
- One second status and counter latching
- Up to 33 MHz operation

Electro-Mechanical

- 27 mm 484 pin BGA
- 1.8 V core and supply
- 3.3 V I/O
- Industrial temp (-40C to 85C)

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