CX29610

OptiPHY™ - M622 STS-12/4x STS-3 SONET/SDH Multiplexer

CX29610 is a highly integrated, multiport chip that provides SONET/SDH processing and multiplexer/demultiplexer functions for a single STS-12/STM-4 data stream or four STS-3/STM-1 data streams. All mappings are compliant with SONET/SDH standards including Bellcore GR-253, ANSI T1.105, and ITU G.707.

Each port supports full-duplex overhead processing of SONET/SDH data streams for section, line, and path layers, framing, scrambling/descrambling, alarm detection/insertion, and BIP error monitoring. Serial interfaces for Section and Line DCC's are also provided. Automatic Protection Switching (APS) is supported via full K1/K2 byte access with Bit Error Rate (BER) calculations done in hardware. This APS support is also fully compatible with Mindspeed's APS protocol stack software package.

The line-side interface is compliant with industry standard LVPECL serial interface transceivers. The drop-side interface is a byte-wide data and clock interface for STS-3 streams in Mindspeed's SONET Interleave interface (SI-Bus) format. This interface provides the ability to pass payload information to nearby processing elements in either STS-1, VC-4 or VC-3 format. An additional serial data channel for each port is provided to support downstream processing (i.e., HDLC). *–Continued–*

Distinguishing Features

- Processes combinations of STS-12, STS-3 payload framing/multiplexing for:
  - 1x STS-12/STM-4
  - 4x STS-3/STM-1
- Glueless connectivity to the CX29503 and CX28500/CX28560 devices.
- Automatic Protection Switching
  - Bit Error Rate calculations performed in hardware
  - User-programmable signal fail and signal degrade thresholds
- Device Driver reference source code available
- Generates/terminates section, line, and path overhead.

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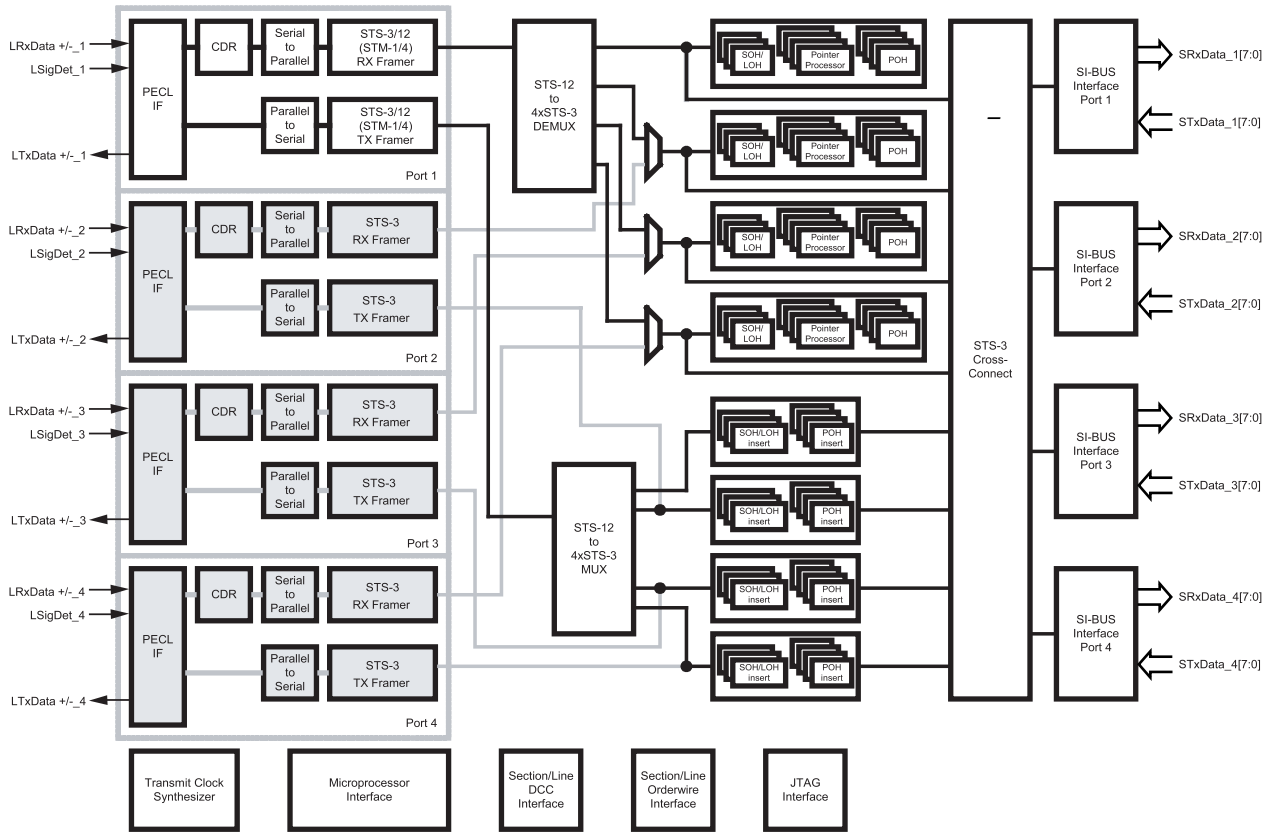
Functional Block Diagram



Ordering Information

Model Number	Package	Operating Temperature
CX29610-12	27 mm PBGA	–40 °C to 85 °C

Revision History

Document Number	Date	Comments
29610-DSH-001-C	July 2005	Revision C. Added note to tie JTAG TRST* low when not using JTAG. Added missing AVDD, AVSS, and NC pins to Table 1-4. Corrrcted pin names in Figure 5-18 and Figure 5-19. Renamed spare/no connects to “Reserved - NC” in Table 1-4 for commonality.
29610-DSH-001-B	July 2004	In chapter 5, updated the MPC read, write, and JTAG timing tables and changed other timing numbers; added footnotes regarding airflow requirements and microprocessor EBUS timing.
29610-DSH-001-A	March 2002	Formerly document number 500243A.

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An 8-bit microprocessor interface is provided for access to control and status registers. This interface provides direct conectivity to the Mindspeed EBUS and the Motorola MPC860 microprocessor interfaces. A full complement of status monitoring, alarm indications, and error counters is provided with maskable interrupts for all status indications.

CX29610 is fully compatible with CX29503 Mindspeed's Broadband Access Multiplexer (BAM) which is a highly integrated STS-1/DS3/E3/DS1/E1/VT1.5 Mapper/Framer. This chipset provides multiplexing solutions from T1/E1 up through STS-12 through either PDH, SONET, or SDH hierarchies.

–Distinguishing Features–Continued

- Embedded clock and data recovery
- Alarm indicators, status monitoring, and error counters
- Provides serial LVPECL interfaces to optical transceivers
- 8-bit microprocessor interface for control and status compatible with the Mindspeed EBUS and Motorola MPC860 interfaces
- Interrupt suppression to suppress low level interrupts when high level interrupts occur
- Low-power 3.3 V process with 5 V tolerant I/O
- JTAG and boundary scan test support

Applications

- Access Concentrators
- Edge Routers
- SONET Cross Connects

Line Interface

- Industry standard serial LVPECL interface to external transceivers
- Transmit clock synthesis
- Built-in receive clock and data recovery
- Monitors receive data for LOS conditions

Overhead Processing

Section Overhead

- Monitors A1/A2 framing and recovers byte-alignment from incoming serial data
- Provides 64-byte transmit and receive buffers for section trace messages
- Generates and checks errors for B1 BIP
- Serial interface for D1-D3 Section DCC
- Section SEF processing
- Codec compatible E1 orderwire serial interface

Line Overhead

- Full pointer processor for tributaries
- Generates and checks errors for B2 BIP
- Serial interface for D4-D12 Line DCC
- Register access for S1 Sync byte
- Line AIS, RDI, REI processing
- Codec compatible E2 orderwire serial interface

Path Overhead

- Provides 64-byte transmit and receive buffers for path trace messages
- Generates and checks errors for B3 BIP
- Generates/monitors for appropriate C2 signal label
- Path AIS, RDI processing

Payload Mapping/Demapping

- SONET: STS-1 -> STS-1 SPE
- SDH: AU-4 -> VC-4 -> TUG-3 -> TU-3
- SDH: AU-3 -> VC-3

Drop Interface

- Mindspeed SONET Interleave interface (SI-Bus)
- 8-bit data, clock, and sync interfaces for STS-1, VC-4, or VC-3 payloads

Control and Status

- 8-bit register interface
- Summary interrupts for various line conditions
- Interrupt supression of low level alarms based on high level alarm conditions (i.e., LOS).
- Error insertion capability
- "One-second" status and counters latching for alarm/error detection and performance monitoring
- Derives 1-sec output from 8 kHz clock input

Electromechanical

- Power dissipation under 2.3 W
- 3.3 V power supply
- 416 pin 27 mm PBGA
- Industrial operating temperature range (-40 ºC to 85 ºC) with airflow

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1.0 Product Description

1.1 CX29610 Features

The CX29610 SONET/SDH Multiplexer enables multiplexing and de-multiplexing of STS-1 SPEs to STS-3 or STS-12 formatted data streams. It operates as a single STS-12 to STS-1 multiplexer or as a four-port (quad) STS-3 to STS-1 multiplexer.

The CX29610 integrates a full SONET/SDH overhead processor, which generates and terminates the STS-12 and/or STS-3 section, line, and path octets. The following features are also provided:

- Internal Clock and Data Recovery for receive line side interface. Transmit line clock synthesis.
- The transmit and receive line interfaces have optional LVPECL clock inputs that can be used if receive and transmit clocks are available in the system.
- Each port has external serial access for section and line DCCs and for the E1/E2 orderwire channels.
- An STS-3 level cross-connect function allows any of the incoming STS-3s (either from separate ports or de-multiplexed from an STS-12) to be routed to any of four SI-Bus interfaces. The SI-Bus interfaces carry the 12 STS-1 streams to downstream devices in an interleaved format as described in Section 2.5.
- An 8-bit microprocessor interface for access to configuration and status registers.
- JTAG test support.

1.1.1 General System Features

The CX29610 provides the following general system features:

- An 8-bit microprocessor interface that supports the Mindspeed EBUS interface used on the CX28500 device and a Motorola MPC860 interface. A single interrupt output, with a programmable interrupt hierarchy. Error counters and status registers. Control registers for device configuration.
- A one-second input, with a one-second output derived from an 8 kHz clock input, to latch status and counter data collection among multiple devices.
- A power down control is provided for each STS-3 port in the 4x STS-3 mode of operation to reduce power consumption on unused ports.
- A default mode of operation (from reset) with the following:
  - 1 x STS-12 interface with line side ports 1-4 mapped to SI-Bus interfaces 1-4
  - internal path overhead processing enabled (except H4 sourced from Transmit SI-Bus)
  - automatic alarm generation enabled
  - no interrupts enabled

1.1.2 Transmitter Features

The CX29610 provides the following transmitter features:

- Maps STS-1 SPEs into STS-3 or STS-12 frame structures.
- Generates section, line, and path overhead.
- A single serial LVPECL interface to external transceiver devices for STS-12 operation or four separate serial LVPECL interfaces for STS-3 operation.
- Four 8-bit SI-Bus interfaces on the system side.
- Serial clock and data interfaces to external circuitry for acess to section DCC, line DCC, and E1/E2 orderwire bytes.
- A frame reference input to allow the transmit frame to be synchronized with an external 8 kHz clock.
- A transmit frame reference output to indicate the relative position of the transmit frame and to coordinate data transfers on the DCC and orderwire channels.
- Transmitter frame scrambling using the $x^7 + x^6 + 1$ polynomial is enabled as the default, but can be disabled by setting the TXSEC register bit 7 high.
- All zeros data in the transmit frame (after scrambling) can be generated by setting the TXSEC register bit 1 high, which allows for LOS testing.

1.1.3 Receiver Features

The CX29610 provides the following receiver features:

- De-maps STS-1 SPEs from STS-3 or STS-12 frame structures.
- Terminates section, line, and path overhead layers and reports errors and alarms.
- A serial LVPECL interface to external transceiver devices for STS-12 operation or four separate serial LVPECL interfaces for STS-3 operation.
- Four 8-bit SI-Bus interfaces on the system side.
- Serial clock and data interfaces allow access to section DCC, line DCC, and E1/E2 orderwire overhead bytes.
- A receive frame reference output to indicate the relative position of the receive frame and to coordinate data transfers on the DCC and orderwire channels.
- Two status output pins for each port to indicate various internal status conditions (selectable via microprocessor control register bits).
- Loss-of-Lock and Signal Detect indications are reported in bits 6 and 7 of the RXSEC register to allow visability of the receive Clock and Data recovery status.
- Bit error rate is monitored from the B2 BIP error count. If the incoming error rate exceeds the thresholds programmed in the APSTHRESH register, then signal degrade or signal fail status is reported in RXAPS bits 0 or 1, respectively.
- Receiver frame descrambling using the $x^7 + x^6 + 1$ polynomial is enabled as the default, but can be disabled by setting bit 3 of the DOWNALM register high.

1.1.3.1 Alarm/Error Detection and Performance Monitoring Features

- LOS—loss of signal. The incoming signal is monitored for an all-zeros or all-ones pattern before descrambling. An all-zeros/ones pattern with a duration longer than 100 µs causes an LOS to be reported in bit 5 of the RXSEC register. LOS is cleared when two consecutive valid framing patterns with no intervening all-zeros/ones pattern qualifying as an LOS have been received.
- LOP-P—loss of pointer. The H1/H2 pointer processor reports LOP in bit 7 of the RXPTH register if a valid pointer is not found for 10 consecutive frames. LOP-P is cleared when a valid pointer with NDF or a valid concatenation indicator has been received in three consecutive frames.
- AIS-L—Line AIS is reported in RXLIN bit 6 when bits 6, 7, and 8 of the K2 byte contain a 111 pattern for 5 consecutive frames. Line AIS is terminated when a non-111 pattern is detected for 5 consecutive frames.
- RDI-L—Line RDI is reported in RXLIN bit 5 when bits 6, 7, and 8 of the K2 byte contain a 110 pattern for 5 consecutive frames. Line RDI is terminated when a non-110 pattern is detected for 5 consecutive frames.
- AIS-P—Path AIS is reported in RXPTH bit 6 when the H1/H2 bytes contain an all-ones pattern for 3 consecutive frames. Path AIS is terminated when a valid H1/H2 pointer is found.
- RDI-P—Path RDI is reported in RXPTH bit 5 according to Table 1-1. The RDI bits from the G1 byte are latched into the RXRDI register when a consistent new value is received for 10 consecutive frames.

Table 1-1. Reported Path RDI

G1 bits 5, 6, 7	Interpretation
000, 011, 001	No RDI-P defect
100, 111	One-bit RDI-P defect
010	ERDI-P payload defect
101	ERDI-P server defect
110	ERDI-P connectivity defect

- PLM-P—Payload Label Mismatch is reported in RXPTH bit 2 when the received C2 value indicates a different payload-specific functionality than that provisioned in the PROVC2 register.
- Uneq-P—Path Unequipped is reported in RXPTH bit 1 when the received C2 value indicates unequipped (00h) and the PROVC2 register contains an equipped functionality code.
- B1 BIP counts are disabled during LOS or OOF conditions.
- B2 BIP counts are disabled during LOS, LOF, or AIS-L conditions.
- Pointer justification counts are disabled during LOS, LOF, AIS-L, or LOP-P conditions.
- REI-L counts are disabled during LOS, LOF, AIS-L, or RDI-L conditions.
- B3 BIP counts are disabled during LOS, LOF, AIS-L, AIS-P, LOP-P, or Uneq-P conditions.

- When an LOS or LOF defect is detected on the incoming signal, AIS-L is automatically generated in the downstream data path by placing all-ones in every byte of the frame except for the section overhead positions. Automatic generation of AIS-L can be disabled by writing bit 7 of DOWNALM low.
- When an LOP-P or a tandem connection ISF defect is detected on the incoming signal, AIS-P is automatically generated in the downstream data path by placing all-ones in the H1/H2/H3 bytes and in the entire STS SPE. Automatic generation of AIS-P can be disabled by writing bits 6, 5, or 4 (for the respective STS-1) of DOWNALM low.
- Capability of generating AIS-P on reception of PLM-P or Uneq-P is provided in addition to the normal generation on reception of LOP-P by setting DOWNALM bit 1 high.

1.1.4 Diagnostic Features

The CX29610 provides the following diagnostic features:

- Source loopback is provided by connecting the line-side transmit clock and data outputs to the receive clock and data inputs (after the clock/data recovery module).
- Line loopback is provided by connecting the receive data inputs (before the clock/data recovery module) to the transmit data line driver outputs.
- DCC interface is such that the receive DCC output can be connected to the transmit DCC input for testing. This requires transmit/receive frame alignment.
- Orderwire interfaces is such that the receive orderwire outputs can be connected to the transmit orderwire inputs for testing in the same manner as for the DCC channels. This requires transmit/receive frame alignment.
- Each SI-Bus interface is individually three-state capable so that separate devices can be used in redundant systems.

1.2 Definitions

It is expected that the reader is somewhat familiar with SONET/SDH terminology, but here are a few definitions that are used in this data sheet.

- **Synchronous Transmit Signal (STS or STM)—**Terminology used to denote the various levels within the SONET (or SDH) hierarchies, as shown in Table 1-2.
- **Synchronous Payload Envelope (SPE)**—Envelope used within an STS frame structure to carry the path layer overhead and payload data.
- **Virtual Container (VC)—**SDH equivalent term to SPE.
- **Path OverHead (POH)**—The 9-byte column of octets in the first column of the SPE. It is used to carry the path overhead octets starting with J1.

Table 1-2. Level Hierarchies within SONET and SDH

SONET	SDH
STS-12 (622.08 Mbps)	STM-4 (622.08 Mbps)
STS-3 (155.52 Mbps)	STM-1 (155.52 Mbps)
STS-3c SPE	VC-4
STS-1 SPE	VC-3 with two columns of stuffing added

1.3 Conventions

The signal direction naming used in this specification is *Transmit* when data is flowing from the slave devices to the CX29610 and *Receive* when data is flowing from the CX29610 to the slave devices.

All signals are active high, unless denoted via a trailing "*" after the signal name, for example:

Signal_1	Active High
Signal_2*	Active Low

An _# (or _**n**) following the a pin label indicates the port number (1–4).

1.4 Terminology

The synchronous digital hierarchy (SDH) is the international counterpart to the synchronous optical network (SONET) used in the United States, Canada, and Japan. As such, SDH and SONET use different terminology to express similar concepts.

Table 1-3 compares SONET terminology with SDH terminology.

Table 1-3. SONET/SDH Terminology

SONET	SDH	Definition
VT Payload	Container (C-n)	Usable payload, sized to carry a standard DS-n (n = 1–4); the VC minus the column of path overhead.
VT Synchronized Payload Envelope (SPE)	Virtual Container (VC-n)	VT Payload or VC plus its column of path overhead (POH). n = 1, 2; basic VC of single C-n with n = 1 or 2. n = 3, 4: higher order VC of one C-n (n = 3, 4), or an assembly of TUG-2s or TU-3s.
—	VC-31	Width of 65 columns fits 4 times (a TUG-31) into a VC-4.
SPE-1	VC-32	85 column capacity.
SPE-3	VC-4	261 column capacity.
Virtual Tributary	Tributary Unit	VC (SPE) plus the pointers to locate the start of the VC/SPE, in a four-frame superframe.
VT1.5	TU-11	1.544 Mbit/s (first form of DS-1) in 3 columns.
VT2	TU-12	2.048 Mbit/s (second form of DS-1) in 4 columns.
VT3	—	For T1-c at 3.152 Mbit/s, not a CEPT rate, in 6 columns.
VT6	TU-21	6.912 Mbit/s payload in 12 columns, 5 map to 1 VC-31.
—	TU-22	9.216 Mbit/s payload in 16 columns, 4 map into 1 VC-31.
—	TU-31	For E-3 in 65 columns.
—	TU-32	For T-3 or STS-1 in 85 columns.
VT Group	TU Group	TUG-2 is an assembly of identical TU-1s or TU-2s.
VTG1, VTG2	TUG-21	Contains 4 TU-11s (VTG1), 3 TU-12s (VTG2), or 1 TU-21 (VTG4) in 12 columns.
VTG3	—	A group of two VC3s, not a defined CEPT rate.

Table 1-3. SONET/SDH Terminology

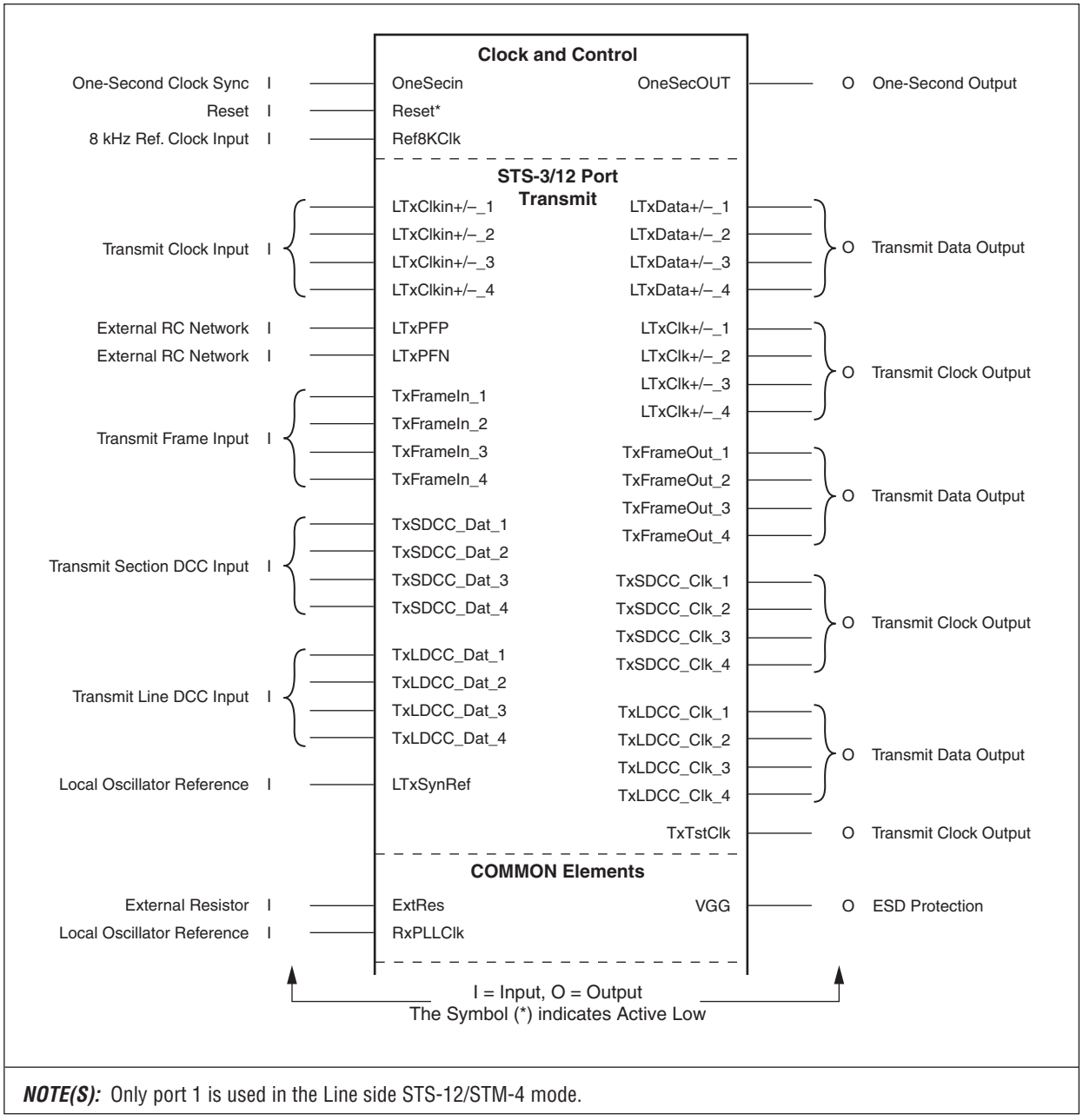
SONET	SDH	Definition
—	TUG-22	Contains 5 TU-11s, 4 TU-12s, or 1 TU-22 in 16 columns.
—	TUG-31	Contains four VC-31s; fills a VC-4.
—	TUG-32	Contains three VC-32s; fills a VC-4.
—	Administrative Unit	A VC plus its pointers H1–H3.
—	AU-31	Four VC-31s fit in STM-1; H1–H3 in rows 1–3, at columns 11–14.
—	AU-32	All 9 H-pointers for 3 VC-32s are in row 4, columns 1–9 of STM-1.
—	AU-4	VC-4 (261 columns) plus the 9 H-pointers in the fourth row of the STM-1 frame.
Section Overhead	—	Contains fields for traffic framing, the identification of the STS payload, error detection, order wires, and a large variety of network-specific functions.
Line Overhead	Section Overhead	All frame overhead is considered the same in SDH pending further definition.
Synchronous Transport Signal (STS)	Synchronous Transport Module (STM)	Basic framing for time division multiplexing in an essentially circuit oriented hierarchy. STS-3 = STM-1.

1.5 Logic Diagram

Figure 1-1 is a logic diagram of the CX29610's functional blocks. There are four general purpose Clock and Control pins. The LIU interface consists of 12 pins. The Microprocessor interface consists of six clock and control inputs, an 8-bit data bus, and an 11-bit address bus. There are six JTAG/Scan pins and eight status pins. The SI-Bus interface consists of 48 transmit pins and 56 receive pins. There are 95 power and 33 ground pins. Pin descriptions are given in Table 1-4.

NOTE: An asterisk (*) following a pin label indicates that the pin logic level is active low, and an _# following the a pin label indicates the port number (1–4).

Figure 1-1. CX29610 Logic Diagram



NOTE(S): Only port 1 is used in the Line side STS-12/STM-4 mode.

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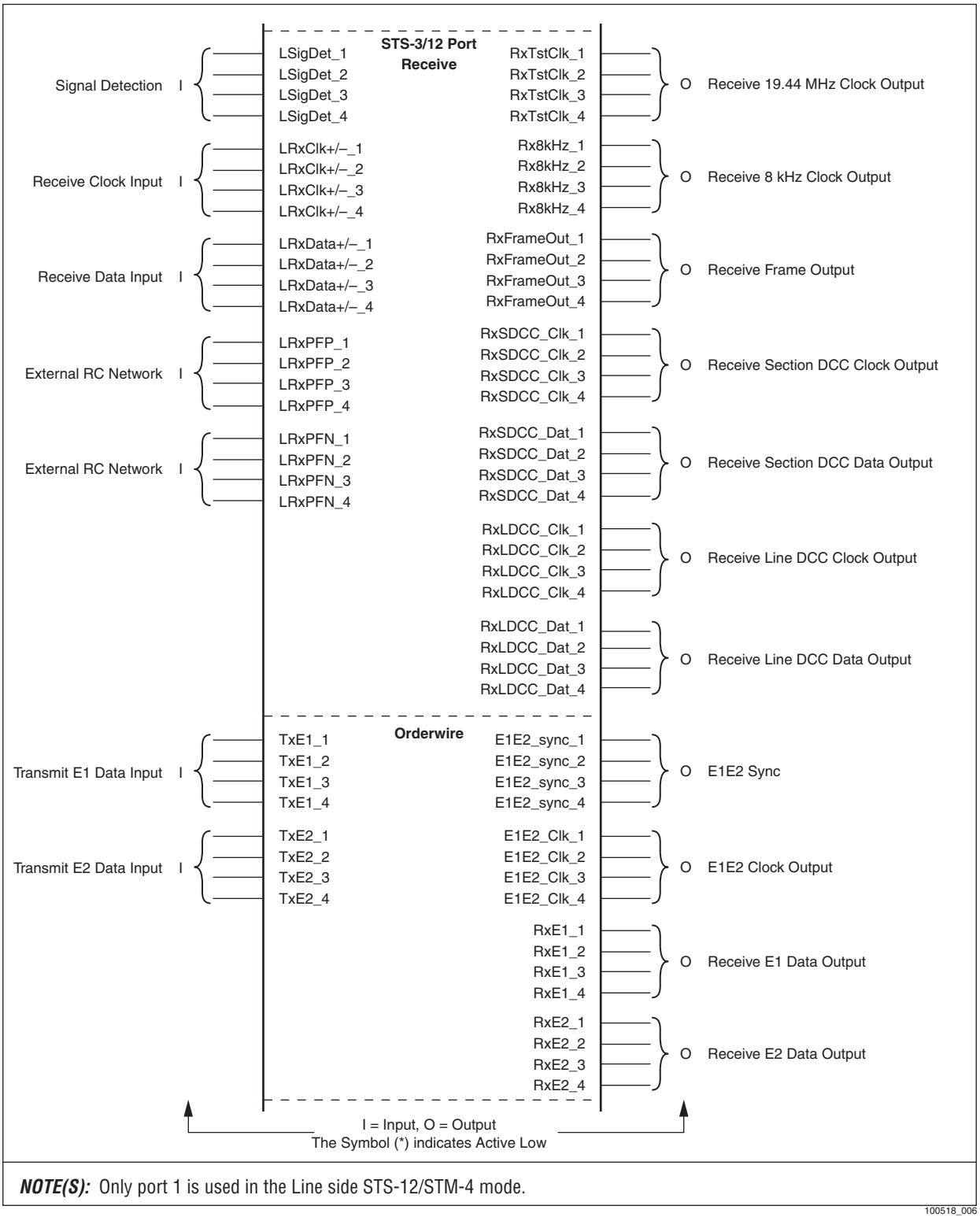
Figure 1-2. CX29610 Logic Diagram



NOTE(S): Only port 1 is used in the Line side STS-12/STM-4 mode.

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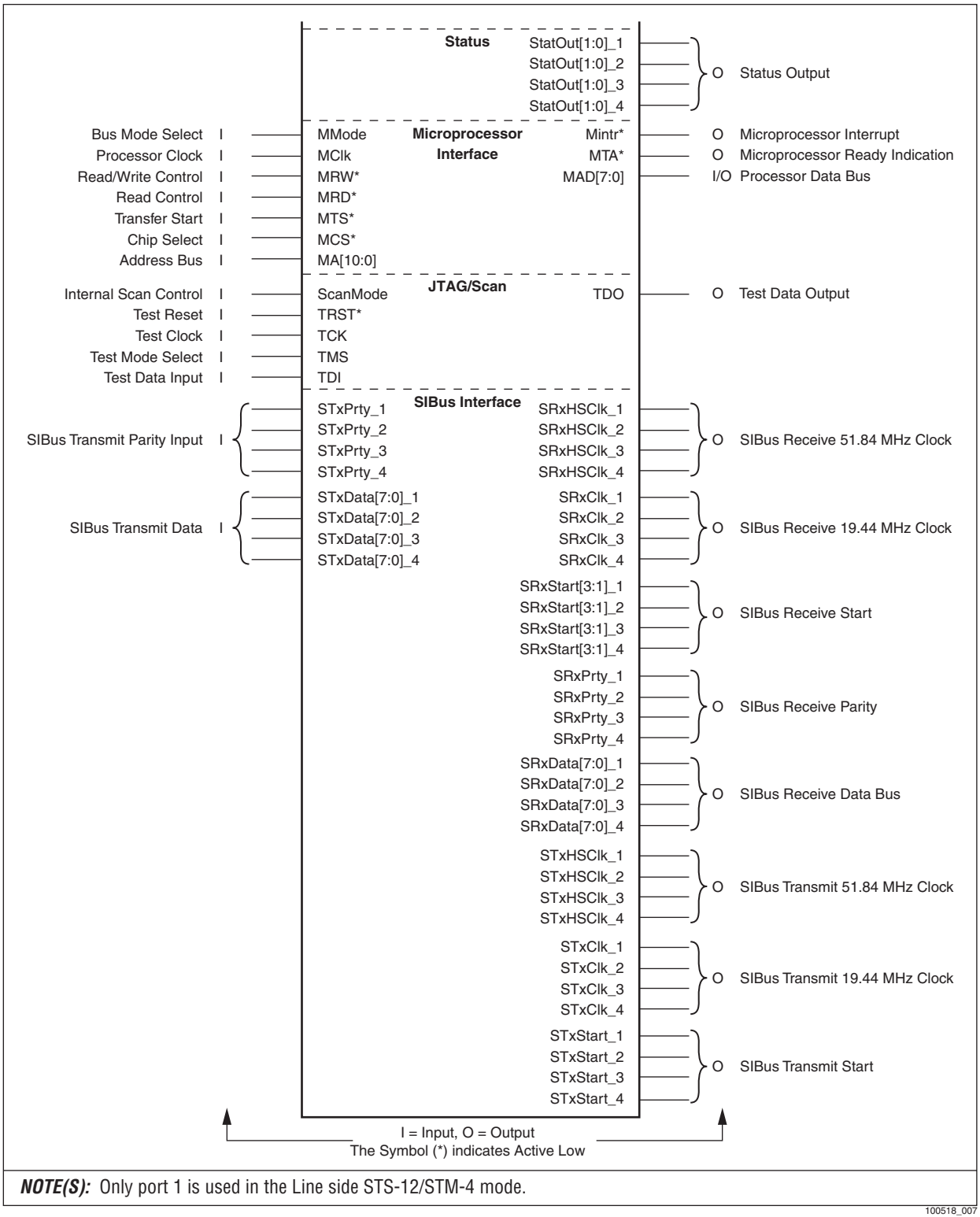
Figure 1-3. CX29610 Logic Diagram



NOTE(S): Only port 1 is used in the Line side STS-12/STM-4 mode.

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Pin names are listed in Table 1-4. An asterisk (*) following a pin label indicates that the pin logic level is active low, and an _# following the a pin label indicates the port number (1-4). Refer to Table 5-21 for a list of pins referenced by pin number.

Table 1-4. Pin Definitions *(1 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Clock and Control	OneSecIn	One Second Input	D6	TTL	I	Latches device status and counters, typically at 1-second intervals.
	Reset*		A6	TTL	I	Resets the device when asserted low.
	Ref8KClk	8 kHz Reference Clock Input	D9	TTL	I	8 kHz clock input used to derive OneSecOut (pin B6).
	OneSecOut	One Second Output	B6	TTL	O	One-second pulse derived from the Ref8KClk input.
Sonet/SDH Line	LTxClkIn–_1	Line Transmit Clock Input Negative Polarity	C1	PECL	I	Optional 155.52 or 622.08 MHz clock for use as the transmit clock as controlled by the CLKREC register.
	LTxClkIn–_2		F2	PECL	I	Allows the use of an externally generated 155.52 MHz clock as selected in the CLKREC register. The external source must be accurate to 20 PPM.
	LTxClkIn–_3		U2	PECL	I	
	LTxClkIn–_4		AC2	PECL	I	
	LTxClkIn+_1	Line Transmit Clock Input Positive Polarity	B1	PECL	I	Optional 155.52 or 622.08 MHz clock for use as the transmit clock as controlled by the CLKREC register.
	LTxClkIn+_2		E2	PECL	I	Allows the use of an externally generated 155.52 MHz clock as selected in the CLKREC register. The external source must be accurate to 20 PPM.
	LTxClkIn+_3		V2	PECL	I	
	LTxClkIn+_4		AD2	PECL	I	
	LTxPFP	Transmit PLL Filter (Positive)	L4	Analog	I	External RC network pins for PLL. See Figure 2-2.
	LTxPFN	Transmit PLL Filter (Negative)	M4	Analog	I	External RC network pins for PLL. See Figure 2-2.

Table 1-4. Pin Definitions (2 of 16)

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Sonet/SDH Line (cont.)	TxFrameIn_1	Transmit Frame Reference Input	AE20	TTL	I	Transmit frame reference input
	TxFrameIn_2		AE15	TTL	I	
	TxFrameIn_3		AE10	TTL	I	
	TxFrameIn_4		AE5	TTL	I	
	TxSDCC_Dat_1	Transmit Data Communications Channel (Section)	AF20	TTL	I	Transmit section DCC data input
	TxSDCC_Dat_2		AF15	TTL	I	
	TxSDCC_Dat_3		AF10	TTL	I	
	TxSDCC_Dat_4		AD5	TTL	I	
	TxLDCC_Dat_1	Transmit Data Communications Channel (Line)	AE21	TTL	I	Transmit line DCC data input
	TxLDCC_Dat_2		AD15	TTL	I	
	TxLDCC_Dat_3		AE11	TTL	I	
	TxLDCC_Dat_4		AE6	TTL	I	
	LTxSynRef	Line Transmit Reference Sync	P2	TTL	I	Local oscillator reference
	ExtRes	External Bias Resistor	N4	Analog	I	External resistor connection for receive CDR
	RxPLLClk	Receive PLL Clock	N2	TTL	I	Local oscillator reference (19.44 MHz).
	LSigDet_1	Line Signal Detect	F1	TTL or PECL	I	This pin is high when the LIU is receiving a valid signal. When this pin is low, the incoming data is clamped to all zero's to provide proper detection of LOS.
	LSigDet_2		L1	TTL or PECL	I	
	LSigDet_3		T1	TTL or PECL	I	
	LSigDet_4		AA1	TTL or PECL	I	
	LRxClk–_1	Line Receive Clock Negative	H2	Diff PECL	I	155.52/622.08 (Ports 2-4 are OC-3/155.52 MHz only) line receive clock input. An external line-rate clock may optionally be provided on this input to clock the SONET/SDH receive line data when the internal CDR is not being used. This clock source can be selected by bit 5 of the CLKREC register. The clock source have an accuracy of +/- 20 PPM. Tie this pin high through a 10K resistor if unused.
	LRxClk–_2		L2	Diff PECL	I	
	LRxClk–_3		W2	Diff PECL	I	
	LRxClk–_4		AC1	Diff PECL	I	

Table 1-4. Pin Definitions *(3 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Sonet/SDH Line (cont.)	LRxClk+_1	Line Receive Clock Positive	G2	Diff PECL	I	Complement of the above PECL Line Receive Clock input. Tie this pin low through a 10 k resistor if unused.
	LRxClk+_2		M2	Diff PECL	I	
	LRxClk+_3		Y2	Diff PECL	I	
	LRxClk+_4		AB1	Diff PECL	I	
	LRxData–_1	Line Receive Input Negative	G1	Diff PECL	I	SONET/SDH Line Receive Data input.
	LRxData–_2		M1	Diff PECL	I	
	LRxData–_3		U1	Diff PECL	I	
	LRxData–_4		AD1	Diff PECL	I	
	LRxData+_1	Line Receive Input Positive	H1	Diff PECL	I	Complement of the above PECL Line Receive Data input.
	LRxData+_2		N1	Diff PECL	I	
	LRxData+_3		V1	Diff PECL	I	
	LRxData+_4		AE1	Diff PECL	I	
	LRxPFP_1	Receive PLL Filter (Positive)	E4	Analog	I	External RC network pins for PLL. See Figure 2-2.
	LRxPFP_2		K4	Analog	I	
	LRxPFP_3		T4	Analog	I	
	LRxPFP_4		Y4	Analog	I	
	LRxPFN_1	Receive PLL Filter (Negative)	F4	Analog	I	External RC network pins for PLL. See Figure 2-2.
	LRxPFN_2		J4	Analog	I	
	LRxPFN_3		U4	Analog	I	
	LRxPFN_4		AA4	Analog	I	
	LTxData–_1	Line Transmit Output Negative Polarity	E1	Diff PECL	O	SONET/SDH formatted Line Transmit Data.
	LTxData–_2		K1	Diff PECL	O	
	LTxData–_3		R1	Diff PECL	O	
	LTxData–_4		Y1	Diff PECL	O	

Table 1-4. Pin Definitions (4 of 16)

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Sonet/SDH Line (cont.)	LTxData+_1	Line Transmit Output Positive Polarity	D1	Diff PECL	O	Complement of the above PECL Line Transmit Data.
	LTxData+_2		J1	Diff PECL	O	
	LTxData+_3		P1	Diff PECL	O	
	LTxData+_4		W1	Diff PECL	O	
	LTxClk–_1	Line Transmit Clock Output Negative Polarity	C2	Diff PECL	O	622.08/155.52 MHz output derived from one of three clock sources: transmit clock synthesizer, recovered receive clock or the LTxClkI+/- Input. The clock source is selected in bits 3 and 4 of the CLKREC register. It is generally used for diagnostic purposes.
	LTxClk–_2		K2	Diff PECL	O	
	LTxClk–_3		T2	Diff PECL	O	
	LTxClk–_4		AB2	Diff PECL	O	
	LTxClk+_1	Line Transmit Clock Output Positive Polarity	D2	Diff PECL	O	Complement of the above PECL Line Transmit Clock output.
	LTxClk+_2		J2	Diff PECL	O	
	LTxClk+_3		R2	Diff PECL	O	
	LTxClk+_4		AA2	Diff PECL	O	
	TxFrameOut_1	Transmit Frame Reference Output	AC19	TTL	O	8 kHz output derived from the Transmit SONET/SDH frame. See Section 5.1.8.
	TxFrameOut_2		AD14	TTL	O	
	TxFrameOut_3		AD9	TTL	O	
	TxFrameOut_4		AC5	TTL	O	
	TxSDCC_Clk_1	Transmit Section DCC Clock Output	AD19	TTL	O	192 kHz output clock used to sampled the Transmit Section DCC input data (TxSDCC_Dat). See Section 2.4.2.7.
	TxSDCC_Clk_2		AE16	TTL	O	
	TxSDCC_Clk_3		AC10	TTL	O	
	TxSDCC_Clk_4		AF5	TTL	O	
	TxLDCC_Clk_1	Transmit Line DCC Clock Output	AC21	TTL	O	576 kHz output clock used to sample the Transmit Line DCC input data (TxLDCC_Dat). See Section 2.4.3.15.
	TxLDCC_Clk_2		AF16	TTL	O	
	TxLDCC_Clk_3		AD10	TTL	O	
	TxLDCC_Clk_4		AC6	TTL	O	
	TxTstClk	Transmit 19.44 MHz Clock Output	C5	TTL	O	19.44 MHz test clock output generated by the Transmit Synthesizer.

Table 1-4. Pin Definitions *(5 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Sonet/SDH Line (cont.)	RxTstClk_1	Receive 19.44 MHz Clock Output	B3	TTL	O	19.44 MHz test clock output generated by the Receive CDR.
	RxTstClk_2		A3	TTL	O	
	RxTstClk_3		AF3	TTL	O	
	RxTstClk_4		AD4	TTL	O	
	RxFrameOut_1	Receive Frame Reference Output	AE22	TTL	O	8 kHz output derived from the Receive SONET/SDH frame. See Section 5.1.8.
	RxFrameOut_2		AD16	TTL	O	
	RxFrameOut_3		AF12	TTL	O	
	RxFrameOut_4		AE7	TTL	O	
	RxSDCC_Clk_1	Receive Section DCC Clock Output	AD21	TTL	O	192 kHz clock output that is synchronous with the RxSDCC_Dat data stream.
	RxSDCC_Clk_2		AC17	TTL	O	
	RxSDCC_Clk_3		AD11	TTL	O	
	RxSDCC_Clk_4		AF7	TTL	O	
	RxSDCC_Dat_1	Receive Section DCC Data Output	AF22	TTL	O	Data received in Section DCC octets (D1-D3) is output on this pin synchronous with the RxSDCC_Clk clock.
	RxSDCC_Dat_2		AF17	TTL	O	
	RxSDCC_Dat_3		AE13	TTL	O	
	RxSDCC_Dat_4		AD7	TTL	O	
	RxLDCC_Clk_1	Receive Line DCC Clock Output	AC22	TTL	O	576 kHz clock output that is synchronous with the RxLDCC_Dat data stream.
	RxLDCC_Clk_2		AD17	TTL	O	
	RxLDCC_Clk_3		AF13	TTL	O	
	RxLDCC_Clk_4		AC8	TTL	O	
	RxLDCC_Dat_1	Receive Line DCC Data Output	AE23	TTL	O	Data received in Line DCC octets (D4-D12) is output on this pin synchronous with the RxLDCC_Clk clock.
	RxLDCC_Dat_2		AE18	TTL	O	
	RxLDCC_Dat_3		AC12	TTL	O	
	RxLDCC_Dat_4		AE8	TTL	O	
	Rx8kHz_1	Receive 8 kHz Clock	C4	TTL	O	8 kHz clock derived from the “Selected Receive Clock.” See Figure 2-6.
	Rx8kHz_2		A2	TTL	O	
	Rx8kHz_3		AE4	TTL	O	
	Rx8kHz_4		AF4	TTL	O	
Orderwire	TxE1_1	Transmit E1 Orderwire Data Input	AF21	TTL	I	Data to be transmitted in the SONET/SDH E1 octet may be input serially on this pin. See Section 5.1.10.
	TxE1_2		AC15	TTL	I	
	TxE1_3		AF11	TTL	I	
	TxE1_4		AD6	TTL	I	

Table 1-4. Pin Definitions (6 of 16)

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Orderwire	TxE2_1	Transmit E2 Orderwire Data Input	AD20	TTL	I	Data to be transmitted in the SONET/SDH E2 octet may be input serially on this pin. See Section 5.1.10.
	TxE2_2		AE17	TTL	I	
	TxE2_3		AE12	TTL	I	
	TxE2_4		AF6	TTL	I	
	E1E2_sync_1	E1/E2 Sync	AF24	TTL	O	Provides frame sync indication for the RxE1/RxE2 and TxE1/TxE2 inputs and outputs. See Section 5.1.10.
	E1E2_sync_2		AF19	TTL	O	
	E1E2_sync_3		AF14	TTL	O	
	E1E2_sync_4		AE9	TTL	O	
	E1E2_Clk_1	E1/E2 Orderwire Clock	AD23	TTL	O	2.048 MHz bit clock for E1/E2 serial inputs/outputs. See Section 5.1.10.
	E1E2_Clk_2		AD18	TTL	O	
	E1E2_Clk_3		AD13	TTL	O	
	E1E2_Clk_4		AF9	TTL	O	
	RxE1_1	Receive E1 Orderwire Data Output	AF23	TTL	O	Data received from the SONET/SDH E1 octet is output serially on this pin. See Section 5.1.10.
	RxE1_2		AF18	TTL	O	
	RxE1_3		AD12	TTL	O	
	RxE1_4		AF8	TTL	O	
	RxE2_1	Receive E2 Orderwire Data Output	AD22	TTL	O	Data received from the SONET/SDH E2 octet is output serially on this pin. See Section 5.1.10.
	RxE2_2		AE19	TTL	O	
	RxE2_3		AE14	TTL	O	
	RxE2_4		AD8	TTL	O	
Status	StatOut[1]_1	Status Outputs	B14	TTL	O	User defined output indications. See Status Output Control register.
	StatOut[0]_1		C16	TTL	O	
	StatOut[1]_2		A15	TTL	O	
	StatOut[0]_2		B15	TTL	O	
	StatOut[1]_3		A16	TTL	O	
	StatOut[0]_3		C17	TTL	O	
	StatOut[1]_4		B16	TTL	O	
	StatOut[0]_4		D17	TTL	O	

Table 1-4. Pin Definitions *(7 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Microprocessor Interface	MMode	Processor Interface Selection	C8	TTL	I	Selects the type of interface. A logic 1 selects the Motorola MPC860 mode; a logic 0 selects the Mindspeed EBUS mode.
	MClk	Microprocessor Clock	D15	TTL	I	Microprocessor interface clock. Frequencies may range from 8 to 33 MHz.
	MRW*	Microprocessor Read/Write Control	A7	TTL	I	Microprocessor read/write control when the Motorola MPC860 mode is selected via the MMode pin. Microprocessor write control when operating in the Mindspeed EBUS mode
	MRD*	Microprocessor Read Control	D8	TTL	I	Microprocessor read control when operating in the Mindspeed EBUS mode.
	MTS*	Microprocessor Transfer Start	B7	TTL	I	Microprocess transfer start when operating in the Motorola MPC860 mode. Microprocessor address latch when operating in the Mindspeed EBUS mode.
	MCS*	Microprocessor Chip Select	C9	TTL	I	When MCS* is set to a logic “0,” the device is enabled for read and write accesses. When MCS* is set to a logic “1,” the device does not respond to input signal transitions on MClk, MRW*, MRD*, MTS*. Additionally, when MCS* is set to a logic “1,” the MAD[7:0] pins are in a high-impedance state but the MIntr* pin remains operational.
	MA[10]	Microprocessor Address Bus	A8	TTL	I	Address inputs for identifying the register that will be accessed. When operating in the Mindspeed EBUS mode, only pins [10:8] are used for the address and pins [7:0] are unused. The lower 8 bits of the EBUS address are multiplexed on the micro interface data bus (MAD). See Figures 5-5 and 5-6.
	MA[9]		B8	TTL	I	
	MA[8]		A9	TTL	I	
	MA[7]		C10	TTL	I	
	MA[6]		B9	TTL	I	
	MA[5]		D10	TTL	I	
	MA[4]		A10	TTL	I	
	MA[3]		C11	TTL	I	
	MA[2]		B10	TTL	I	
	MA[1]		D12	TTL	I	
	MA[0]		A11	TTL	I	

Table 1-4. Pin Definitions *(8 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Microprocessor Interface (cont.)	MIntr*	Microprocessor Interrupt	A14	TTL	OD	When a logic "0" is read on this pin, the device needs servicing. It remains asserted until the pending interrupt is acknowledged. This pin is an open drain output for an external wired "OR" logic implementation.
	MTA*	Microprocessor Transfer Acknowledge	C15	TTL	OD	Motorola MPC860 microprocessor interface transfer acknowledge. This pin requires an external 1K pull-up resistor. This pin is only used in the Motorola MPC860 microprocessor interface mode.
	MAD[7]	Microprocessor Data Bus	C12	TTL	I/O	These eight bits are a bidirectional data bus for transferring the read and write data. When operating in the EBUS microprocessor interface mode, the data bus is multiplexed with address lines [7:0]. See Figures 5-5 and 5-6.
	MAD[6]		B11	TTL	I/O	
	MAD[5]		A12	TTL	I/O	
	MAD[4]		C13	TTL	I/O	
	MAD[3]		B12	TTL	I/O	
	MAD[2]		C14	TTL	I/O	
	MAD[1]		A13	TTL	I/O	
	MAD[0]		B13	TTL	I/O	
JTAG/Scan	ScanMode	Scan mode	A4	TTL	I	Internal scan control. Tie to ground for normal operation. Set to 1 for the scan test.
	TRST*	JTAG Test Reset	D5	TTL pull-up	I	When this pin is asserted, the internal boundary-scan logic is reset. This pin has an internal pull-up resistor. Note: When JTAG is not used, this pin should be tied either directly to ground or though a 1K or less pull down resistor.
	TCK	JTAG Test Clock	B4	TTL	I	This pin samples the value of TMS and TDI on its rising edge in order to control the boundary-scan operations.
	TMS	JTAG Test Mode Select	C6	TTL pull-up	I	This pin controls the boundary-scan Test Access Port (TAP) controller operation. This pin has an internal pull-up resistor.
	TDI	JTAG Test Data Input	A5	TTL pull-up	I	Serial test data input. This pin has an internal pull-up resistor.
	TDO	JTAG Test Data Output	B5	TTL	O	Serial test data output.

Table 1-4. Pin Definitions *(9 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
SI-Bus Interface	STxPrty_1	SI-Bus Transmit Parity Input	C20	TTL	I	Odd parity calculated over STxData[7:0].
	STxPrty_2		E26	TTL	I	
	STxPrty_3		M25	TTL	I	
	STxPrty_4		Y25	TTL	I	

Table 1-4. Pin Definitions (10 of 16)

	Pin Label	Signal Name	No.	Type	I/O(1)	Description
SI-Bus Interface (cont.)	STxData[7]_1	SI-Bus Port 1 Transmit Data	C18	TTL	I	SI-Bus Port 1 transmit data from the slave device.
	STxData[6]_1		B17	TTL	I	
	STxData[5]_1		A18	TTL	I	
	STxData[4]_1		B18	TTL	I	
	STxData[3]_1		C19	TTL	I	
	STxData[2]_1		A19	TTL	I	
	STxData[1]_1		D19	TTL	I	
	STxData[0]_1		B19	TTL	I	
	STxData[7]_2	SI-Bus Port 2 Transmit Data	C26	TTL	I	SI-Bus Port 2 transmit data from the slave device.
	STxData[6]_2		D24	TTL	I	
	STxData[5]_2		C25	TTL	I	
	STxData[4]_2		E24	TTL	I	
	STxData[3]_2		D26	TTL	I	
	STxData[2]_2		E23	TTL	I	
	STxData[1]_2		D25	TTL	I	
	STxData[0]_2		F24	TTL	I	
	STxData[7]_3	SI-Bus Port 3 Transmit Data	L24	TTL	I	SI-Bus Port 3 transmit data from the slave device.
	STxData[6]_3		K25	TTL	I	
	STxData[5]_3		M23	TTL	I	
	STxData[4]_3		L26	TTL	I	
	STxData[3]_3		M24	TTL	I	
	STxData[2]_3		L25	TTL	I	
	STxData[1]_3		M26	TTL	I	
	STxData[0]_3		N24	TTL	I	
	STxData[7]_4	SI-Bus Port 4 Transmit Data	V26	TTL	I	SI-Bus Port 4 transmit data from the slave device.
	STxData[6]_4		V25	TTL	I	
	STxData[5]_4		W24	TTL	I	
	STxData[4]_4		W26	TTL	I	
	STxData[3]_4		W23	TTL	I	
	STxData[2]_4		W25	TTL	I	
	STxData[1]_4		Y24	TTL	I	
	STxData[0]_4		Y26	TTL	I	

Table 1-4. Pin Definitions *(11 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
SI-Bus Interface (cont.)	STxHSClk_1	SI-Bus High Speed Transmit Clock	A17	TTL	O	A 51.84 MHz clock derived from the 155.52/622.08 MHz SONET/SDH receive line clock. Generated for slave devices that need a STS-1 bit rate clock.
	STxHSClk_2		B26	TTL	O	
	STxHSClk_3		K26	TTL	O	
	STxHSClk_4		U25	TTL	O	
	STxClk_1	SI-Bus Transmit Clock	A20	TTL	O	SI-Bus 19.44 MHz clock used to transfer 8-bit SI-Bus data from the slave devices.
	STxClk_2		E25	TTL	O	
	STxClk_3		P24	TTL	O	
	STxClk_4		AA26	TTL	O	
	STxStart_1	SI-Bus Transmit Start	B20	TTL	O	SI-Bus transmit start sync signal for slave devices. Asserted high for three STxClk cycles to indicate the A1 byte of each STS-1 in a STS-3 signal on the STxData bus.
	STxStart_2		G24	TTL	O	
	STxStart_3		N26	TTL	O	
	STxStart_4		AA24	TTL	O	
	SRxHSClk_1	SI-Bus HS Receive Clock	A22	TTL	O	A 51.84 MHz clock derived from the 155.52/622.08 MHz transmit line clock. Generated for slave devices that need a STS-1 bit rate clock.
	SRxHSClk_2		G26	TTL	O	
	SRxHSClk_3		P25	TTL	O	
	SRxHSClk_4		AB23	TTL	O	
	SRxClk_1	SI-Bus Receive Clock	A21	TTL	O	SI-Bus 19.44 MHz clock used to transfer 8-bit SI-Bus data to the slave devices.
	SRxClk_2		F26	TTL	O	
	SRxClk_3		N25	TTL	O	
	SRxClk_4		AA23	TTL	O	
	SRxStart[3]_1	SI-Bus Receive Start	B21	TTL	O	SI-Bus receive start sync signal for slave devices. Asserted high to indicate the A1 byte of each STS-1 on the SRxData bus.
	SRxStart[2]_1		D21	TTL	O	
	SRxStart[1]_1		C21	TTL	O	
	SRxStart[3]_2		H24	TTL	O	
	SRxStart[2]_2		F25	TTL	O	
	SRxStart[1]_2		F23	TTL	O	
	SRxStart[3]_3		R23	TTL	O	
	SRxStart[2]_3		P26	TTL	O	
	SRxStart[1]_3		R24	TTL	O	
	SRxStart[3]_4		AB24	TTL	O	
	SRxStart[2]_4		AB26	TTL	O	
	SRxStart[1]_4		AA25	TTL	O	

Table 1-4. Pin Definitions (12 of 16)

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
SI-Bus Interface (cont.)	SRxData[7]_1	SI-Bus Receive Data Bus	C22	TTL	O	SI-Bus Port 1 receive data sent to the slave device.
	SRxData[6]_1		D22	TTL	O	
	SRxData[5]_1		B22	TTL	O	
	SRxData[4]_1		A23	TTL	O	
	SRxData[3]_1		C23	TTL	O	
	SRxData[2]_1		B23	TTL	O	
	SRxData[1]_1		A24	TTL	O	
	SRxData[0]_1		B24	TTL	O	
	SRxData[7]_2		H23	TTL	O	
	SRxData[6]_2		G25	TTL	O	
	SRxData[5]_2		J24	TTL	O	
	SRxData[4]_2		H26	TTL	O	
	SRxData[3]_2		H25	TTL	O	
	SRxData[2]_2		J26	TTL	O	
	SRxData[1]_2		K24	TTL	O	
	SRxData[0]_2		J25	TTL	O	
	SRxData[7]_3		T24	TTL	O	
	SRxData[6]_3		R26	TTL	O	
	SRxData[5]_3		R25	TTL	O	
	SRxData[4]_3		T26	TTL	O	
	SRxData[3]_3		U24	TTL	O	
	SRxData[2]_3		T25	TTL	O	
	SRxData[1]_3		U23	TTL	O	
	SRxData[0]_3		U26	TTL	O	
	SRxData[7]_4		AB25	TTL	O	
	SRxData[6]_4		AC26	TTL	O	
	SRxData[5]_4		AC24	TTL	O	
	SRxData[4]_4		AC25	TTL	O	
	SRxData[3]_4		AD26	TTL	O	
	SRxData[2]_4		AE24	TTL	O	
	SRxData[1]_4		AE26	TTL	O	
	SRxData[0]_4		AF25	TTL	O	

Table 1-4. Pin Definitions *(13 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
SI-Bus Interface (cont.)	SRxPrty_1	SI-Bus Receive Parity	A25	TTL	O	Odd parity calculated over SRxData[7:0].
	SRxPrty_2		K23	TTL	O	
	SRxPrty_3		V24	TTL	O	
	SRxPrty_4		AD25	TTL	O	
Supply Power	VDD	Digital Power	D7		—	3.3 V digital power supply
			D11			
			D16			
			D20			
			G23			
			L23			
			T23			
			Y23			
			AC7			
			AC11			
			AC16			
			AC20			

Table 1-4. Pin Definitions (14 of 16)

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Supply Power (cont.)	AVDD	Analog Power	E3		—	3.3 V analog power supply
			F3			
			G3–G4			
			H3–H4			
			J3			
			K3			
			L3			
			M3			
			R3–R4			
			T3			
			U3			
			V3–V4			
			W3			
			Y3			
			AA3			
			AB3			
			AC3			
	VGG	ESD Protection—Voltage Clamp	C7		—	Provides Electrostatic Discharge (ESD) protection and over voltage protection. When the device is used with 5 V devices on the board, tie this pin to 5 V for 5 V signal tolerance. Otherwise, tie to 3.3 V. ***NOTE:*** The 5 V supply must be applied concurrent or ahead of the 3.3 V supply.

Table 1-4. Pin Definitions *(15 of 16)*

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Supply Power (cont.)	VSS	Digital Ground	A26		—	These pins are ground connections.
			B25			
			C24			
			D13–D14			
			D18			
			D23			
			J23			
			K10–K17			
			L11–L17			
			M12–M17			
			N12–N17			
			N23			
			P12–P17			
			P23			
			R12–R17			
			T11–T17			
			U10–U17			
			V23			
			AC9			
			AC13–AC14			
			AC18			
			AC23			
			AD24			
			AE25			
			AF26			

Table 1-4. Pin Definitions (16 of 16)

	Pin Label	Signal Name	No.	Type	I/O[1]	Description
Supply Power (cont.)	AVSS	Analog Ground	A1		—	These pins are ground connections.
			B2			
			C3			
			D4			
			L10			
			M10–M11			
			N3			
			N10–N11			
			P3–P4			
			P10–P11			
			R10–R11			
			T10			
			W4			
			AC4			
			AD3			
			AE2			
			AF1			
Reserved - NC	Reserved - NC	Reserved, Do Not Connect	D3		—	These pins are reserved and must be left unconnected.
			AB4			
			AE3			
			AF2			

(1) KEY:
I = Input
O = Output
OD = Open Drain Output
The symbol (*) indicates Active Low

1.6 Block Diagram and Descriptions

The CX29610 can be used to multiplex and de-multiplex SONET STS-1 SPEs from an interleaved bus format (Mindspeed SI-Bus) to STS-3 or STS-12 formatted data streams. The device can be operated as a single STS-12 to STS-1 demultiplexer or as a quad STS-3 to STS-1 demultiplexer. Data flow diagrams are shown for the STS-12 and 4xSTS-3 modes in Figure 1-4 and Figure 1-5, respectively.

Figure 1-4. STS-12 Mode Data Flow Diagram

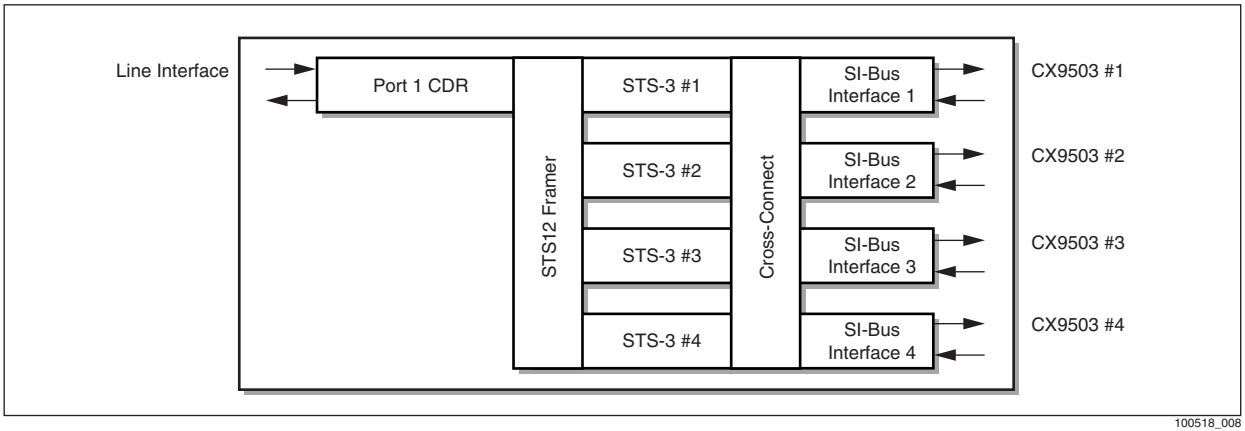
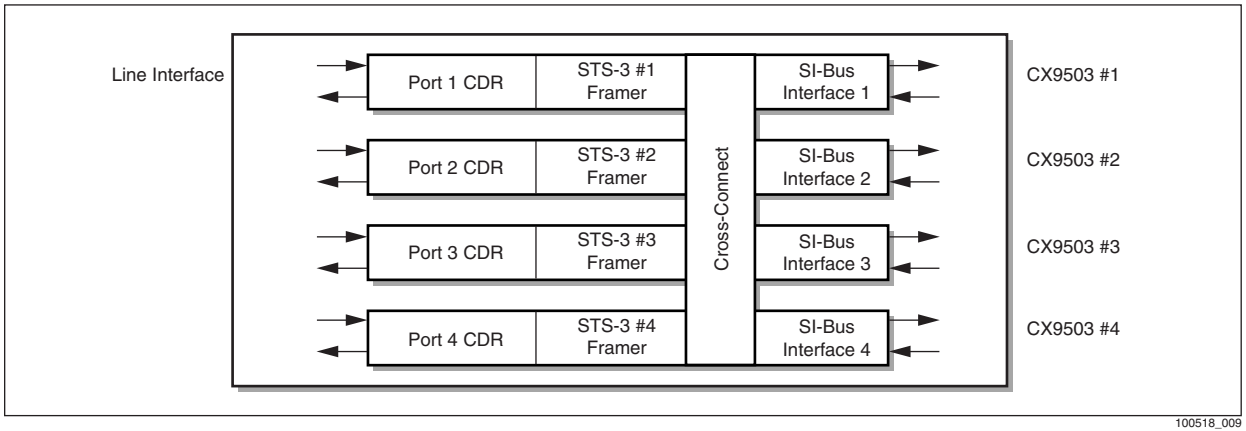
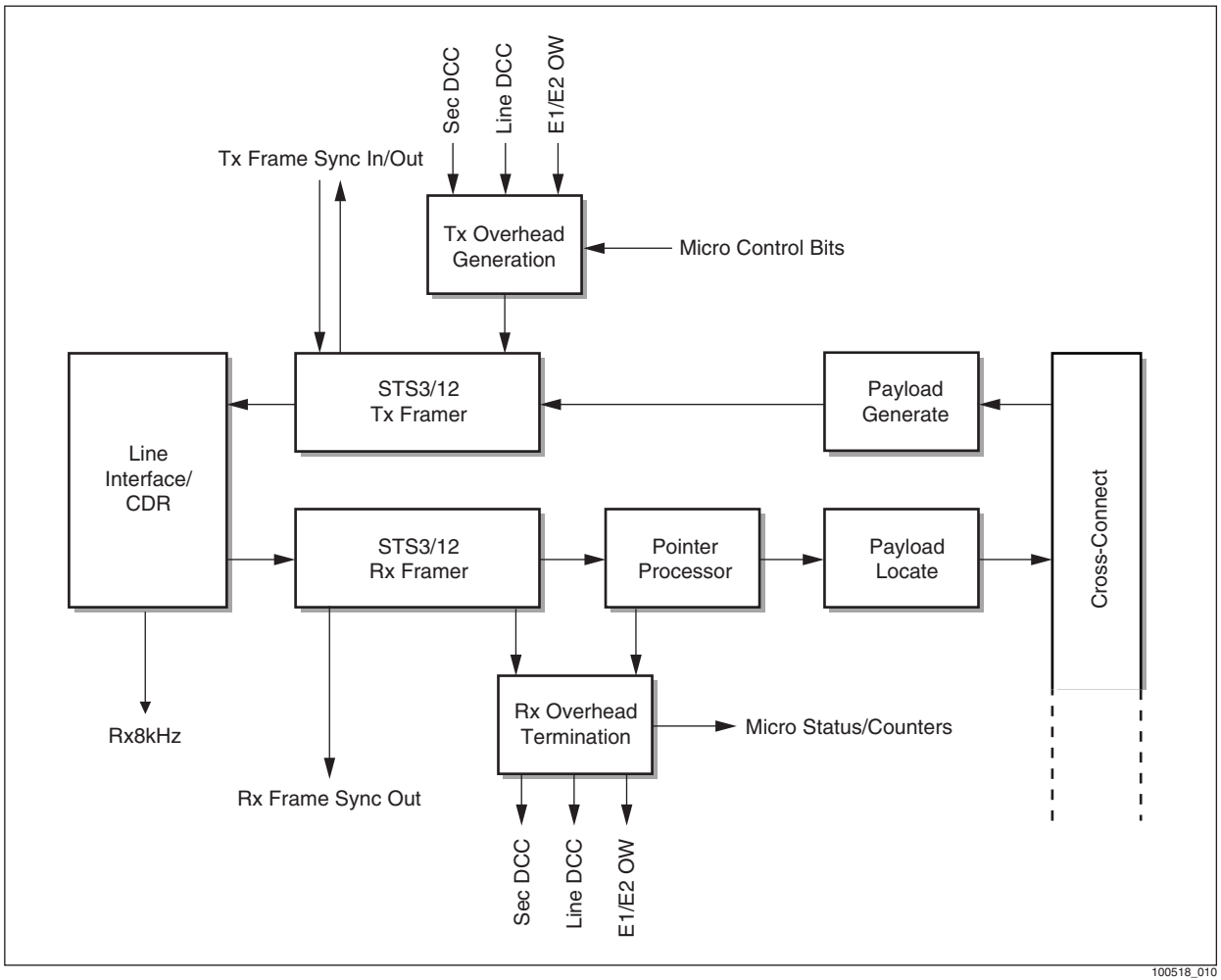


Figure 1-5. 4xSTS-3 Mode Data Flow Diagram



The device provides overhead generation and termination for STS-12 and STS-3 section, line, and path overhead. External serial access for section and line DCCs and for the E1/E2 orderwire channels is provided for each port. A serial, differential clock and data interface to external clock and data recovery devices is provided for the transmit and receive line interfaces. Internal clock synthesis and clock/data recovery capability is also provided. Figure 1-6 shows a block diagram of an individual framer.

Figure 1-6. Framer Block Diagram

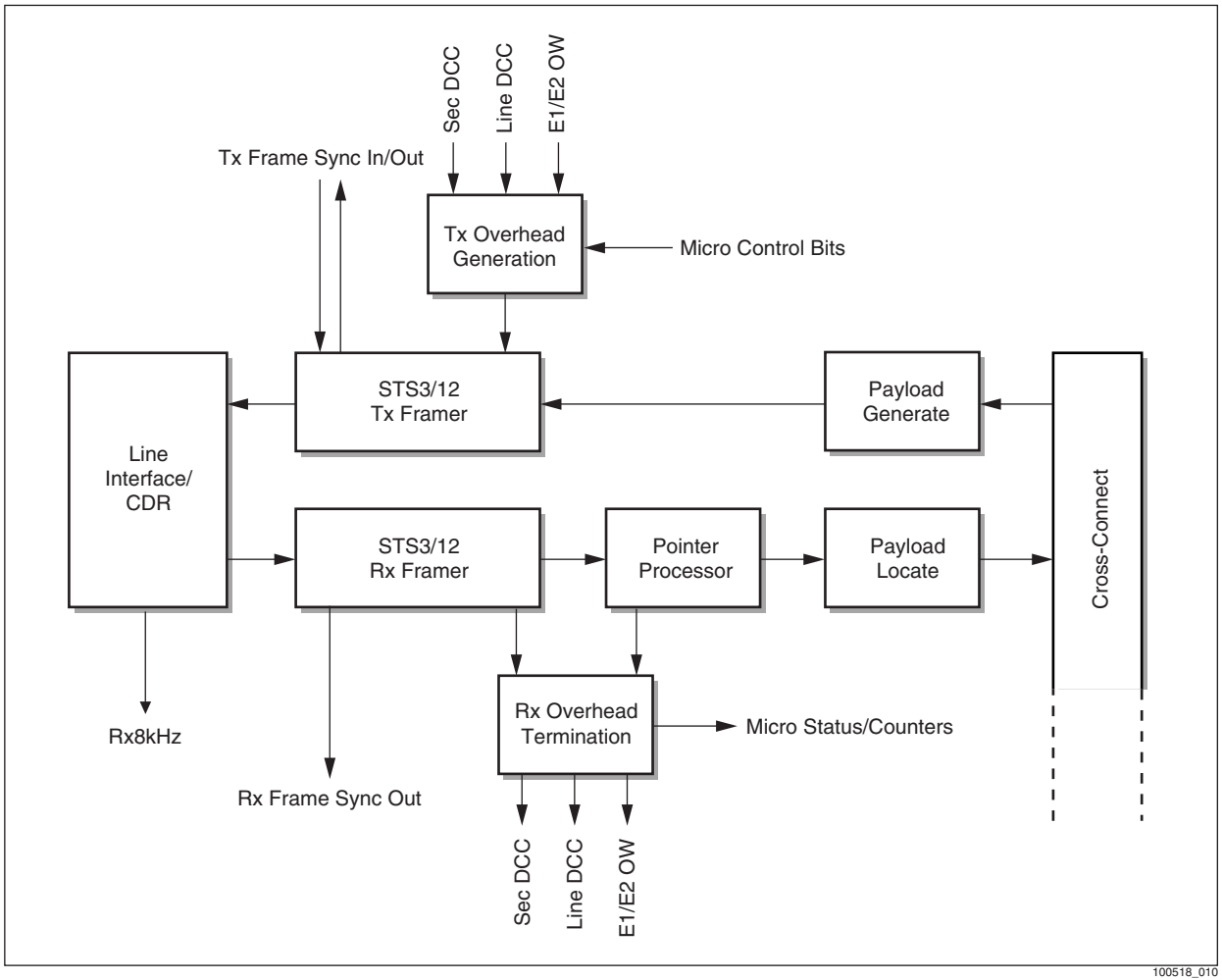


An STS-3 level cross-connect function allows any of the incoming STS-3s (either from separate ports or de-multiplexed from an STS-12) to be routed to any of four SI-Bus interfaces. The SI-Bus interfaces carry the 12 STS-1 streams to downstream devices in an interleaved format. The SONET Interleave Bus (SI-Bus) is defined in Section 2.5. An 8-bit microprocessor interface provides access to configuration, status and counter registers.

2.0 Functional Description

This chapter describes the CX29610 architecture and functional blocks. Figure 2-1 shows the CX29610's transmit and receive signal path.

Figure 2-1. CX29610 Block Diagram



2.1 Line Interface

The CX29610 communicates with the external SONET/SDH network through its line interface, which can connect to a optical trasnceiver enabling transmission over a fiber optic cable. The CX29610 recovers a receive clock from the incoming receive data via an onboard PLL circuit. The receive PLL requires a 19.44 MHz reference clock to be supplied on the RxPLLClk input. A transmit PLL synthesizes a transmit clock from a 19.44 MHz reference clock supplied on the LTxSynRef input. The RxPLLClk and LTxSynRef may be connected to a common 19.44 MHz clock source. The line interface is a Low Voltage Pseudo-Emitter Coupled Logic (PECL) interface.

A PECL device requires the same voltage differential on the inputs as an Emitter Coupled Logic (ECL) device. The PECL device is referenced to a positive source, which is generally 3.3 V or 5.0 V. Use caution when interfacing components that use different V_{cc} levels.

The CX29610 has five pairs of differential PECL pins: LTxClkI+/–, LTxClkO+/–, LRxClk+/–, LTxDat+/–, and LRxDat+/–, which are described in Table 1-4. All inputs and outputs include a positive pin and a negative pin. The voltage difference between the two pins determines the logic value under normal operating conditions. The input logic for this PECL interface is shown in Table 2-1.

Table 2-1. PECL Input Logic Table

Input +	Input –	Internal Logic Level
0	0	Invalid
0	1	0
1	0	1
1	1	Invalid

The output logic table for this PECL interface is shown in Table 2-2.

Table 2-2. PECL output Logic Table

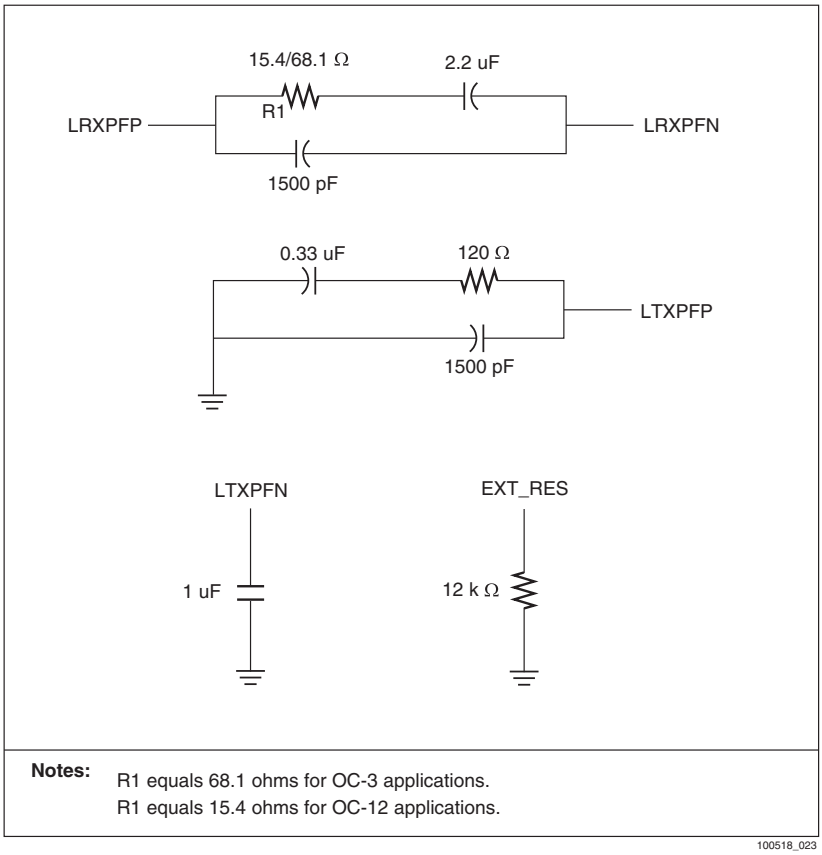
Internal Logic Level	Output +	Output –
0	0	1
1	1	0

See Section 5.3.4 and Section 5.3.5 for examples on how to properly interface fiber optic transceivers to the CX29610's PECL interface.

2.1.1 Transmit and Receive PLL Filter Networks

External filter networks are required by the transmit and receive Phase Locked Loop (PLL) as shown in Figure 2-2. These components should be located as close to the device as possible.

Figure 2-2. PLL Bias Network



Notes: R1 equals 68.1 ohms for OC-3 applications.
R1 equals 15.4 ohms for OC-12 applications.

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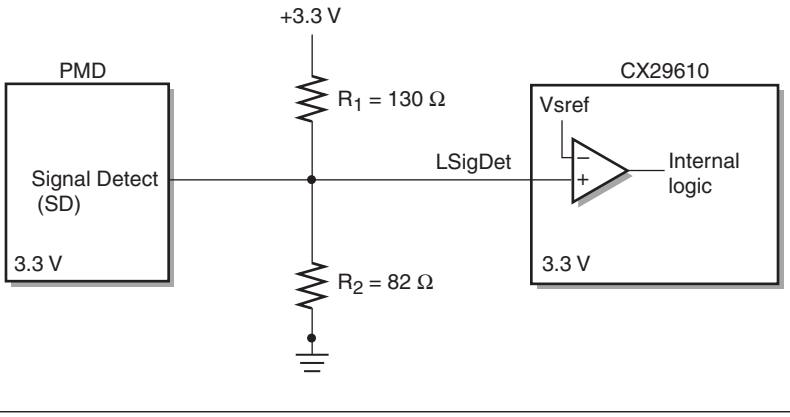
2.1.2 Signal Detect Interface

The LSigDet pin on the CX29610 indicates when the PMD has lost its signal. If the LSigDet goes low, the CX29610 internally forces its receive data to logic ‘0’ to prevent false framing indications. Designs that do not use the LSigDet input must tie this pin high and then ensure that they either externally force the receive data to a logic ‘0’ or detect false framing indications with software.

The LSigDet pin can be driven by TTL or PECL drivers. The CX29610 can be connected directly to a TTL interface without external components. When using a single-ended PECL interface, a standard PECL termination of 50 Ω to V_{cc} – 2 V is required for most PMDs. The PECL termination can be implemented by using the Thevenin equivalent circuit shown in Figure 2-3.

Figure 2-3. Single-ended PECL Diagram



Note:
The termination network shown is valid for a 3.3 V PMD. For a 5.0 V PMD, please refer to Figure 5-17.

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2.2 Clock Circuits

The CX29610 has four transceiver blocks comprised of a PECL interface, a CDR circuit, a serial to parallel, and a parallel to serial circuit as shown in Figure 2-4. One transmit synthesizer circuit generates a transmit line clock for all four ports. The transceiver and synthesizer blocks operate at OC-12 (622 Mbps) for port one and OC-3 (155 Mbps) for all four ports.

There are several muxes at different inputs and outputs of each transceiver block to provide test options for production, evaluation, and system level testing. The muxes which select different clock and data path options are shown in Figures 2-5 and 2-6 along with the register names and associated control bits.

Figure 2-4. Functional Block Diagram

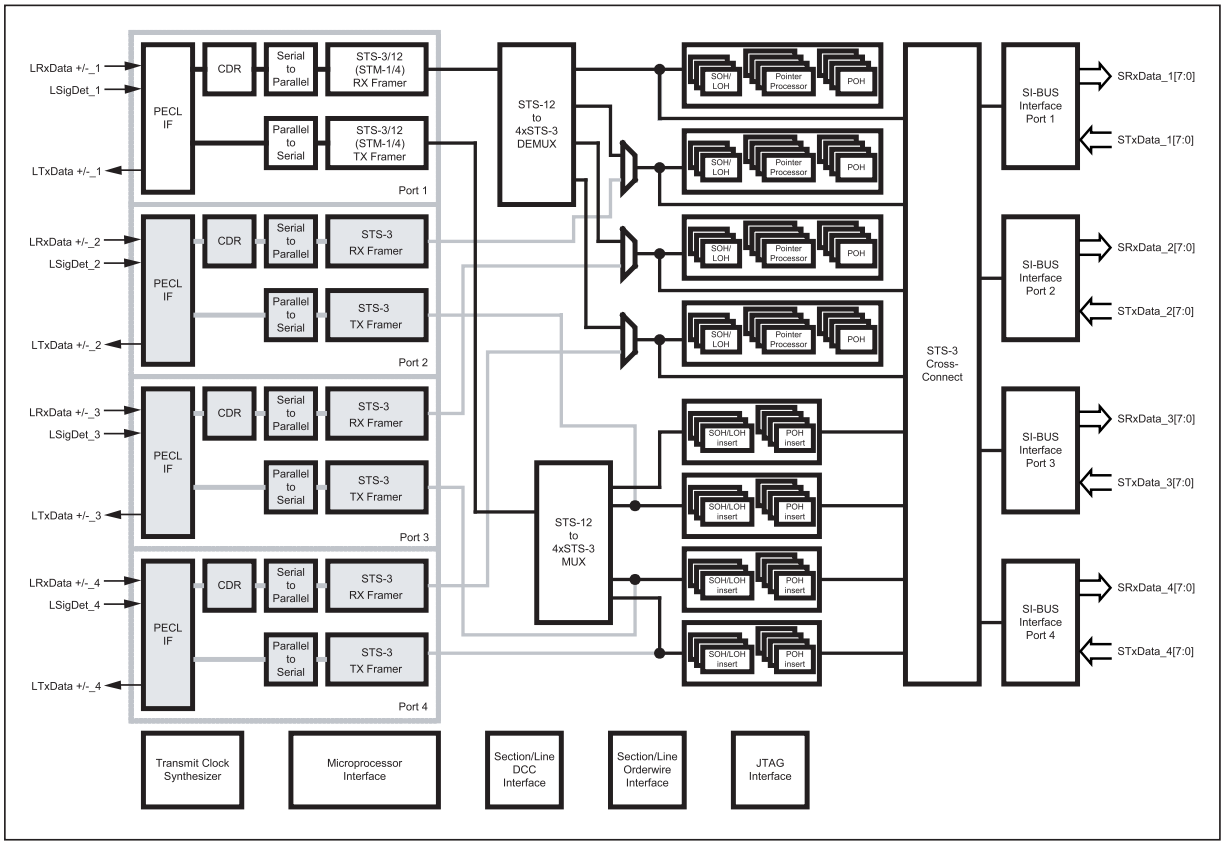


Figure 2-5. Receive Clock Generation and Data Path

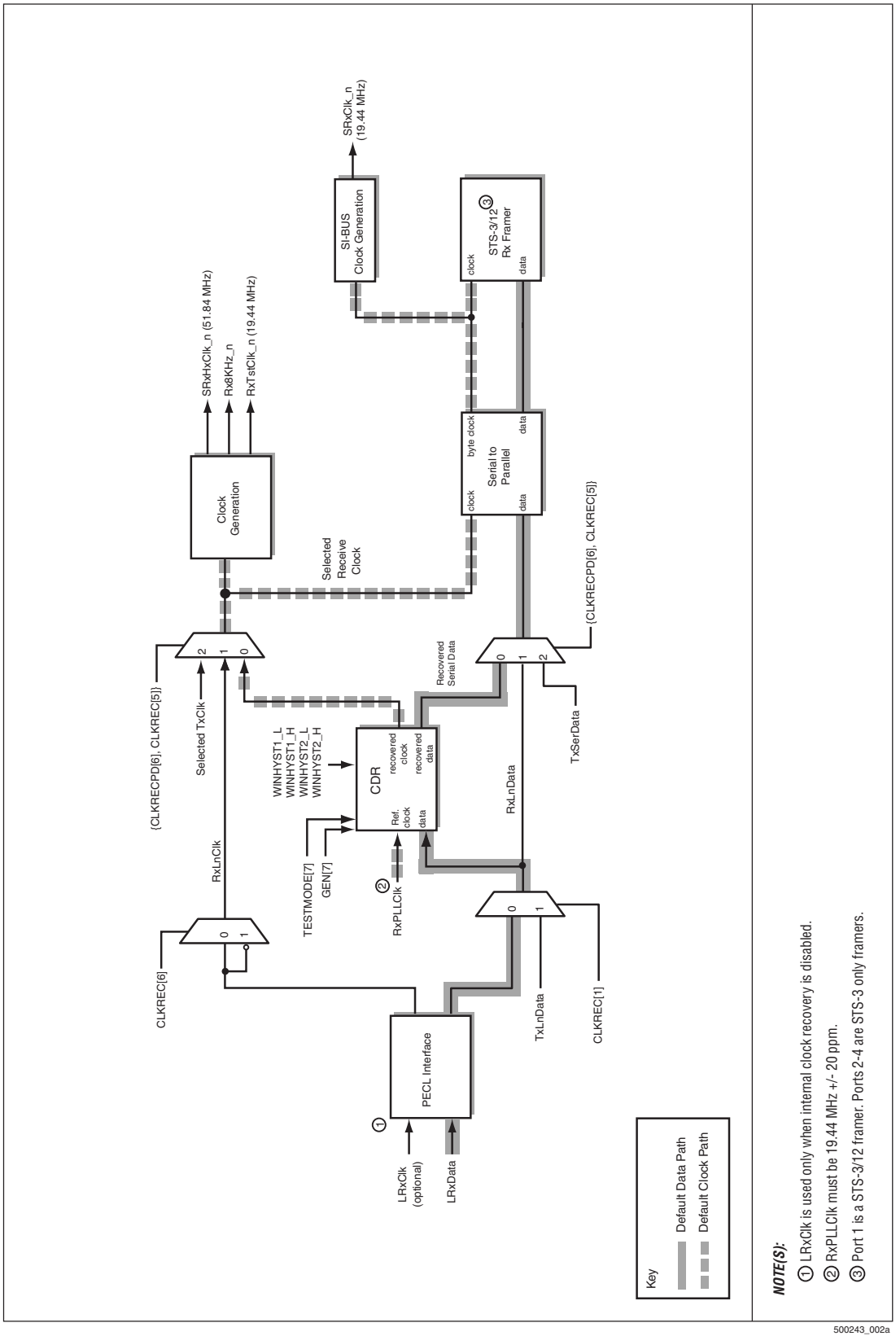
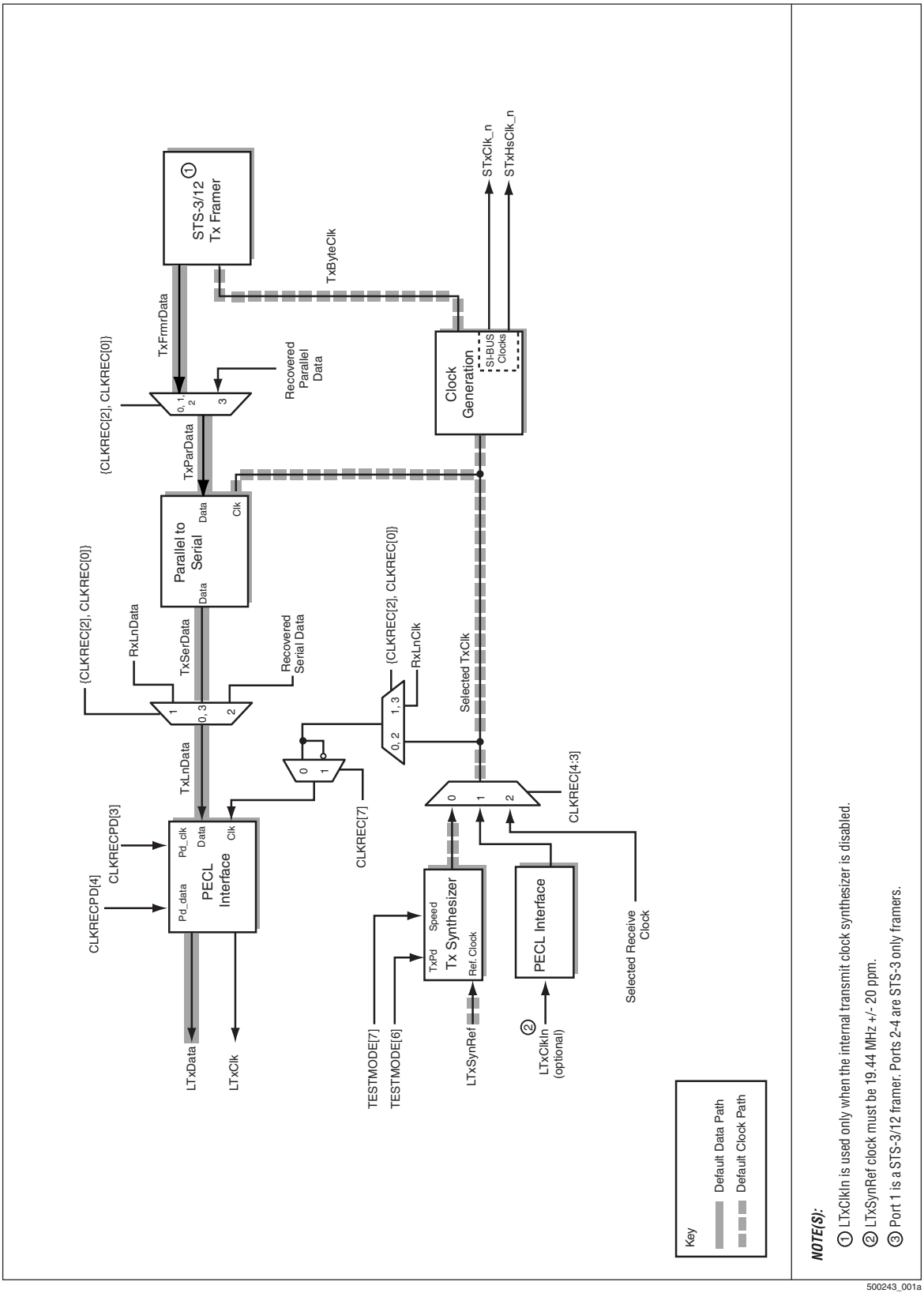


Figure 2-6. Transmit Clock Generation and Data Path



The line interface circuits of the CX29610 provide many clock and data path selections for loopback capabilies. The available loopback modes are described in Section 2.8.

Table 2-3 shows the register bits which are required for proper configuration of the the line interface for the OC-12 SONET mode. This is the default mode of operation upon device reset. The control registers shown in Figures 2-5 and 2-6.

Table 2-3. Transmit/Receive Default Clock Configuration

Configuration Description	Control Register and Bit Position Index	Register Bit Names and Values	Default Register Value
SONET STS-12	GEN[7]	PrtMode = 1	GEN = 0x80
Internal CDR enabled	CLKREC[5]	ExtClkRec = 0	CLKREC = 0x00
Transmit clock synthesized from 19.44 MHz reference input (LTxSynRef pin)	CLKREC[4:3]	TxClkSel[1:0] = 00	
LTxData sourced from transmit framer	CLKREC[2]	TxDataSel = 0	
Receive data from LRxData +/- inputs	CLKREC[1]	SrcLoop = 0	
PECL line loopback disabled	CLKREC[0]	NELnLoop = 0	
Local source loopback disabled	CLKRECPD[6]	LclSrcLoop = 0	CLKRECPD = 0x08
LTxData buffer enabled	CLKRECPD[4]	PD_Data = 0	
LTxClk buffer power down enabled	CLKRECPD[3]	PD_Clk = 1	
CDR charge pump frequency - 622 MHz	TESTMODE[7]	Speed_CP = 1	TESTMODE = 0x80
Transmit clock synthesizer enabled	TESTMODE[6]	Pd_TxSyn = 0	
CDR PLL hysteresis values	WINHYST1_L WINHYST		

The transmit section synthesizes the 155.52/622.08 MHz clock used for transmitting data from one of four sources based on the control bits TxClkSel[1:0] in the CLKREC register as shown in Table 2-4.

Table 2-4. TxClkSel[1:0] Control Bits

TxClkSel1	TxClkSel0	Transmit Clock
0	0	Synthesized from the 19.44 MHz reference on the LTxSynRef pin (default).
0	1	Taken directly from the LTxClkIn+/–_n input pins. This 155.52 MHz clock must meet jitter specifications. For Port 1, this may also be a 622.08 MHz clock for OC-12 operation.
1	0	Uses the recovered clock from the CDR block for loop timed operations.
1	1	Reserved.

The receiver section uses an internal Phase Locked Loop (PLL) to recover the clock from the incoming NRZ data stream. The clock recovery circuit requires the 19.44 MHz clock. When no NRZ data is present or when the signal detect input (LSigDet_n) is low, indicating that the signal has been lost by the optical transceiver, the receive clock recovery circuit free-runs at a nominal 155.52 MHz (622.08) so that a receive clock is always present for the receive data path and the transmit path for loop-timed applications.

This clock meets jitter tolerance and jitter transfer specifications according to Bellcore GR-253 (see Figure 2-7, Table 2-5, and Table 2-6). Jitter tolerance is defined as how much jitter the receiver can tolerate and still extract the correct data from the incoming signal. Jitter transfer is the maximum amount of jitter that any device is allowed to add to the data stream.

Figure 2-7. Bellcore GR-253-CORE Jitter Specifications

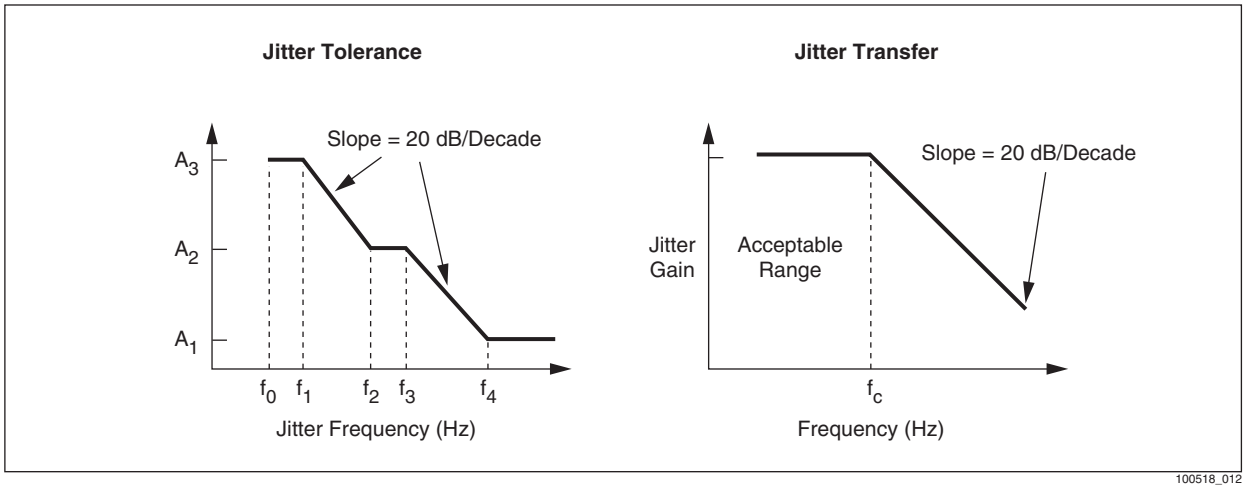


Table 2-5. SONET Category II Jitter Tolerance Mask

OC/STS Level	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (Hz)	f_4 (Hz)	A_1 (UI_{pp})	A_2 (UI_{pp})	A_3 (UI_{pp})
3	10	30	300	6.5 k	65 k	0.15	1.5	15
12	10	30	300	25 k	250 k	0.15	1.5	15

Table 2-6. Category II Jitter Transfer Mask

OC/STS Level	f_c (Hz)	P (dB)
3	130	0.1
12	500	0.1

Table 2-7. CX29610 Jitter Specification

Parameter	Min	Typical	Max	Unit
Jitter Generation (Tx Output)	—	0.004	0.006	UI_{rms}
Jitter Generation	—	—	0.06	UI_{pp}
Jitter Generation (loopback from Rx to Tx)	—	0.005	0.007	UI_{rms}
Adjacent Channel Isolation	—	40	—	dB
Rise/Fall Time	—	120	150	ps

2.2.1 Loss of Lock

When the CDR determines that a Loss of Lock (also referred to as a Loss of Synchronization) has occurred, it asserts the Loss of Lock (LOL) bit in the RXSEC register and the LOL bit in the SECINT register. In addition, if enabled by the EnLOL bit in the ENSEC register, the interrupt will be propagated to the PORTINT register.

2.3 Device Configuration and Setup

The following information illustrates how to configure the CX29610 for various SONET and SDH operating modes. The device can operate in either a OC-12/STM-4 or a 4xOC-3/STM-1 configuration. The device has four sets of registers for each physical line port (1-4) when operating in the 4xOC-3/STM-1 mode. When operating in the OC-12/STM-4 mode, with only one physical line port active (i.e., port 1), registers labeled as ports 2–4 are reconfigured to control and monitor the larger set of section, line, and path bytes.

Table 2-8. Valid Framing Modes for the CX29610

Gen Register				Description
PrtMode (bit 7)	**FrmMode (bit 6)**	**AU4Mode (bit 5)**	**TU3Mode (bit 3)**	
0	0	0	0	SONET; 4 independent OC-3s
1	0	0	0	SONET OC-12
0	1	0	0	SDH; 4 independent AU-3s
0	1	1	0	SDH; 4 independent AU-4s with TUG-2 payload
0	1	1	1	SDH; 4 independent AU-4s with TU-3 payload
1	1	0	0	SDH; STM-4; AU-3 to TUG-2
1	1	1	0	SDH; STM-4; TUG-3 to TUG-2
1	1	1	1	SDH; STM-4; TUG-3 to TU-3

The GEN register selects the mapping format for the CX29610.

The PrtMode bit configures the device as either four independent STS-3/STM-1 ports or a single STS-12/STM-4. (The SI-Bus is always four independent OC-3/STM-1 data streams.)

The FrmMode bit selects between SONET and SDH framing modes. This determines what values are transmitted in the J0/Z0 overhead octets as shown in Table 2-11.

The AU4Mode and TU3Mode bits determine how the payload is mapped for the SDH modes. Consult the appropriate standard's document (G.707 or Bell CORE-253) for details.

Figure 2-8. Default Clock and Data Receive Path

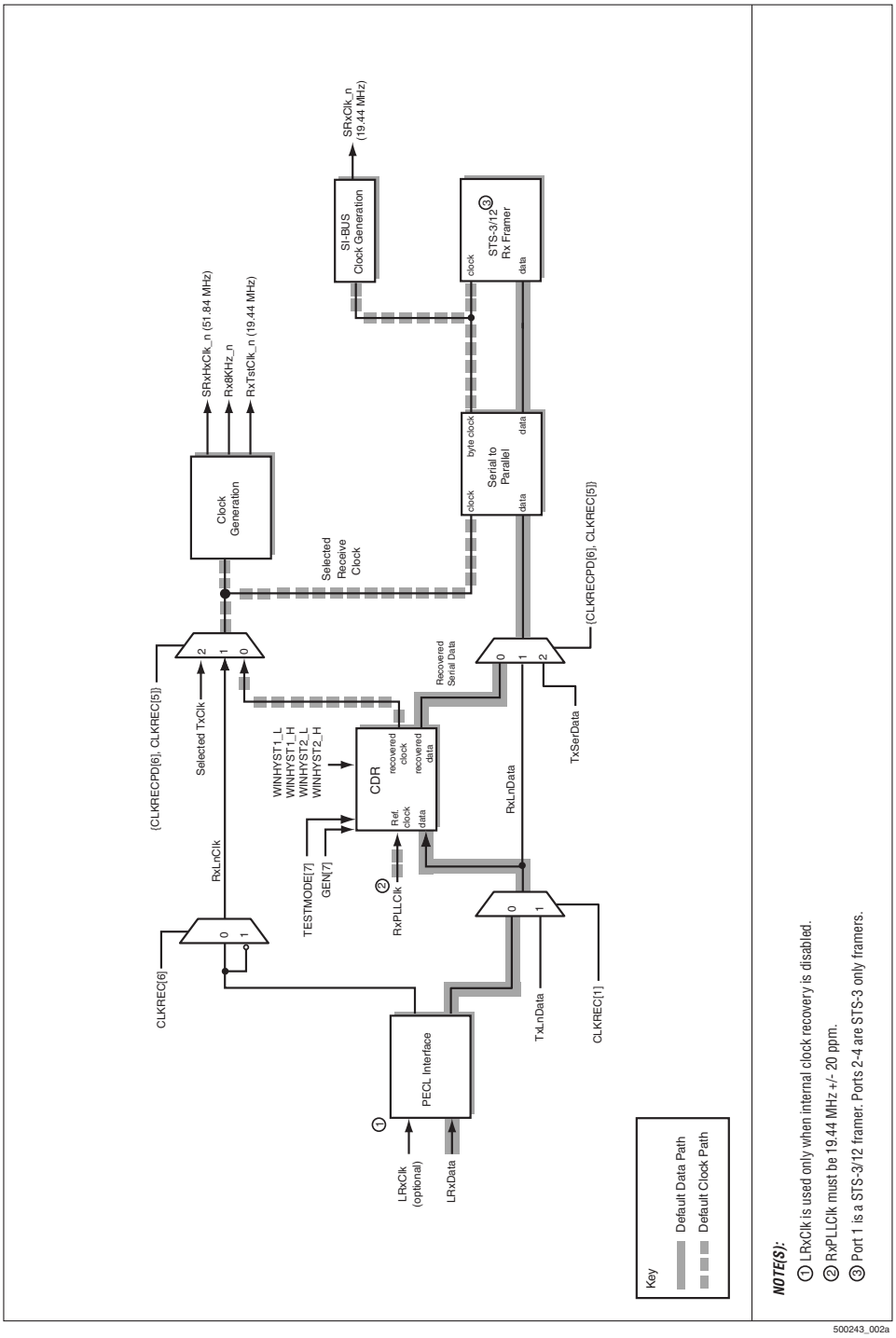


Figure 2-9. Default Clock and Data Transmit Path

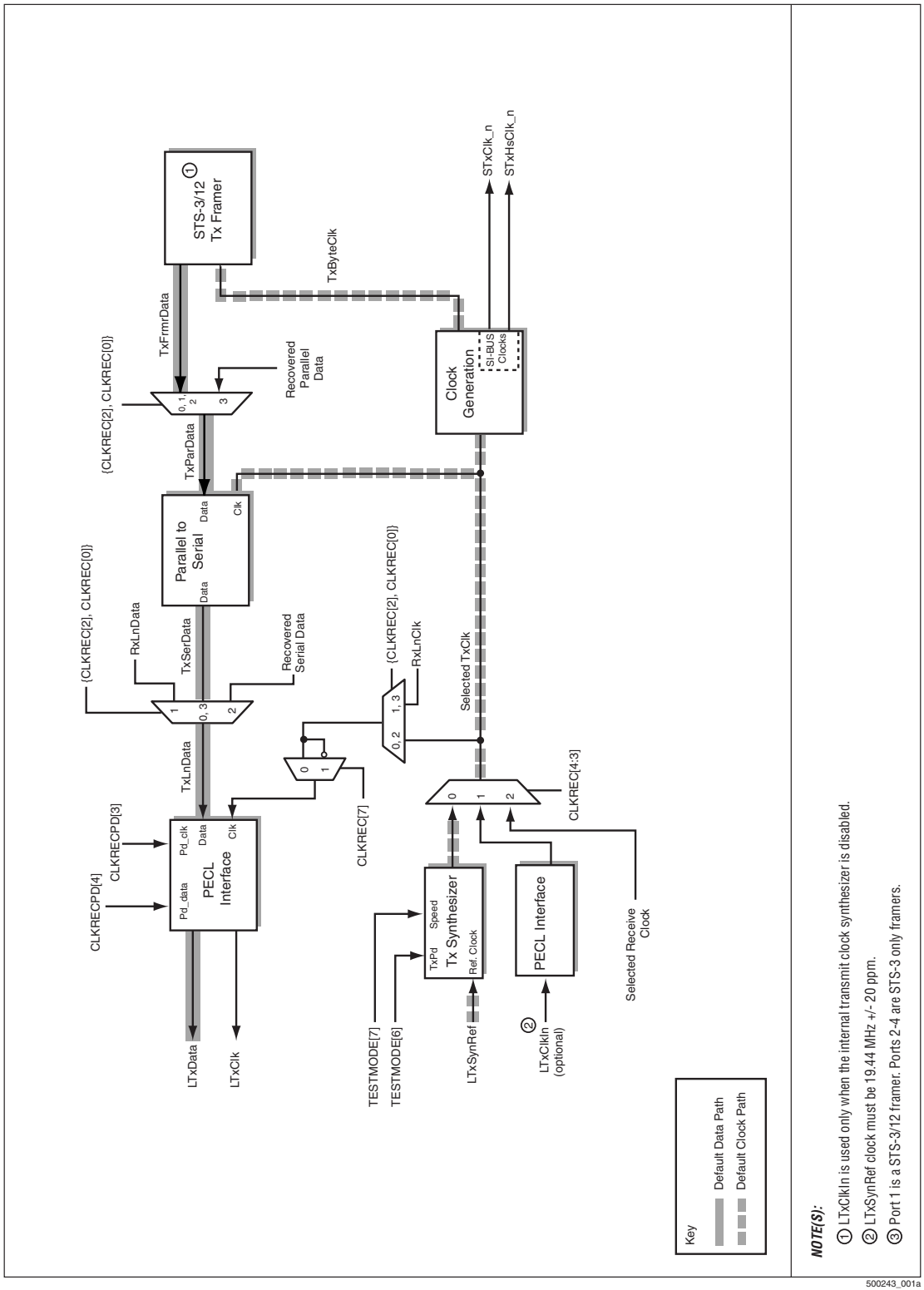


Table 2-9 shows the register bits which are required for proper configuration of the line interface for the OC-12 SONET mode.

The line interface circuits of the CX29610 provide many clock and data path selections for loopback capabilies. The available loopback modes are described in Section 2.8.

Table 2-9. Transmit/Receive Configuration: OC-12 Mode, Internal CDR and Transmit Clock Synthesis Enabled

Configuration Description	Control Register and Bit Position Index	Register Bit Names and Values	Default Register Value
SONET STS-12	GEN[7]	PrtMode = 1	GEN = 0x80
Internal CDR enabled	CLKREC[5]	ExtClkRec = 0	CLKREC = 0x00
Transmit clock synthesized from 19.44 MHz reference input (LTxSynRef pin)	CLKREC[4:3]	TxClkSel[1:0] = 00	
LTxData sourced from transmit framer	CLKREC[2]	TxDataSel = 0	
Receive data from LRxData +/- inputs	CLKREC[1]	SrcLoop = 0	
PECL line loop disabled	CLKREC[0]	NELnLoop = 0	
Local Source Loopback disabled	CLKRECPD[6]	LclSrcLoop = 0	CLKRECPD = 0x08
LTxData buffer enabled	CLKRECPD[4]	PD_Data = 0	
LTxClk buffer power down enabled	CLKRECPD[3]	PD_Clk = 1	
CDR charge pump frequency - 622 MHz	TESTMODE[7]	Speed_CP = 1	TESTMODE = 0x80
Transmit clock synthesizer enabled	TESTMODE[6]	Pd_TxSyn = 0	

2.4 SONET/SDH Framer and Overhead Processor

Mindspeed's CX29610 SONET/SDH framer has an extensive overhead processing section with external access for D1-D3 and D4-D12 Data Link message processing. The framer provides data transmission at a standard bit rate, frequency justification, pointer processing, and frame delineation. The overhead processor provides frame synchronization, byte scrambling and descrambling, and byte multiplexing and demultiplexing. Figures 2-10 through 2-16 and Table 2-10 illustrate the mapping supported by the CX29610.

Table 2-10. Valid Framing Modes for the CX29610

Gen Register				Description
PrtMode (bit 7)	FrmMode (bit 6)	AU4Mode (bit 5)	TU3Mode (bit 3)	
0	0	0	0	SONET; 4 independent OC-3s
1	0	0	0	SONET OC-12
0	1	0	0	SDH; 4 independent AU-3s
0	1	1	0	SDH; 4 independent AU-4s with TUG-2 payload
0	1	1	1	SDH; 4 independent AU-4s with TU-3 payload
1	1	0	0	SDH; STM-4; AU-3 to TUG-2
1	1	1	0	SDH; STM-4; TUG-3 to TUG-2
1	1	1	1	SDH; STM-4; TUG-3 to TU-3

The GEN register selects the mapping format for the CX29610.

The PrtMode bit configures the device as either four independent STS-3/STM-1 ports or a single STS-12/STM-4. (The SI-Bus is always four independent OC-3/STM-1 data streams.)

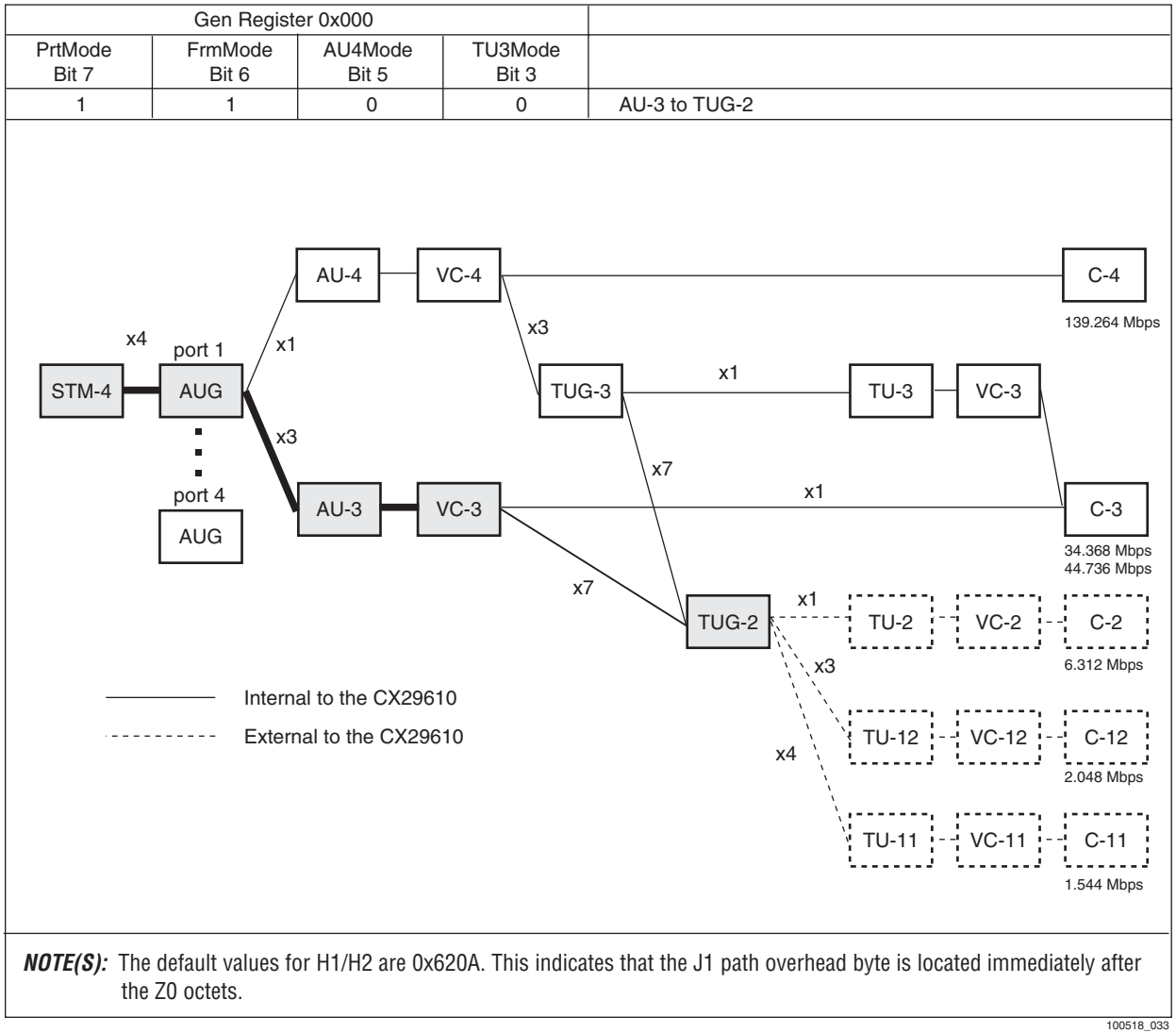
The FrmMode bit selects between SONET and SDH framing modes. This determines what values are transmitted in the J0/Z0 overhead octets as shown in Table 2-11.

The AU4Mode and TU3Mode bits determine how the payload is mapped for the SDH modes. Consult the appropriate standard's document (G.707 or Bell CORE-253) for details.

Table 2-11. Default J0/Z0 Transmitted Values

	Transmitted Values											
	J0	**Z0-2**	**Z0-3**	**Z0-4**	**Z0-5**	**Z0-6**	**Z0-7**	**Z0-8**	**Z0-9**	**Z0-10**	**Z0-11**	**Z0-12**
STM-1/STS-3	01	02	03	—	—	—	—	—	—	—	—	—
STS-12 FrmMode=0	01	02	03	04	05	06	07	08	09	0A	0B	0C
STM-4 FRMMode = 1	01	02	03	04	AA	AA	AA	AA	AA	AA	AA	AA

Figure 2-10. AU-3 to TUG-2



NOTE(S): The default values for H1/H2 are 0x620A. This indicates that the J1 path overhead byte is located immediately after the Z0 octets.

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Figure 2-11. AU-3 Basic Frame (STM-4 to 4 x AUG to 3 x AU-3 Mapping)

Row	Column 1											
1	A1-1 A1/A2 port 1	A1-2 A1/A2 port 1	A1-3 A1/A2 port 1	A1-4 A1/A2 port 1	A1-5 A1/A2 port 1	A1-6 A1/A2 port 1	A1-7 A1/A2 port 1	A1-8 A1/A2 port 1	A1-9 A1/A2 port 1	A1-10 A1/A2 port 1	A1-11 A1/A2 port 1	A1-12 A1/A2 port 1
2	B1 B1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D1 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H1-1 TxPntr port 1 path 1	H1-2 TxPntr port 2 path 1	H1-3 TxPntr port 3 path 1	H1-4 TxPntr port 4 path 1	H1-5 TxPntr port 1 path 2	H1-6 TxPntr port 2 path 2	H1-7 TxPntr port 3 path 2	H1-8 TxPntr port 4 path 2	H1-9 TxPntr port 1 path 3	H1-10 TxPntr port 2 path 3	H1-11 TxPntr port 3 path 3	H1-12 TxPntr port 4 path 3
5	B2-1 InsB2Err1 port 1	B2-2 InsB2Err1 port 2	B2-3 InsB2Err1 port 3	B2-4 InsB2Err1 port 4	B2-5 InsB2Err2 port 1	B2-6 InsB2Err2 port 2	B2-7 InsB2Err2 port 3	B2-8 InsB2Err2 port 4	B2-9 InsB2Err3 port 1	B2-10 InsB2Err3 port 2	B2-11 InsB2Err3 port 3	B2-12 InsB2Err3 port 4
6	D4 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D7 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D10 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	S1 S1 port 1	0	0	0	0	0	0	0	0	0	0	0

Row	Column 2											
1	A2-1 A1/A2 port 1	A2-2 A1/A2 port 1	A2-3 A1/A2 port 1	A2-4 A1/A2 port 1	A2-5 A1/A2 port 1	A2-6 A1/A2 port 1	A2-7 A1/A2 port 1	A2-8 A1/A2 port 1	A2-9 A1/A2 port 1	A2-10 A1/A2 port 1	A2-11 A1/A2 port 1	A2-12 A1/A2 port 1
2	E1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D2 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H2-1 TxPntr port 1 path 1	H2-2 TxPntr port 2 path 1	H2-3 TxPntr port 3 path 1	H2-4 TxPntr port 4 path 1	H2-5 TxPntr port 1 path 2	H2-6 TxPntr port 2 path 2	H2-7 TxPntr port 3 path 2	H2-8 TxPntr port 4 path 2	H2-9 TxPntr port 1 path 3	H2-10 TxPntr port 2 path 3	H2-11 TxPntr port 3 path 3	H2-12 TxPntr port 4 path 3
5	K1 K1 port 1	0	0	0	0	0	0	0	0	0	0	0
6	D5 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D8 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D11 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	0	0	M1 REI-L port 1	0	0	0	0	0	0	0	0	0

Row	Column 3											
1	J0 TxSec port 1	Z0-2 Gen	Z0-3 Gen	Z0-4 Gen	Z0-5 Gen	Z0-6 Gen	Z0-7 Gen	Z0-8 Gen	Z0-9 Gen	Z0-10 Gen	Z0-11 Gen	Z0-12 Gen
2	F1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D3 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H3-1 TxPntr port 1 path 1	H3-2 TxPntr port 2 path 1	H3-3 TxPntr port 3 path 1	H3-4 TxPntr port 4 path 1	H3-5 TxPntr port 1 path 2	H3-6 TxPntr port 2 path 2	H3-7 TxPntr port 3 path 2	H3-8 TxPntr port 4 path 2	H3-9 TxPntr port 1 path 3	H3-10 TxPntr port 2 path 3	H3-11 TxPntr port 3 path 3	H3-12 TxPntr port 4 path 3
5	K2 K2 port 1	0	0	0	0	0	0	0	0	0	0	0
6	D6 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D9 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D12 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	E2 E2 port 1	0	0	0	0	0	0	0	0	0	0	0

Row	Column 4											
1	J1-1 port 1 path 1	J1-2 port 2 path 1	J1-3 port 3 path 1	J1-4 port 4 path 1	J1-5 port 1 path 2	J1-6 port 2 path 2	J1-7 port 3 path 2	J1-8 port 4 path 2	J1-9 port 1 path 3	J1-10 port 2 path 3	J1-11 port 3 path 3	J1-12 port 4 path 3
2	B3-1 port 1 path 1	B3-2 port 2 path 1	B3-3 port 3 path 1	B3-4 port 4 path 1	B3-5 port 1 path 2	B3-6 port 2 path 2	B3-7 port 3 path 2	B3-8 port 4 path 2	B3-9 port 1 path 3	B3-10 port 2 path 3	B3-11 port 3 path 3	B3-12 port 4 path 3
3	C2-1 port 1 path 1	C2-2 port 2 path 1	C2-3 port 3 path 1	C2-4 port 4 path 1	C2-5 port 1 path 2	C2-6 port 2 path 2	C2-7 port 3 path 2	C2-8 port 4 path 2	C2-9 port 1 path 3	C2-10 port 2 path 3	C2-11 port 3 path 1	C2-12 port 4 path 3
4	G1-1 port 1 path 1	G1-2 port 2 path 1	G1-3 port 3 path 1	G1-4 port 4 path 1	G1-5 port 1 path 2	G1-6 port 2 path 2	G1-7 port 3 path 2	G1-8 port 4 path 2	G1-9 port 1 path 3	G1-10 port 2 path 3	G1-11 port 3 path 1	G1-12 port 4 path 3
5	F2-1 port 1 path 1	F2-2 port 2 path 1	F2-3 port 3 path 1	F2-4 port 4 path 1	F2-5 port4 path 2	F2-6 port 2 path 2	F2-7 port 3 path 2	F2-8 port 4 path 2	F2-9 port 1 path 3	F2-10 port 2 path 3	F2-11 port 3 path 1	F2-12 port 4 path 3
6	H4-1 port 1 path 1	H4-2 port 2 path 1	H4-3 port 3 path 1	H4-4 port 4 path 1	H4-5 port 1 path 2	H4-6 port 2 path 2	H4-7 port 3 path 2	H4-8 port 4 path 2	H4-9 port 1 path 3	H4-10 port 2 path 3	H4-11 port 3 path 1	H4-12 port 4 path 3
7	F3-1 port 1 path 1	F3-2 port 2 path 1	F3-3 port 3 path 1	F3-4 port 4 path 1	F3-5 port 1 path 2	F3-6 port 2 path 2	F3-7 port 3 path 2	F3-8 port 4 path 2	F3-9 port 1 path 3	F3-10 port 2 path 3	F3-11 port 3 path 1	F3-12 port 4 path 3
8	K3-1 port 1 path 1	K3-2 port 2 path 1	K3-3 port 3 path 1	K3-4 port 4 path 1	K3-5 port 1 path 2	K3-6 port 2 path 2	K3-7 port 3 path 2	K3-8 port 4 path 2	K3-9 port 1 path 3	K3-10 port 2 path 3	K3-11 port 3 path 1	K3-12 port 4 path 3
9	N1-1 port 1 path 1	N1-2 port 2 path 1	N1-3 port 3 path 1	N1-4 port 4 path 1	N1-5 port 1 path 2	N1-6 port 2 path 2	N1-7 port 3 path 2	N1-8 port 4 path 2	N1-9 port 1 path 3	N1-10 port 2 path 3	N1-11 port 3 path 1	N1-12 port 4 path 3

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Figure 2-12. TUG-2 to TUG-3 to AU-4

Gen Register 0x000				
PrtMode Bit 7	FrmMode Bit 6	AU4Mode Bit 5	TU3Mode Bit 4	
1	1	1	0	TUG-2 to TUG-3 to AU-4

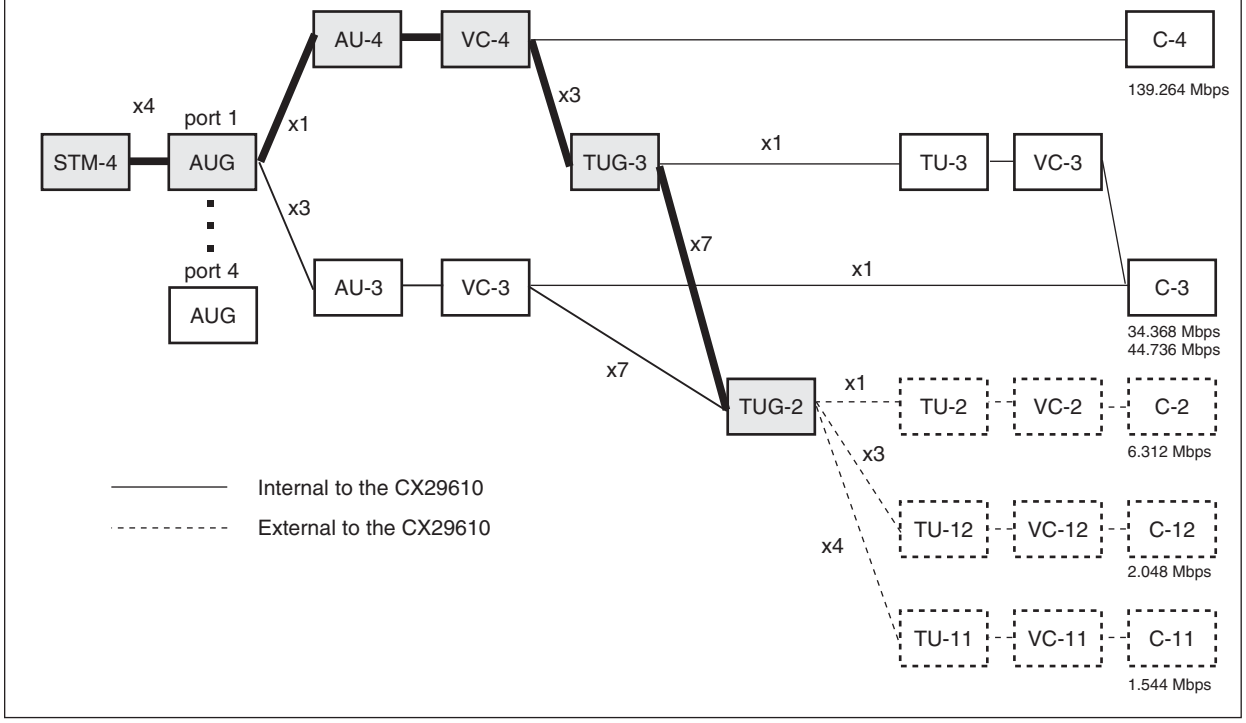

Figure 2-13. STM-4 to TUG-2

Row	Column 1											
1	A1-1 A1/A2 port 1	A1-2 A1/A2 port 1	A1-3 A1/A2 port 1	A1-4 A1/A2 port 1	A1-5 A1/A2 port 1	A1-6 A1/A2 port 1	A1-7 A1/A2 port 1	A1-8 A1/A2 port 1	A1-9 A1/A2 port 1	A1-10 A1/A2 port 1	A1-11 A1/A2 port 1	A1-12 A1/A2 port 1
2	B1 B1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D1 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H1-1 TxPntr port 1 path 1	H1-2 TxPntr port 2 path 1	H1-3 TxPntr port 3 path 1	H1-4 TxPntr port 4 path 1	H1-5 TxPntr port 1 path 2	H1-6 TxPntr port 2 path 2	H1-7 TxPntr port 3 path 2	H1-8 TxPntr port 4 path 2	H1-9 TxPntr port 1 path 3	H1-10 TxPntr port 2 path 3	H1-11 TxPntr port 3 path 3	H1-12 TxPntr port 4 path 3
5	B2-1 InsB2Err1 port 1	B2-2 InsB2Err1 port 2	B2-3 InsB2Err1 port 3	B2-4 InsB2Err1 port 4	B2-5 InsB2Err2 port 1	B2-6 InsB2Err2 port 2	B2-7 InsB2Err2 port 3	B2-8 InsB2Err2 port 4	B2-9 InsB2Err3 port 1	B2-10 InsB2Err3 port 2	B2-11 InsB2Err3 port 3	B2-12 InsB2Err3 port 4
6	D4 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D7 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D10 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	S1 S1 port 1	Z1-2 S1 port 2	Z1-3 S1 port 3	Z1-4 S1 port 4	Z1-5 S1 port 1	Z1-6 S1 port 2	Z1-7 S1 port 3	Z1-8 S1 port 4	Z1-9 S1 port 1	Z1-10 S1 port 2	Z1-11 S1 port 3	Z1-12 S1 port 4

Row	Column 2											
1	A2-1 A1/A2 port 1	A2-2 A1/A2 port 1	A2-3 A1/A2 port 1	A2-4 A1/A2 port 1	A2-5 A1/A2 port 1	A2-6 A1/A2 port 1	A2-7 A1/A2 port 1	A2-8 A1/A2 port 1	A2-9 A1/A2 port 1	A2-10 A1/A2 port 1	A2-11 A1/A2 port 1	A2-12 A1/A2 port 1
2	E1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D2 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H2-1 TxPntr port 1 path 1	H2-2 TxPntr port 2 path 1	H2-3 TxPntr port 3 path 1	H2-4 TxPntr port 4 path 1	H2-5 TxPntr port 1 path 2	H2-6 TxPntr port 2 path 2	H2-7 TxPntr port 3 path 2	H2-8 TxPntr port 4 path 2	H2-9 TxPntr port 1 path 3	H2-10 TxPntr port 2 path 3	H2-11 TxPntr port 3 path 3	H2-12 TxPntr port 4 path 3
5	K1 K1 port 1	0	0	0	0	0	0	0	0	0	0	0
6	D5 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D8 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D11 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	0	0	M1 REI-L port 1	0	0	0	0	0	0	0	0	0

Row	Column 3											
1	J0 TxSec port 1	Z0-2 Gen	Z0-3 Gen	Z0-4 Gen	Z0-5 Gen	Z0-6 Gen	Z0-7 Gen	Z0-8 Gen	Z0-9 Gen	Z0-10 Gen	Z0-11 Gen	Z0-12 Gen
2	F1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D3 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H3-1 TxPntr port 1 path 1	H3-2 TxPntr port 2 path 1	H3-3 TxPntr port 3 path 1	H3-4 TxPntr port 4 path 1	H3-5 TxPntr port 1 path 2	H3-6 TxPntr port 2 path 2	H3-7 TxPntr port 3 path 2	H3-8 TxPntr port 4 path 2	H3-9 TxPntr port 1 path 3	H3-10 TxPntr port 2 path 3	H3-11 TxPntr port 3 path 3	H3-12 TxPntr port 4 path 3
5	K2 K2 port 1	0	0	0	0	0	0	0	0	0	0	0
6	D6 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D9 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D12 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	E2 E2 port 1	0	0	0	0	0	0	0	0	0	0	0

Row	Column 4											
1	J1-1 port 1 path 1	J1-2 port 2 path 1	J1-3 port 3 path 1	J1-4 port 4 path 1	J1-5 port 1 path 2	J1-6 port 2 path 2	J1-7 port 3 path 2	J1-8 port 4 path 2	J1-9 port 1 path 3	J1-10 port 2 path 3	J1-11 port 3 path 3	J1-12 port 4 path 3
2	B3-1 port 1 path 1	B3-2 port 2 path 1	B3-3 port 3 path 1	B3-4 port 4 path 1	B3-5 port 1 path 2	B3-6 port 2 path 2	B3-7 port 3 path 2	B3-8 port 4 path 2	B3-9 port 1 path 3	B3-10 port 2 path 3	B3-11 port 3 path 3	B3-12 port 4 path 3
3	C2-1 port 1 path 1	C2-2 port 2 path 1	C2-3 port 3 path 1	C2-4 port 4 path 1	C2-5 port 1 path 2	C2-6 port 2 path 2	C2-7 port 3 path 2	C2-8 port 4 path 2	C2-9 port 1 path 3	C2-10 port 2 path 3	C2-11 port 3 path 1	C2-12 port 4 path 3
4	G1-1 port 1 path 1	G1-2 port 2 path 1	G1-3 port 3 path 1	G1-4 port 4 path 1	G1-5 port 1 path 2	G1-6 port 2 path 2	G1-7 port 3 path 2	G1-8 port 4 path 2	G1-9 port 1 path 3	G1-10 port 2 path 3	G1-11 port 3 path 1	G1-12 port 4 path 3
5	F2-1 port 1 path 1	F2-2 port 2 path 1	F2-3 port 3 path 1	F2-4 port 4 path 1	F2-5 port4 path 2	F2-6 port 2 path 2	F2-7 port 3 path 2	F2-8 port 4 path 2	F2-9 port 1 path 3	F2-10 port 2 path 3	F2-11 port 3 path 1	F2-12 port 4 path 3
6	H4-1 port 1 path 1	H4-2 port 2 path 1	H4-3 port 3 path 1	H4-4 port 4 path 1	H4-5 port 1 path 2	H4-6 port 2 path 2	H4-7 port 3 path 2	H4-8 port 4 path 2	H4-9 port 1 path 3	H4-10 port 2 path 3	H4-11 port 3 path 1	H4-12 port 4 path 3
7	F3-1 port 1 path 1	F3-2 port 2 path 1	F3-3 port 3 path 1	F3-4 port 4 path 1	F3-5 port 1 path 2	F3-6 port 2 path 2	F3-7 port 3 path 2	F3-8 port 4 path 2	F3-9 port 1 path 3	F3-10 port 2 path 3	F3-11 port 3 path 1	F3-12 port 4 path 3
8	K3-1 port 1 path 1	K3-2 port 2 path 1	K3-3 port 3 path 1	K3-4 port 4 path 1	K3-5 port 1 path 2	K3-6 port 2 path 2	K3-7 port 3 path 2	K3-8 port 4 path 2	K3-9 port 1 path 3	K3-10 port 2 path 3	K3-11 port 3 path 1	K3-12 port 4 path 3
9	N1-1 port 1 path 1	N1-2 port 2 path 1	N1-3 port 3 path 1	N1-4 port 4 path 1	N1-5 port 1 path 2	N1-6 port 2 path 2	N1-7 port 3 path 2	N1-8 port 4 path 2	N1-9 port 1 path 3	N1-10 port 2 path 3	N1-11 port 3 path 1	N1-12 port 4 path 3

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Figure 2-14. STS-4–STS-12

Gen Register 0x000				
PrtMode Bit 7	FrmMode Bit 6	AU4Mode Bit 5	TU3Mode Bit 3	
1	0	0	0	SONET OC-12

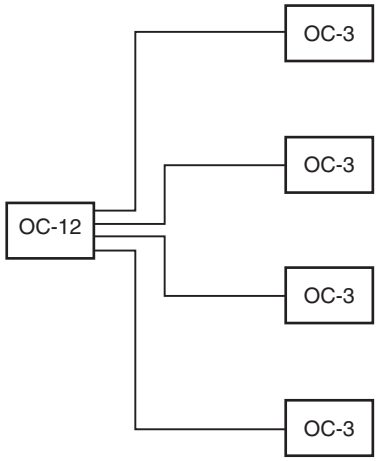

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Figure 2-15. TU-3 to TUG-3 to AU-4

Gen Register 0x000				
PrtMode Bit 7	FrmMode Bit 6	AU4Mode Bit 5	TU3Mode Bit 4	
1	1	1	1	TU-3 to TUG-3 to AU-4

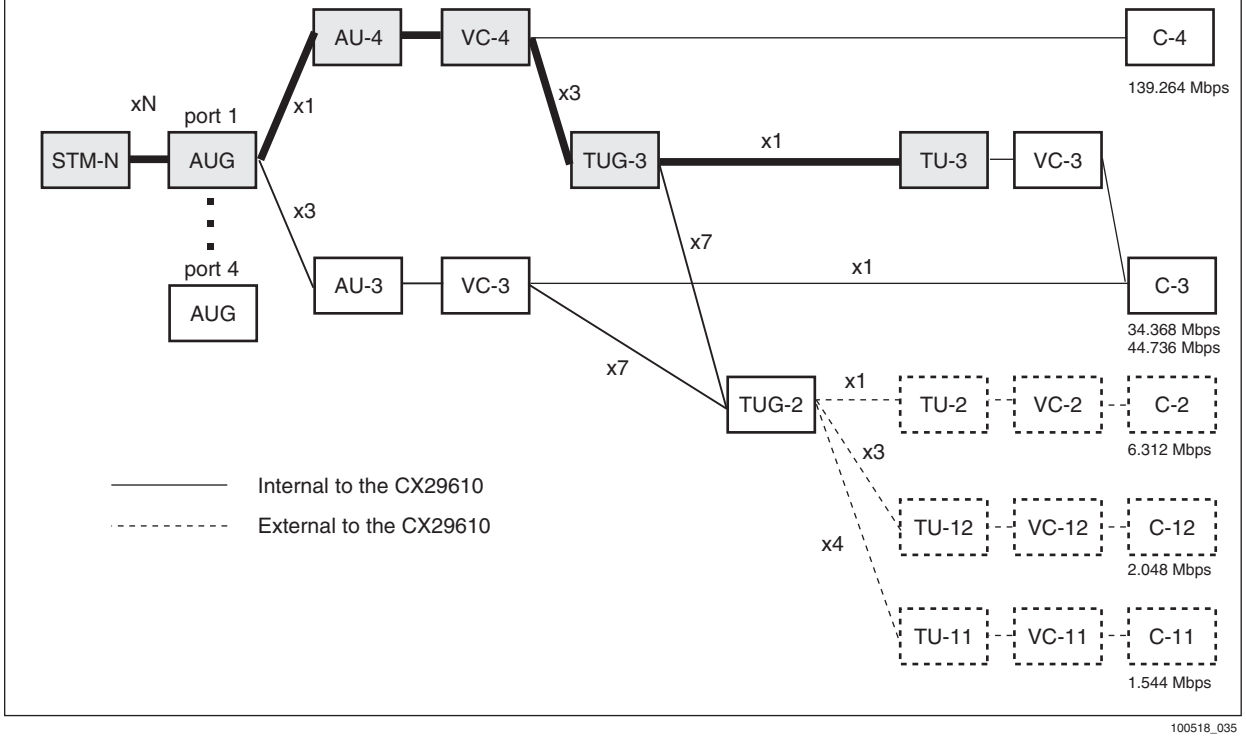

Figure 2-16. TU-3 Basic Frame (STM-4 to 4 x AUG to AU-4 to VC-4 to 3 x TU-3 Mapping)

Row	Column 1											
1	A1-1 A1/A2 port 1	A1-2 A1/A2 port 1	A1-3 A1/A2 port 1	A1-4 A1/A2 port 1	A1-5 A1/A2 port 1	A1-6 A1/A2 port 1	A1-7 A1/A2 port 1	A1-8 A1/A2 port 1	A1-9 A1/A2 port 1	A1-10 A1/A2 port 1	A1-11 A1/A2 port 1	A1-12 A1/A2 port 1
2	B1 B1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D1 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H1-1 TxPntr port 1 path 1	H1-2 TxPntr port 2 path 1	H1-3 TxPntr port 3 path 1	H1-4 TxPntr port 4 path 1	0	0	0	0	0	0	0	0
5	B2-1 InsB2Err1 port 1	B2-2 InsB2Err1 port 2	B2-3 InsB2Err1 port 3	B2-4 InsB2Err1 port 4	B2-5 InsB2Err2 port 1	B2-6 InsB2Err2 port 2	B2-7 InsB2Err2 port 3	B2-8 InsB2Err2 port 4	B2-9 InsB2Err3 port 1	B2-10 InsB2Err3 port 2	B2-11 InsB2Err3 port 3	B2-12 InsB2Err3 port 4
6	D4 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D7 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D10 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	S1 S1 port 1	0	0	0	0	0	0	0	0	0	0	0

Row	Column 2											
1	A2-1 A1/A2 port 1	A2-2 A1/A2 port 1	A2-3 A1/A2 port 1	A2-4 A1/A2 port 1	A2-5 A1/A2 port 1	A2-6 A1/A2 port 1	A2-7 A1/A2 port 1	A2-8 A1/A2 port 1	A2-9 A1/A2 port 1	A2-10 A1/A2 port 1	A2-11 A1/A2 port 1	A2-12 A1/A2 port 1
2	E1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D2 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H2-1 TxPntr port 1 path 1	H2-2 TxPntr port 2 path 1	H2-3 TxPntr port 3 path 1	H2-4 TxPntr port 4 path 1	0	0	0	0	0	0	0	0
5	K1 K1 port 1	0	0	0	0	0	0	0	0	0	0	0
6	D5 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D8 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D11 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	0	0	M1 REI-L port 1	0	0	0	0	0	0	0	0	0

Row	Column 3											
1	J0 TxSec port 1	Z0-2 Gen	Z0-3 Gen	Z0-4 Gen	Z0-5 Gen	Z0-6 Gen	Z0-7 Gen	Z0-8 Gen	Z0-9 Gen	Z0-10 Gen	Z0-11 Gen	Z0-12 Gen
2	F1 port 1	0	0	0	0	0	0	0	0	0	0	0
3	D3 SDCC port 1	0	0	0	0	0	0	0	0	0	0	0
4	H3-1 TxPntr port 1 path 1	H3-2 TxPntr port 2 path 1	H3-3 TxPntr port 3 path 1	H3-4 TxPntr port 4 path 1	H3-5 TxPntr port 1 path 1	H3-6 TxPntr port 2 path 1	H3-7 TxPntr port 3 path 1	H3-8 TxPntr port 4 path 1	H3-9 TxPntr port 1 path 1	H3-10 TxPntr port 2 path 1	H3-11 TxPntr port 3 path 1	H3-12 TxPntr port 4 path 1
5	K2 K2 port 1	0	0	0	0	0	0	0	0	0	0	0
6	D6 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
7	D9 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
8	D12 LDCC port 1	0	0	0	0	0	0	0	0	0	0	0
9	E2 E2 port 1	0	0	0	0	0	0	0	0	0	0	0

Row	Column 4											
1	J1-1 port1 path 1	J1-2 port 2 path 1	J1-3 port 3 path 1	J1-4 port 4 path 1	0	0	0	0	0	0	0	0
2	B3-1 port1 path 1	B3-2 port 2 path 1	B3-3 port 3 path 1	B3-4 port4 path 1	0	0	0	0	0	0	0	0
3	C2-1 port1 path 1	C2-2 port 2 path 1	C2-3 port 3 path 1	C2-4 port4 path 1	0	0	0	0	0	0	0	0
4	G1-1 port1 path 1	G1-2 port 2 path 1	G1-3 port 3 path 1	G1-4 port4 path 1	0	0	0	0	0	0	0	0
5	F2-1 port1 path 1	F2-2 port 2 path 1	F2-3 port 3 path 1	F2-4 port4 path 1	0	0	0	0	0	0	0	0
6	H4-1 port1 path 1	H4-2 port 2 path 1	H4-3 port 3 path 1	H4-4 port4 path 1	0	0	0	0	0	0	0	0
7	F3-1 port1 path 1	F3-2 port 2 path 1	F3-3 port 3 path 1	F3-4 port4 path 1	0	0	0	0	0	0	0	0
8	K3-1 port1 path 1	K3-2 port 2 path 1	K3-3 port 3 path 1	K3-4 port4 path 1	0	0	0	0	0	0	0	0
9	N1-1 port1 path 1	N1-2 port 2 path 1	N1-3 port 3 path 1	N1-4 port4 path 1	0	0	0	0	0	0	0	0

Row	Column 5											
1	H1-1 port1 path 2	H1-2 port2 path 2	H1-3 port3 path 2	H1-4 port4 path 2	H1-5 port1 path 3	H1-6 port2 path 3	H1-7 port3 path 3	H1-8 port4 path 3	H1-9 port1 path 4	H1-10 port2 path 4	H1-11 port3 path 4	H1-12 port4 path 4
2	H2-1 port1 path 2	H2-2 port2 path 2	H2-3 port3 path 2	H2-4 port4 path 2	H2-5 port1 path 3	H2-6 port2 path 3	H2-7 port3 path 3	H2-8 port4 path 3	H2-9 port1 path 4	H2-10 port2 path 4	H2-11 port3 path 4	H2-12 port4 path 4
3	H3-1 port1 path 2	H3-2 port2 path 2	H3-3 port3 path 2	H3-4 port4 path 2	H3-5 port1 path 3	H3-6 port2 path 3	H3-7 port3 path 3	H3-8 port4 path 3	H3-9 port1 path 4	H3-10 port2 path 4	H3-11 port3 path 4	H3-12 port4 path 4
4	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0

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STS-3/STM-1 framing delineates the frame with a block of octets, A1 and A2, with payload data in the areas between overhead blocks. In STS-3, the payload is called the Synchronous Payload Envelope (SPE). In SDH, the payload is called Virtual Container 4 (VC4). This document uses SPE to refer to the payload in either format.

The SONET Framer block recovers the A1/A2 framing location from octet-delineated data provided by the clock recovery front-end. This block also performs the pointer processing and generates row and byte counts to identify locations within the frame to downstream blocks such as the SONET overhead processor. The SONET Framer block interfaces directly with the SONET Overhead block and provides status bits to the SONET Overhead processor for presentation in status registers. The SONET Overhead block uses defined overhead bytes in an STS-3/STM-1 frame for Performance Monitoring, Fault Management, and Facility Testing. Table 2-12 lists the SONET Overhead bytes the CX29610 uses.

Table 2-12. SONET Overhead Byte Definitions and Values *(1 of 2)*

Layer	Byte	Function	Transmitted Value
Section	A1	Framing	F6h
	A2	Framing	28h
	J0	Section Trace	01h or 64-byte Section Trace message
	Z0	Section Growth	02, 03, ...
	B1	Section error monitoring	BIP-8
	E1	Section orderwire	00
	F1	Section user's data channel	00
	D1, D2, D3	Data link channel	00, 00, 00
Line	H1, H2, H3	Pointer/Concatenation indicator Path AIS	62, 0A, 00
	B2	Line error monitoring	BIP-24 or BIP-96
	K1, K2 (bits 1-5)	APS channel	00
	K2 (bits 6-8)	Line RDI Line AIS No Alarm	00
	D4-D12	Data link channel	00h
	S1	Synchronization status	00
	Z1	Future growth	00
	Z2	Future growth	00
	M1	Line REI	B2 error count
	E2	Line orderwire	00

Table 2-12. SONET Overhead Byte Definitions and Values (2 of 2)

Layer	Byte	Function	Transmitted Value
Path	J1	Path Trace	00h or 64-byte Path Trace message
	B3	Path error monitoring	BIP-8
	C2	Path signal label	01
	G1 (bits 1-4)	Path REI	B3 error count
	G1 (bits 5-7)	No Alarm Path RDI alarms	00
	F2	User communications	00
	H4	Byte not monitored	00
	F3(Z3)	Future growth	00
	K3(Z4)	Future growth	00
	N1(Z5)	Future growth	00

2.4.1 Loss of Signal

The incoming signal is monitored for an all-zeros pattern before descrambling. All-zeros patterns with a duration longer than 100 µs causes a Loss of Signal (LOS) to be reported in RXSEC bit 5. LOS is cleared when two consecutive valid framing patterns with no intervening all-zeros pattern have been received.

NOTE: A low level input on the SigDet pin causes the CX29610 to clamp the input data to all zeroes, forcing an LOS alarm.

2.4.2 Section Overhead

The Section Overhead handles the transport of the STS/STM frame across the physical medium and section-level communications. Its functions are framing and scrambling on the transmit side, and section error monitoring on the receive side. The transmit and receive functions of the Section Overhead bytes are shown in Table 2-13.

Table 2-13. Section Overhead Transmit and Receive Functions

Byte	Transmit	Receive
A1/A2	F6/28 hex, A1 inverted, or 00	Monitor out of frame state machine
B1	Calculated, error insertion option	Checked, errors counted
E1	From external pin	To external pin
F1	From TXF1 register	To RXF1 register
D1, D2, D3	00 hex or external serial access	External serial access
J0	01 hex or 64-byte trace buffer	Monitor Rx trace buffer, interrupt on change
Z0	02, 03 hex	Not checked

NOTE: Undefined overhead positions carry 00h.

2.4.2.1 A1, A2 Severely Errored Frames (SEF)

In normal operation, the A1 and A2 bytes contain F6h and 28h respectively, and are used by the CX29610 to determine the location of a frame within a data stream.

The STS-3/STM-1 framing bytes, A1 and A2, are monitored for SEF conditions. SEF is declared if errors are detected in four consecutive frames. A SEF condition causes the SEF bit in the RXSEC register to be set high and the SEFCNT register to be incremented.

On the transmit side, A1 and A2 contain F6h and 28h by default. Software can for A1 and A2 to 00 and 00 by setting the DisA1A2 bit high in the TXSEC register. To insert a single framing error on the transmit side, software set the InsFrErr bit in the ERRINS register high. This inverts the last A1 octet.

2.4.2.2 Loss of Frame

If the CX29610 detects 24 consecutive SEF, it will assert LOF bit (Loss of Frame) in the RXSEC register. LOF is deasserted after eight frames of SEF inactive.

2.4.2.3 J0, Z0

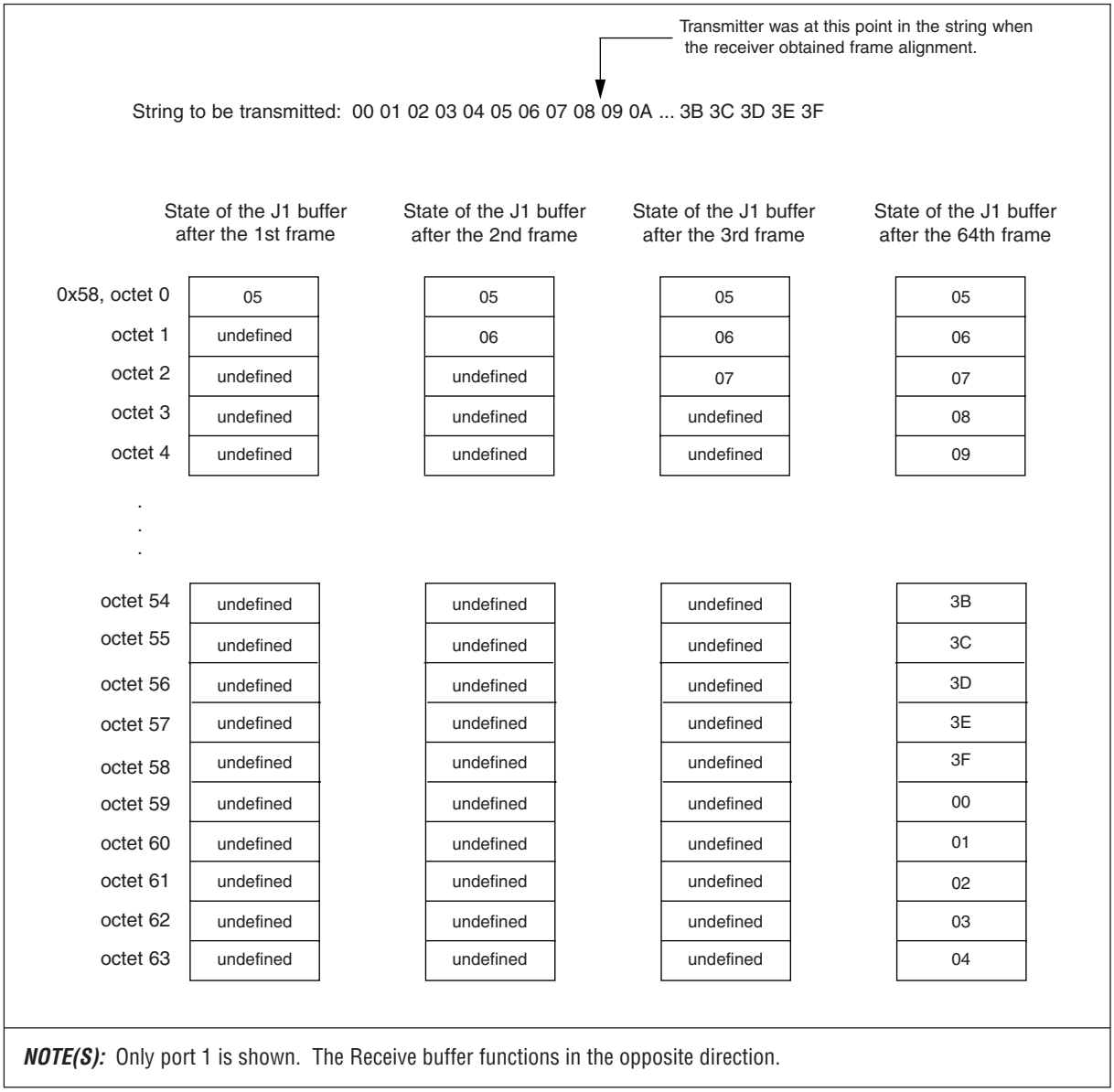
The Section Trace byte, J0, is connected to a circular 64-byte buffer that carries the Section Trace message. This enables section elements to track a continuous connection.

By default, the transmitted J0 octet contains 0x01. If the EnSecTr bit in the TXSEC register is set to 1, the device will read the next location from the TXSECBUF and transmit it in the J0 octet. Note that the contents of the TXSECBUF are undefined on power up. Figure 2-17 illustrates this.

The incoming J0 octets are written to the RXSECBUF register. This is also a circular buffer that overwrites when full. If the incoming message differs from the previous message, the SecTraceInt bit in the SECINT register will be asserted.

The Z0 octet is set to the value corresponding to its order of appearance within the frame (02, 03, 04, etc.). The received Z0 octet is not monitored.

Figure 2-17. J0 Buffer Behavior



NOTE(S): Only port 1 is shown. The Receive buffer functions in the opposite direction.

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2.4.2.4 B1

The B1 octets are allocated for section layer monitoring and contain a Bit Interleaved Parity (BIP-8) code. An error causes the B1Err bit in RXSEC to be set high and increments the B1CNT registers.

On the transmit side, the B1 octet contains the BIP-8 calculation by default. The transmit value can be forced to 00 by setting DisB1, bit 2 of the TXSEC register.

A BIP error can be introduced by setting InsB1Err, bit 6 of the ERRINS register. This performs an XOR between the B1 octet (either the valid BIP-8 value or 00, depending on DisB1) and the contents of the ERRPAT register and transmits the result.

2.4.2.5 E1

The Section Orderwire byte, E1, is allocated as an orderwire channel for voice communication. It is set to 00h as the default. If TXSEC bit 0 is set high, E1 will contain data as shifted in from the TxE1 input pin.

The E1 byte is latched from receive stream and then shifted out to the RxE1 output pin. See Section 5.1.6 for timing waveforms.

2.4.2.6 F1

The Section User's Data Channel byte, F1, is allocated for the user. It contains the value in the TXF1 register.

The F1 byte is latched in to the RXF1 register for processor access. A maskable interrupt (SECINT bit 0) is generated when the incoming F1 byte differs from the current value for 3 consecutive frames.

2.4.2.7 D1-D3

The Section Data Communication Channels (SDCC), D1–D3, provides for the transmission of management and status information. On the receive side, the D1/D2/D3 octet values are latched from the incoming data stream and output on both the SI-Bus and the RxSDCC_D pins.

The transmit values are determined as shown in Table 2-14:

Table 2-14. DCC Transmit Values

TXSEC Register		Transmit Source for D1, D2, and D3
EnTxSecDCC (bit 6)	SecDCCSrc (bit 5)	
0	0	All zeroes
0	1	All zeroes
1	0	Data input on the TxSDCC_D pin
1	1	Data from the SI-Bus

In OC-12 mode, the DCC transmit values are sourced from TxSDCC_D[0] or SI-Bus port 0.

2.4.3 Line Overhead

The Line Overhead handles the transport of path-level payloads across the physical medium. This layer of the overhead provides synchronization and multiplexing functions, including maintenance and line protection, for the Line layer. The Section Overhead must be terminated before the Line Overhead can be accessed. The transmit and receive functions of the Line Overhead are shown in Table 2-15.

Table 2-15. Line Overhead Transmit and Receive Functions

Byte	Transmit	Receive
H1/H2	620A/93FF hex pointer	Full GR.253 pointer processor
H3	00 hex	Used for negative justification
B2	Calculated, error insertion	Checked, errors counted
K1/K2	Insertable via register	Checked, interrupt on change
D4-12	00 hex or external serial access	External serial access
S1	Insertable via register	Checked, interrupt on change
Z1	From the TXZ1b/TXZ1c registers	To the RXZ1b/RXZ1c registers
Z2	From the TXZ2a/TXZ2b registers	To the RXZ2a/RXZ2b registers
M1	Line FEBE inserted	Checked, errors counted
E2	From the TxE2 pin	To the RxE2 pin

NOTE: Undefined overhead positions carry 00h.

2.4.3.1 H1 and H2

Two bytes—H1 and H2—in the STS-3/STM-1 frame are fixed on the transmit side to locate path overhead byte J1 immediately after the Z0 byte of the Section Overhead. H1 and H2 carry a fixed pointer value of 620Ah as the default. Bits 5 and 6 of the H1 byte contain the values from TXPNTR (for the respective STS-1) bits 7 and 6. This allows the SS bits to be set to any value to accommodate SDH pointers. If TXPNTR bit 5 is high, the H1/H2 bytes will each contain 33h as an invalid pointer value.

For the H1 and H2, a full pointer processor is implemented for each STS-3 to locate the STS-3/12 SPEs. Increment, decrement, and New Data Flag capability is included. The current pointer position and status is reported in the RXPNTR and PNTRSTAT registers. Positive and negative pointer justifications are counted in PJCNT and NJCNT, respectively. New Data Flags are counted in NDFCNT. The H1 and H2 bytes from the first STS-1 position can be replicated into the second and third STS-1 positions when the data is transferred downstream.

Pointer justification and New Data Flag counts are disabled during LOS, LOF, AIS-L, AIS-P, or LOP-P conditions.

2.4.3.2 H3

On the receive side, this byte is used during negative justification. Otherwise it is unused.

On the transmit side, it is always set to 00.

2.4.3.3 Loss of Pointer

The H1and H2 pointer processor reports Loss of Pointer (LOP) in RXPTH bit 7 if a valid pointer is not found for 10 consecutive frames. LOP-P is cleared when a valid pointer with NDF or a valid concatenation indicator has been received for three consecutive frames. LOP-P is terminated upon detection of AIS-P or when relaying an all-ones pointer.

AIS-P is reported in RXPTH bit 6 when the H1/H2 bytes contain an all-ones pattern for 3 consecutive frames. Path AIS is terminated when a valid H1/H2 pointer is found or when LOP-P (not AIS) is detected.

The transmit pointer generator generates a New Data Flag indication on the first valid pointer value after deassertion of either AIS-L or AIS-P.

Upstream AIS-P detection can force downstream AIS-P generation if DOWNALM is high. In TU-3 mode, AIS-P detection in the AU-4 (path 1) forces downstream AIS-P in all paths.

Set TXPTH bit 4 high to generate AIS-P, causing the H1/H2/H3 bytes and the SPE contents to be all ones.

When an LOP-P, AIS-P, or a tandem connection ISF defect is detected on the incoming signal, AIS-P is automatically generated in the downstream data path by placing all-ones content in the H1/H2/H3 bytes and in the entire STS SPE. Write bits 6, 5, or 4 (for the respective STS-1) of DOWNALM low to disable Automatic generation of AIS-P.

Set DOWNALM bit 1 high to generate AIS-P on reception of PLM-P or Uneq-P in addition to the normal generation on reception of LOP-P.

2.4.3.4 B2

The Line Parity byte, B2, monitors the line for BIP-24 and BIP-96 errors. Errors are reported in RXLIN bit 4 and counted in B2CNT. The counter length is 20 bits so that saturation does not occur during a one-second latching interval.

B2 carries the BIP-24 calculation (for STS-3 signals) or the BIP-96 calculation (for STS-12 signals) as the default. If TXLIN bit 4 is set high, all B2 bytes will contain 00h. If ERRINS bits 5, 4, or 3 are set high, the normal B2 byte value (by calculation or 00h as determined by TXLIN bit 4) in the appropriate B2 byte will be XORed with the value contained in the ERRPAT register before transmission.

B2 BIP counts are disabled during LOS, LOF, or AIS-L conditions.

2.4.3.5 APS Threshold

The Bit Error Rate (BER) is monitored from the B2 BIP error count. If the incoming error rate exceeds the thresholds programmed in the APSTHRESH register, then signal degrade or signal fail status will be reported in RXAPS bits 0 or 1, respectively.

The CX29610 can detect BERs in the range 10^{-3} to 10^{-9} by programming the exponent into a control register. The circuitry configures observation window lengths and error count thresholds directly from the programmed BER exponent. As stated in *Network node interface for the synchronous digital hierarchy (SDH)*, ITU-T Recommendation G.707 (03/96) and *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria*, Bell Communications Research, GR-253-CORE, to estimate a given BER, at least 10/BER bits need to be observed to state with 95% confidence that the estimated BER is within a factor of 2 of the actual BER. If more bits are observed, the estimate is closer for the same confidence level or the confidence in the estimate is tighter for the same estimate accuracy. This criteria is true if the BER is low or the number of bits observed is large (because the binomial error distribution can be assumed to be approximated by the Poisson distribution in this case). The observation windows are set in terms of the number of STS-3 frames. The Line BIP (B2) byte covers 19,224 bits (2403 octets) per STS-3 frame. The table below shows the parameters for each BER threshold.

Table 2-16. Bit Error Rate Analysis for STS-3

BER	Minimum Observation	Frames Observed	Actual Bits Observed	Error Threshold	Threshold Detect Time	APS Switch Requirement
10^{-3}	10^{4}	8	1.54×10^{5}	150	1 msec	8 msec
10^{-4}	10^{5}	16	3.08×10^{5}	30	2 msec	13 msec
10^{-5}	10^{6}	128	2.46×10^{6}	23	16 msec	100 msec
10^{-6}	10^{7}	1024	1.97×10^{7}	18	128 msec	1 sec
10^{-7}	10^{8}	16384	3.15×10^{8}	30	2.048 sec	10 sec
10^{-8}	10^{9}	131,072	2.52×10^{9}	24	16.384 sec	83 sec
10^{-9}	10^{10}	1,048,576	2.02×10^{10}	18	131.072 sec	667 sec
10^{-10}	10^{11}	8,388,608	1.61×10^{11}	16	1048 sec	—

2.4.3.6 BER

This column lists the thresholds that can be programmed into the control register (10^{-3} to 10^{-9}) for setting the SD or SF alarm. The 10^{-10} threshold is included in the table because the criteria for clearing an SD or SF alarm is that the BER must drop to 1/10 of the set threshold.

2.4.3.7 Minimum Observation

This column shows the number of bits that must be observed to have a 95% confidence that the estimated BER is within a factor of 2 of the actual BER.

2.4.3.8 Frames Observed

This column shows the number of frames that the circuit observes based on the BER threshold. This was picked as the power of 2 (for ease of counter implementation) that gives a number of bits observed greater than the minimum observation requirement. Substantially more bits are observed at the 10^{-3} threshold than are necessary to keep the Poisson distribution assumption intact.

2.4.3.9 Actual Bits Observed

This column is the number of frames observed multiplied by 19,224 bits/frame (amount covered by the B2 BIP). Since two to three times the number of bits that is required are observed, the accuracy of BER estimation is improved.

2.4.3.10 Error Threshold

This column is the BER multiplied by the actual number of bits observed. This is the threshold that is wired in the circuit. If this threshold is exceeded by the number of incoming B2 errors accumulated during the frames' observed period, then the set criteria for the BER alarm (SD or SF) has been reached. For clearing thresholds, the accumulated number of B2 errors during the observation period must be below the threshold to clear the SD or SF alarm. The clearing threshold is automatically set to 1/10 of the setting threshold by the set/clear circuit.

2.4.3.11 Threshold Detect Time

This column is the number of frames observed multiplied by 125 µsec per frame. This is the maximum amount of time that it takes to declare that the programmed BER is being received. If the threshold is exceeded at any time, the alarm is set immediately; not at the end of the window period. This is to meet the requirement in *Synchronous Optical Network*, ANSI T1.105 that an actual incoming BER higher than the programmed threshold is detected in the amount of time listed for the actual BER rather than in the time for the threshold BER.

2.4.3.12 APS Switch Requirement

This column lists the APS switch initiation objective from *Synchronous Optical Network*, ANSI T1.105. This is the time that an APS switch operation should commence from onset of the incoming BER. At worst, the current window is missed when the incoming errors start, thus requiring a maximum of two times the threshold detect time to set an SD or SF alarm. This still provides ample time for interrupt response and software processing to initiate the APS operation within the required time. The tightest requirement is at the 10^{-3} threshold.

Table 2-17 shows an equivalent analysis of the window and threshold requirements for the STS-12 rate that is needed for CX29610. At the STS-12 rate, the Line BIP (B2) covers 9612 octets or 76,896 bits per STS-12 frame. Since the data rate is higher, fewer frames need to be observed to estimate the BER; but the same observation windows can't be kept for the STS-3 case because the APS switch requirement is faster. The table shows that observed frames to one-quarter of the STS-3 amount and preserve the bits observed value and the error threshold value. This also decreases the detection time by four.

Table 2-17. Window and Threshold requirements for STS-12

BER	Minimum Observation	Frames Observed	Actual Bits Observed	Error Threshold	Threshold Detect Time	APS Switch Requirement
10^{-3}	10^{4}	2	1.54×10^{5}	150	0.25 msec	8 msec
10^{-4}	10^{5}	4	3.08×10^{5}	30	0.5 msec	8 msec
10^{-5}	10^{6}	32	2.46×10^{6}	23	4 msec	25 msec
10^{-6}	10^{7}	256	1.97×10^{7}	18	32 msec	250 msec
10^{-7}	10^{8}	4096	3.15×10^{8}	30	512 msec	2.5 sec
10^{-8}	10^{9}	32,768	2.52×10^{9}	24	4.096 sec	21 sec
10^{-9}	10^{10}	262,144	2.02×10^{10}	18	32.768 sec	167 sec
10^{-10}	10^{11}	2,097,152	1.61×10^{11}	16	262.144 sec	—

2.4.3.13 K1, K2

The APS Channel bytes, K1 and K2, are allocated for APS signaling between line level entities. K1/K2 carries the values from the TXK1 and TXK2 control registers. Bits 6, 7, 8 of K2 carry the AIS-L and RDI-L indications.

The K1/K2 bytes are latched into the RXK1 and RXK2 registers. A maskable interrupt (LININT bit 7) is generated when the incoming K1/K2 bytes consistently differ from the current values for 3 consecutive frames. A Protection Switching Byte Failure (PSBF) is reported in RXAPS bit 2 if a consistent APS byte can not be found.

AIS-L is reported in RXLIN bit 6 when bits 6, 7, and 8 of the K2 byte contain a 111 pattern for 5 consecutive frames. Line AIS is terminated when a non-111 pattern is detected for 5 consecutive frames.

RDI-L is reported in RXLIN bit 5 when bits 6, 7, and 8 of the K2 byte contain a 110 pattern for 5 consecutive frames. Line RDI is terminated when a non-110 pattern is detected for 5 consecutive frames.

When the transmitter has stopped transmitting AIS-L or AIS-P and is about to resume normal data transmission, the first valid pointer transmitted is accompanied by a New Data Flag for one frame.

2.4.3.14 Line RDI/AIS Detect

RDI-L can be generated either automatically or manually. Automatic generation is the default (TXLIN bit 1 high) and manual generation is set by making TXLIN bit 2 high. K2 bits 6, 7, 8 contain the AIS-L and RDI-L indications; the contents are shown in Table 2-18.

Table 2-18. K2 Indications

InsAIS-L	InsRDI-L	AutoRDI-L	K2 bits 6, 7, 8
1	X	X	111
0	1	X	110 for a minimum of 20 frames.
0	0	1	110 for a minimum of 20 frames upon detection of LOS, LOF, or AIS-L. From TXK2 bits 2, 1, 0 when no LOS, LOF, or AIS-L detected.
0	0	0	From TXK2 bits 2, 1, 0

When an LOS or LOF defect is detected on the incoming signal, an all-ones signal is placed in every byte of the frame except for the section overhead positions. This ensures that an AIS-L is automatically generated in the downstream data path. Automatic generation of AIS-L can be disabled by writing bit 7 of DOWNALM low.

AIS-L can be generated by setting TXLIN bit 3 high, causing the frame contents to be composed of valid section overhead and scrambled all-ones for the remainder of the frame.

2.4.3.15 D4-D12

The Line Data Communication Channels (DCC), D4-D12, transmit management and status information. They are set to 00h as the default. If TXLIN bit 7 is high, D4-D12 will contain data from either the TxLDCC_D input pin or from the SI-Bus interface mapped to this STS-3. In STS-12 mode, TxLDCC_D[0] or SI-Bus port 0 is the source for the line DCC.

The D4-D12 bytes are latched from receive stream and then shifted out to the RxLDCC_D output pin.

2.4.3.16 S1

The Synchronization Status byte, S1, indicates the signal clock quality and clock source. S1 carries the value from the TXS1 register.

The S1 byte is latched into the RXS1 register. A maskable interrupt (LININT bit 2) will be generated when the incoming S1 byte differs consistently from the current value for 8 consecutive frames.

The S1 Unstable interrupt and status bit is set when 2 or more of 8 consecutively received S1 bytes differ from the current stable S1 byte. It is cleared when the same S1 byte is received 8 times consecutively, whether this is the S1 byte that was received previously, or it is of a new value. The S1 Unstable status bit is reset to an active high state.

The values of the S1 byte are described in Table 2-19.

Table 2-19. S1 Byte Description

Acronym	Description	Quality Level	Lower Nibble Bits 5,6,7,8
PRS	Stratum 1 Traceable	1	0001
STU	Sync - Traceability Unknown	2	0000
ST2	Stratum 2 Traceable	3	0111
ST3	Stratum 3 Traceable	4	1010
SMC	SONET Min Clock Traceable	5	1100
ST4	Stratum 4 Traceable	5	1100
DUS	Do not use for Sync	7	1111
RES	Reserved for Network Sync Use	—	1110

2.4.3.17 Z1

The Z1 bytes are allocated for future growth, and are set to the values of the TXZ1b/TXZ1c registers.

The Z1 bytes are latched into the RXZ1b/RXZ1c registers. A maskable interrupt (LININT bit 1) is generated when the incoming Z1 bytes differ consistently from the current values for 3 consecutive frames.

2.4.3.18 Z2

The Z2 bytes are allocated for future growth, and are set to the values of the TXZ2a/TXZ2b registers.

The Z2 bytes are latched into the RXZ2a/RXZ2b registers. A maskable interrupt (LININT bit 0) is generated when the incoming Z2 bytes differ consistently from the current values for 3 consecutive frames.

2.4.3.19 M1

The Remote Error Indication (REI) byte, M1, contains the number of incoming B2 BIP errors. Errors are reported in RXLIN bit 3 and counted in RLCNT. The counter length is 20 bits so that saturation does not occur during a one-second latching interval. If TXLIN bit 0 is low, M1 will contain 00h. If ERRINS bit 2 is high, the contents of the ERRPAT register will be transmitted in the M1 byte for one frame.

REI-L counts are disabled during LOS, LOF, AIS-L, or RDI-L conditions.

2.4.3.20 E2

The Line Orderwire byte, E2, is allocated as orderwire channels for voice communication. E2 is set to 00h as the default. If TXLIN bit 5 is set high, E2 will contain data as shifted in from the TxE2 input pin.

The E2 byte is latched from the receive stream and then shifted out to the RxE2 output pin.

2.4.4 Path Overhead

Path overhead can either be generated by CX29610 or taken from the path overhead presented in the STS-1 inputs from the SI-Bus interface. Internal generation is the default, but each overhead octet can be individually selected as either internally generated or sourced from the SI-Bus interface by the bits in the PTHINS register.

The Path Overhead checks for end-to-end communication integrity. The Section and Line Overhead must be terminated before the Path Overhead can be accessed. Table 2-20 lists the transmit and receive functions of the Path Overhead.

Table 2-20. Path Overhead Transmit and Receive Functions

Byte	Transmit	Receive
J1	00 hex or 64-byte trace buffer	Monitor Rx trace buffer, interrupt on change
B3	Calculated, error insertion	Checked, errors counted
C2	From the TXC2 register	Compared to PROVC2
G1	Path FEBE, RDI inserted	Checked, errors counted, status

2.4.4.1 J1

The Path Trace byte, J1, is a circular 64-byte buffer, carrying the Path Trace message, so that a receiving Path Terminating Equipment (PTE) can verify continued connection to the transmitting PTE. This buffer overwrites when full. This byte is set to 00h as the default. If TXPTH bit 7 is set high, then the J1 byte will contain a 64-byte circular message extracted from the TXPTHBUF RAM space. If PTHINSL bit 7 is high, then J1 will contain the contents as received on the SI-Bus interface regardless of the settings of other control bits affecting J1.

The J1 byte is captured into a 64-byte circular buffer that is readable from the microprocessor interface. A maskable interrupt (PTHINT bit 0) is generated when the incoming message differs from the previous buffer contents.

2.4.4.2 B3

The Path BIP-8 byte, B3, is allocated for path error monitoring. Errors are reported in RXPTH bit 4 and counted in B3CNT. The counter length is 16 bits so that saturation does not occur during a one-second latching interval. B3 carries the BIP-8 calculation for path error monitoring as the default. If TXPTH bit 6 is set high, the B3 byte will contain 00h. If PTHINSH bit 3 is set high, the normal B3 byte value (by calculation or 00h as determined by TXPTH bit 6) will be XORed with the value contained in the ERRPAT register before transmission. If PTHINSL bit 6 is high, then B3 will contain the contents as received on the SI-Bus interface regardless of the settings of other control bits affecting B3 (except error insertion will work on any B3 source).

B3 BIP counts are disabled during LOS, LOF, AIS-L, AIS-P, LOP-P, or Uneq-P conditions.

2.4.4.3 C2

The Path Signal label byte, C2, identifies the type of payload being received. C2 carries the value from the SI-Bus as the default. If PTHINSL bit 5 is high, then C2 will contain the contents as received on the SI-Bus interface.

The C2 byte is latched into the RXC2 register after consistent values are received for 5 consecutive frames. The received value is compared to the provisioned value programmed into the PROVC2 register to monitor for PLM-P and Uneq-P alarms. PLM-P and Uneq-P are reported in RXPTH bits 2 and 1, respectively.

Payload Label Mismatch (PLM-P) is reported in RXPTH bit 2 when the received C2 value indicates a different payload specific functionality than that provisioned in the PROVC2 register. PLM-P is terminated upon detection of Uneq-P.

Path Unequipped (Uneq-P) is reported in RXPTH bit 1 when the received C2 value indicates unequipped (00h) and the PROVC2 register contains an equipped functionality code.

2.4.4.4 G1

The Path Status byte, G1, is used to convey path terminating status and performance monitoring information back to an originating STS PTE. Errors are reported in RXPTH bit 3 and counted in RPCNT. The counter length is 16 bits so that saturation does not occur during a one-second latching interval. G1 is also monitored for RDI-P errors. RDI-P errors are reported in RXPTH bit 5. G1 contains the REI-P and RDI-P values in response to incoming B3 BIP errors and path alarms as the default. If TXPTH bit 5 is low, G1 bits 1–4 will contain 0000. If PTHINSH bit 2 is written high, the contents of the ERRPAT bits 7–4 will be transmitted in G1 bits 1–4 for one frame. If PTHINSL bit 4 is high, then G1 will contain the contents as received on the SI-Bus interface regardless of the settings of other control bits affecting G1.

Path RDI (RDI-P) is reported in RXPTH bit 5 according to the following table. The RDI bits from the G1 byte are latched into the RXRDI register when a consistent new value is received for 10 consecutive frames.

Table 2-21. G1 bit Interpretation

G1 bits 5, 6, 7	Interpretation
000, 011, 001	No RDI-P defect
100, 111	One-bit RDI-P defect
010	ERDI-P payload defect
101	ERDI-P server defect
110	ERDI-P connectivity defect

RDI-P can be generated either automatically or manually. Automatic generation is the default (TXPTH bit 0 high). G1 bits 5, 6, 7 contain the RDI-P indications; the contents are shown in the table below in order of generation priority.

REI-P counts are disabled during LOS, LOF, AIS-L, AIS-P, LOP-P, Uneq-P, or RDI-P (101 or 110).

Table 2-22. G1 bit Indications

AutoRDI-P	Trigger	G1 bits 5, 6, 7
1	LOS, LOF, AIS-L, AIS-P, LOP-P	101 for a minimum of 20 frames.
1	UNEQ-P	110 for a minimum of 20 frames.
1	PLM-P	010 for a minimum of 20 frames.
1	No defects	001 for a minimum of 20 frames.

2.4.4.5 F2

The F2 byte is allocated for user communication purposes between STS Path terminating NEs. F2 is set to the value contained in the TXF2 register. If PTHINSL bit 3 is high, then F2 will contain the contents as received on the SI-Bus interface.

The F2 byte is latched in to the RXF2 register for processor access. A maskable interrupt (PNTRINT bit 3) is generated when the incoming F2 byte differs consistently from the current value for 3 consecutive frames.

2.4.4.6 H4

The H4 byte is allocated for use as a mapping-specific indicator byte. H4 is set to 00h as the default. If PTHINSL bit 2 is high, then H4 will contain the contents as received on the SI-Bus interface.

The H4 byte from the first STS-1 position can be replicated into the second and third STS-1 positions when the data is transferred downstream.

2.4.4.7 F3 (Z3)

The F3 (Z3) byte is allocated for future growth, and is set to the value of the TXF3 register. If PTHINSL bit 1 is high, then F3 will contain the contents as received on the SI-Bus interface.

The F3 (Z3) byte is latched in to the RXF3 register for processor access. A maskable interrupt (PNTRINT bit 2) is generated when the incoming F3 byte differs consistently from the current value for 3 consecutive frames.

2.4.4.8 K3 (Z4)

The K3 (Z4) byte is allocated for future growth, and is set to the value of the TXK3 register. If PTHINSL bit 0 is high, then K3 will contain the contents as received on the SI-Bus interface.

The K3 (Z4) byte is latched in to the RXK3 register for processor access. A maskable interrupt (PNTRINT bit 1) is generated when the incoming K3 byte differs consistently from the current value for 3 consecutive frames.

2.4.4.9 N1 (Z5)

The N1 (Z5) byte is allocated for Tandem Connection Maintenance and the Path Data Channel, and is set to the value of the TXN1 register. If PTHINSH bit 6 is high, then N1 bits 1–4 will contain the incoming B3 error count value from the receiver (or signal fail indication) for use with tandem connections. If PTHINSH bit 7 is high, then N1 bits 1–4 will contain the contents as received on the SI-Bus interface. If bits 7 and 6 are high, then N1 bits 1–4 will contain 1111. If PTHINSH bit 5 is high, then N1 bits 5–8 will contain the contents as received on the SI-Bus interface.

The N1(Z5) byte is latched in to the RXN1 register each frame for processor access. Bits 1–4 are also monitored for ISF status and tandem connection error counts. A maskable interrupt (PNTRINT bit 0) is generated when ISF (IEC=1111) is detected or when a tandem error count is detected.

2.4.5 Custom Extensions

Several of the control register bits in the CX29610 register map are for specific applications when CX29610 is used with the Broadband Access Mapper (BAM) device. These bits may be of use in other applications but may also generate operation that does not conform to SONET standards. This is not a problem when used with BAM, since BAM is a termination device and thus the non-standard data contained is only visible between CX29610 and BAM. The BAM-specific bits are listed below:

- DOWNALM bit 2—copies the H1/H2 pointer bytes from the first STS-1 position to the second and third STS-1 positions. This is used to provide the pointer information to independent BAM slices that observe data in the second and third STS-1 positions since they do not have visibility of the first position pointer. An example of this is the VC-4 to TUG-3 mapping for SDH. The H4 byte is also copied in the same manner when this bit is set. This feature is disabled by default.
- DOWNALM bit 1—allows generation of AIS-P downstream upon reception of PLM-P or Uneq-P. Usually downstream AIS-P is generated only upon reception of LOP-P. BAM performs path conditioning and generates upstream alarms for PLM-P and Uneq-P the same as when it receives AIS-P or LOP-P. Generating this downstream alarm in CX29610 removes the requirement of separate notification to BAM of reception of PLM-P or Uneq-P since BAM has the capability to detect AIS-P. This feature is disabled by default.

2.4.6 SONET Frame Scrambler

Each SONET Network Element (NE) is required to have the capability to derive the clock timing from the incoming line interface signal. All transmitted line interface signals are timed from this clock. Therefore, it is important to maintain the ones density in the data stream to ensure enough data transitions for robust clock recovery. The technique commonly used with modems, called scrambling and descrambling, is used in SONET to make the data appear to be more random.

This process uses a frame synchronous scrambler with a sequence length of 127, operating at the line rate. The generating polynomial is $x^7 + x^6 + 1$. The scrambler is reset to 1111111 on the most-significant bit of the J1 byte. This bit and all the subsequent bits to be scrambled are added, modulo 2, to the output from the x^7 position of the scrambler. Everything but the first row of the section overhead is scrambled.

Set bit 7 in register TXSEC to disable transmitter frame scrambling. Set bit 1 in register TXSEC to send all zeros after scrambling.

Set bit 3 in register DOWNALM to disable receiver frame scrambling.

2.5 Microprocessor Interface

2.5.1 Interface Modes

The CX29610 microprocessor interface can operate in one of two modes. The Mindspeed EBUS mode is normally selected when the device is used in applications with the CX29503 and the CX28500/CX28560. The EBUS mode has a multiplexed address and data bus, and seperate read and write control signals. See Table 1-4 for the interface signal descriptions. Read and write cycle timing diagrams are shown in Figures 5-5 and 5-6.

The MPC860 interface mode allows easy glueless connectivity to a Motorola MPC860 style interface. This interface has seperate address and data lines with a single read/write signal. Table 1-4 describes the interface signal descriptions. Figures 5-5 and 5-6 illustrate the read and write cycle timing.

2.5.2 Status and Control

Several registers provide status and control information to the microprocessor. Status information includes interrupts, counters, and generic functional status. Control information includes configuration and real-time control, according to the specific function of each control register. There are two types of status input: live and latched. Live status provides the current status of the device. Latched status is used for rapidly changing states in order to capture information until it can be read.

The CX29610 contains general purpose status and control functions, such as a master reset, output status, and device part number and revision. The software-controlled master reset, GEN register (0x00) bit 0, restarts all device functions and sets the control and status registers to their default values. The OUTSTAT register (0x02) provides a means for controlling external devices via the OutStat pins. It is enabled by setting the StatPinMode (bit 2) of the GEN register (0x00). The VER register (0x03) uniquely identifies the device and revision level.

2.5.3 Counters

The CX29610 counters are used to record events within the device. There are two types of events: error events, such as Section BIP errors, and transmission events.

Counters which are composed of more than one register must be accessed by reading the least significant byte first. This guarantees that the value contained in each component register accurately reflects the composite counter value at the time the least significant byte was read. This is important because the counter may be updated while the component registers are being read.

Each counter is large enough to accommodate the maximum number of events that may occur within a one-second interval. The counters are cleared after being read. Therefore, if the counters are read every second, the application receives an accurate recording of all event occurrences.

2.5.4 One-second Latching

Mindspeed's implementation of one-second latching assures the integrity of the statistics being gathered by the network management software. Internal statistics counters can be latched at one-second intervals, which are synchronized to the OneSecIn pin. Therefore, the data read from the statistic counters represents the same "one second" of real-time data, independent of network management software timing.

The CX29610 implements one-second latching for both status signals and counter values. When EnStatLat (bit 5) in the GEN register is written to a logic 1, a read from any of the status registers will return the state of the device at the time of the previous OneSecIn pin assertion. When the EnCntrLat bit (4) in the GEN register is written to a logic 1, a read from any of the counters returns the state of the device at the time of the previous OneSecIn pin assertion. Every second, the counter is read, moved to the latch, and cleared.

The OneSecIn pin is intended to be asserted at one-second intervals. This can be achieved by connecting the OneSecIn pin to the OneSecOut pin. The OneSecOut signal is derived from the 8kHzIn pin. This signal is asserted for one 8kHzIn clock period, every 8,000 8kHzIn periods. If 8kHzIn is being driven by an 8 kHz clock, the OneSecOut signal is asserted every second.

NOTE: When latching is disabled and a counter is wider than one byte, the LSB should be read first, which will retain the values of the other bytes for a subsequent read.

2.5.5 Interrupts

The status registers and corresponding interrupt/enable registers for the receiver are listed in Table 2-23.

Table 2-23. Receiver Registers

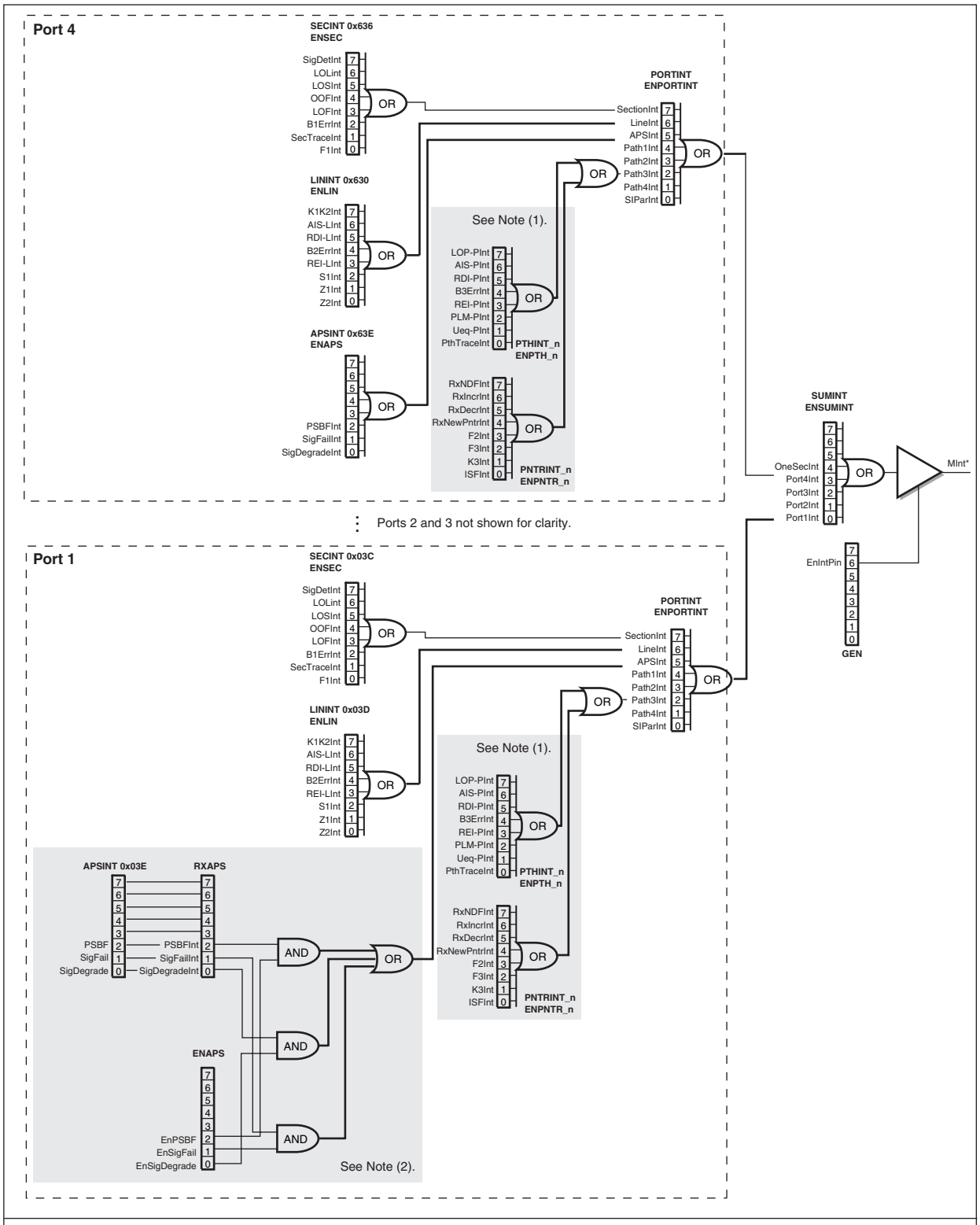
Status Register	Interrupt Indication Register	Interrupt Enable Register
—	SUMINT	ENSUMINT
—	PORTINT	ENPORTINT
RXSEC	SECINT	ENSEC
RXLIN	LININT	ENLIN
RXAPS	APSINT	ENAPS
RXPTH_n	PTHINT_n	ENPTH_n
PNTRSTAT_n	PNTRINT_n	ENPNTR_n

Each status register bit has a corresponding interrupt bit in the interrupt register and an enable bit in the enable register. The status register shows the current condition of the circuit. Some of the bits are latched to show that an event occurred since the register was last read. Other bits show the current condition of an alarm or state. The differences are noted in the register descriptions.

All of the interrupt register bits are latched indications that a transition occurred on the corresponding status bit. Interrupt indications are cleared when the indication register is read. Each interrupt indication bit has an enable bit in the enable register. The enable bit must be set high to allow that interrupt to appear on the MInt* output. The state of the enable control does not affect operation of the indication or status bits; only whether those indications are allowed to appear on the output pin.

The output enable for the MInt* pin is found in GEN bit 4. In addition to the individual status/interrupt bits, a summary interrupt register for each port indicates the source register of the interrupt in that port and a top-level summary interrupt register indicates whether the interrupt was from a port or from the one-second latching circuit. Each of these indications has a corresponding enable. Figure 2-18 illustrates the interrupt hierarchy.

Figure 2-18. Interrupt Hierarchy



NOTE(S):

(1) For clarity, only one Path Pointer is shown. See the Data Sheet for addresses.

(2) Schematic relationship between the status registers, enable registers, and interrupt registers. For clarity, only one is shown.

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The CX29610's interrupt indications can be classified as either single-event or dual-event. A single-event interrupt is triggered by a status assertion. A dual-event interrupt is triggered by either a status assertion or deassertion. Both types of interrupts are further described in the following examples.

Single-event interrupt	When a signal-fail event occurs, an interrupt is generated on the SigFail bit in the RXAPS register. This bit is cleared when read.
Dual-event interrupt	When an LOS occurs, the SigDetInt bit in the SECINT register is set to 1. This bit is cleared when the register is read. Once the signal is recovered, the SigDetInt bit is set to 1 again, generating another interrupt.

All interrupt bits have a corresponding enable bit. This allows software to disable or mask interrupts as required.

2.5.5.1 Interrupt Suppression During Error Conditions

A single, low level error condition can generate numerous false interrupts. For example, a LOS condition results in almost all other interrupts being set, even though only the LOS condition needs to be addressed by software. To help simplify the software interrupt routines, the CX29610 automatically supresses higher-level interrupt when the errors shown in Table 2-24 occur.

Table 2-24. Interrupt Suppression during Error Conditions

Register	Interrupts	Suppressed during:							
		LOS	LOF	AIS-L	AIS-P	LOP-P	RDI-L	Uneq-P	RDI-P
SECINT	B1Err	3							
	SecTrace	3							
LININT	K1K2	3	3	3			3		
	RDI-L	3	3	3					
	B2Err	3	3	3					
	REI-L	3	3	3			3		
	S1	3	3	3					
	Z1	3	3	3					
	Z2	3	3	3					
APSINT	PSBF	3	3	3					
	SigFail	3	3	3					
	SigDegrade	3	3	3					
PTHINT_n	RDI-P	3	3	3	3	3			
	B3Err	3	3	3	3	3		3	
	REI-P	3	3	3	3	3		3	3
	PLM-P	3	3	3	3	3			
	Uneq-P	3	3	3	3	3			
	PthTrace	3	3	3	3	3			
PNTRINT_n	RxNDF	3	3	3	3	3			
	RxIncr	3	3	3	3	3			
	RxDecr	3	3	3	3	3			
	RxNewPntr	3	3	3	3	3			
	F2	3	3	3	3	3			
	F3	3	3	3	3	3			
	K3	3	3	3	3	3			

2.6 SI-Bus Interface

This section describes the system interface the CX29610 uses. This interface can transfer payload data derived from either SONET or SDH data streams. The SONET terminology for various rates and formats is used with the corresponding SDH terminology following in parenthesis.

2.6.1 Description

The SI-Bus transfers three complete, interleaved STS-1s with three separate start of frame syncs.

The SI-Bus interface is capable of full-duplex, bi-directional transmission of SONET(SDH) data between a CX29610 device and several slave devices. By definition, receive data flows from the CX29610 to the slave and transmit data flows from the slave to the CX29610. Clocks and alignment controls flow from the CX29610 to the slave in both the transmit and receive directions.

It operates at the nominal octet data rate of 19.44 MHz and has a continuous clock. Transmit and Receive 51.84 MHz clocks are generated for slave devices thtat require STS-1 bit rate clocks.

2.6.2 Signals

Tables 2-25 and 2-26 summarize the signals required to implement the SI-Bus interface. There are a total of 26 signals required to implement each SI-Bus interface. The CX29610 has four independent SI-Busses.

Table 2-25. Signal Definition for Transmit Interface

Signal	Description
TxHSClk	The clock signal is generated by the CX29610 and supplied to the slave. Nominal rate is 51.84 MHz.
TxClk	The clock signal is generated by the CX29610 and supplied to the slave. Nominal rate is 19.44 MHz.
TxData[7:0]	The 8-bit data path for transmit data from the slave device to the CX29610 device. TxData[7] is the MSB, TxData[0] is the LSB. Data is provided in response to the TxClk signal.
TxStart	The start signal, which is generated by the CX29610, indicates the start of frame for the STS-1 frame.
TxPrty	Data path parity. The TxPrty parity bit serves as the odd parity bit calculated over TxData[7:0]. TxPrty ≈ (TxData[7] ^ TxData[6] ^ TxData[5] ^ TxData[4] ^ TxData[3] ^ TxData[2] ^ TxData[1] ^ TxData[0]) where ^ is the XOR operator.

Table 2-26. Signal Definition for Receive Interface

Signal	Description
RxHSClk	The clock signal is generated by the CX29610 and supplied to the slave. Nominal rate is 51.84 MHz. This clock is derived from the incoming line timing for the OC3 data stream.
RxClk	The clock signal is generated by the CX29610 and supplied to the slave. Nominal rate is 19.44 MHz. This clock is derived from the incoming line timing for the OC3 data stream.
RxData[7:0]	The 8-bit data path for receive data from the CX29610 device to the slave device. RxData[7] is the MSB, RxData[0] is the LSB. Data is provided synchronously with the RxClk signal.
RxStart[3:1]	The start signals indicate the start of frame for STS-1 numbers 3, 2, and 1, respectively.
RxPrty	Data path parity. The RxPrty parity bit serves as the odd parity bit calculated over RxData[7:0]. RxPrty ≈ (RxData[7] ^ RxData[6] ^ RxData[5] ^ RxData[4] ^ RxData[3] ^ RxData[2] ^ RxData[1] ^ RxData[0]) where ^ is the XOR operator.

2.6.3 Operation

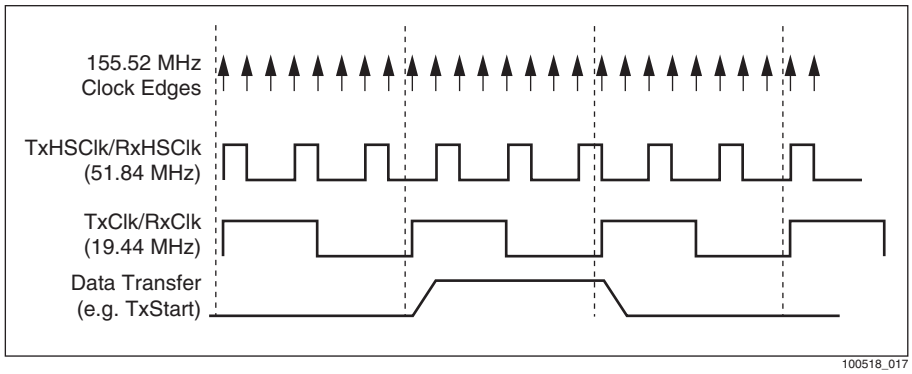
The following sections describe the operation of the transmit and receive interfaces, which can connect three slave devices, capable of processing multiple (or single) STS-1 data streams, to a single CX29610.

NOTE: Each port (1–4) of the CX29610 is an independent master for its own SI-Bus.

2.6.3.1 Clock Operation

The octet transfer rate across the SI-Bus interface is 19.44 MHz in each direction synchronous with TxClk and RxClk. Also, the TxHSClk and RxHSClk provided on the interface are 51.84 MHz, which eliminates the need for clock multiplication in the slave device. The high speed clocks are not used by the interface for data transfer/sampling but are used in the slave devices for deriving sub-STS-1 payload clocks. Figure 2-19 illustrates the relationship of the clock and data transfers relative to the 155.52 MHz line rate clock for the STS-3. The TxHSClk and RxHSClk signals present on the SI-Bus interface are 51.84 MHz clocks derived from the 155.52 MHz line clocks as a divide-by-three. The octet clocks TxClk and RxClk are 19.44 MHz clocks derived from the 155.52 MHz line clocks as a divide-by-eight.

Figure 2-19. SI-Bus Clock Relationships



2.6.3.2 Basic Operation

Data transfer can be between three slave devices (or a multi-channel slave device) and the CX29610 and involves the transfer of three interleaved STS-1 frames across the data bus. The Start signals indicate the beginning of the STS-1 frame (A1 octet) and are one octet clock in duration. Figure 2-20 illustrates an STS-1 frame.

Figure 2-20. Unit of Transfer (3 Interleaved STS-1 Frames)

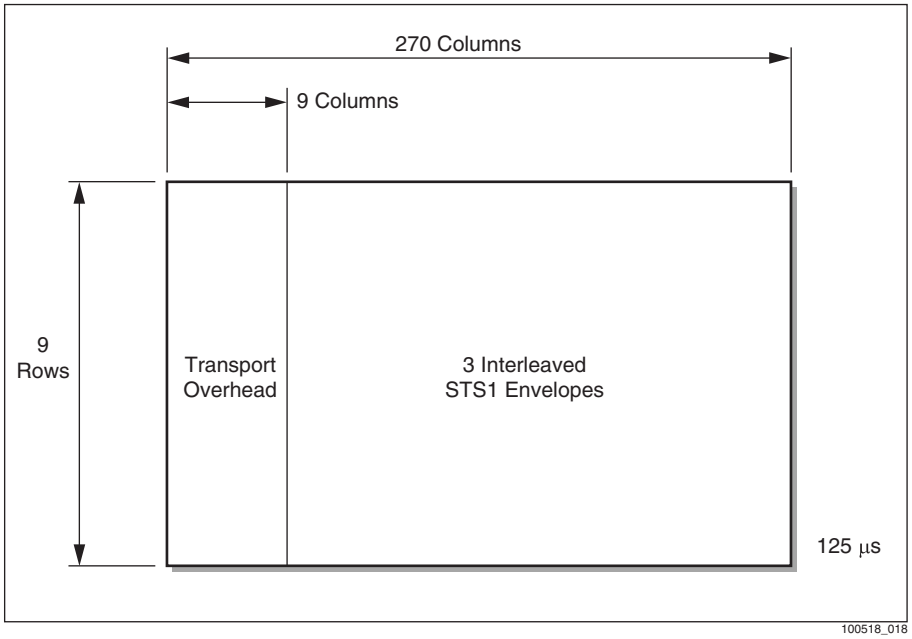
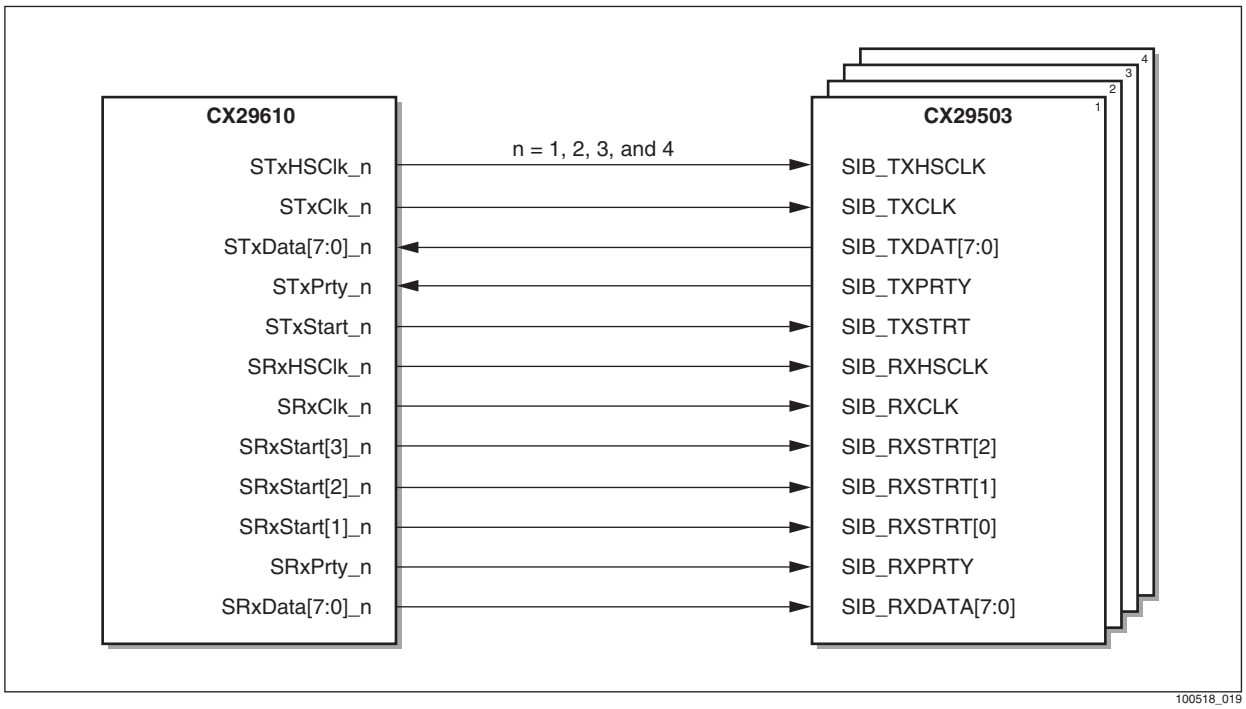


Figure 2-21 illustrates the interconnection between the CX29610 and four CX29503 devices. The "_n" suffixes on the CX29610 signal names range from 1–4 and indicate the four SI-Bus interfaces on the CX29610. The set of signals for each SI-Bus interface must connect to the same CX29503 device. For example, STxHSClk_1, STxClk_1, etc. must connect to the same CX29503 device.

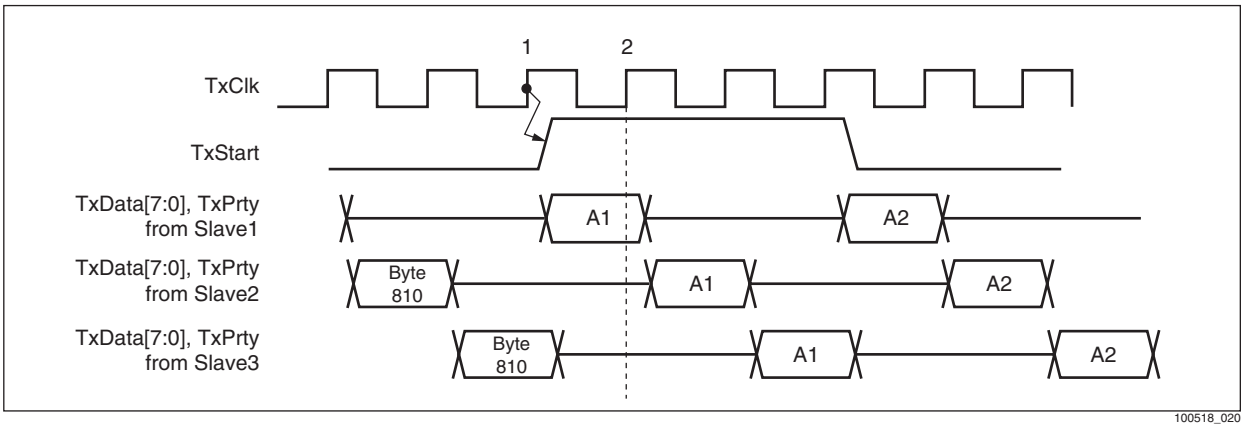
Figure 2-21. SI-Bus Mode Interface to CN29503



Transmit Interface

The CX29610 device generates TxHSClk, TxClk, and TxStart signals to control the slave devices. The slave devices respond with TxData and TxPrty in their appropriate time slots. The CX29610 device samples TxData and TxPrty on the rising edge of TxClk and provides TxStart synchronously with the rising edge of TxClk. Figure 2-22 illustrates these data relationships. The CX29610 device expects to sample the A1 octet position (first octet of the STS frame) on the clock edge (2) after the TxStart signal is provided (edge 1). The CX29610 device samples data on every TxClk edge, with 2430 clock edges defining the 3 interleaved STS-1 frames. Each slave device responds on every third TxClk edge and is three-stated during the intervening two TxClk cycles. Each slave has a predetermined time slot in which it is expected to respond relative to the rising edge of the TxStart signal. The CX29610 device generates the correct Transport Overhead and ignores data from the slave during overhead timeslots. Content of the Path Overhead positions is dependent on the CX29610/slave implementations. The TxPrty signal is not shown but should follow the same relationship as TxData. A multi-channel capable slave does not have to three-state the data bus between channels and can drive interleaved data continuously onto the bus.

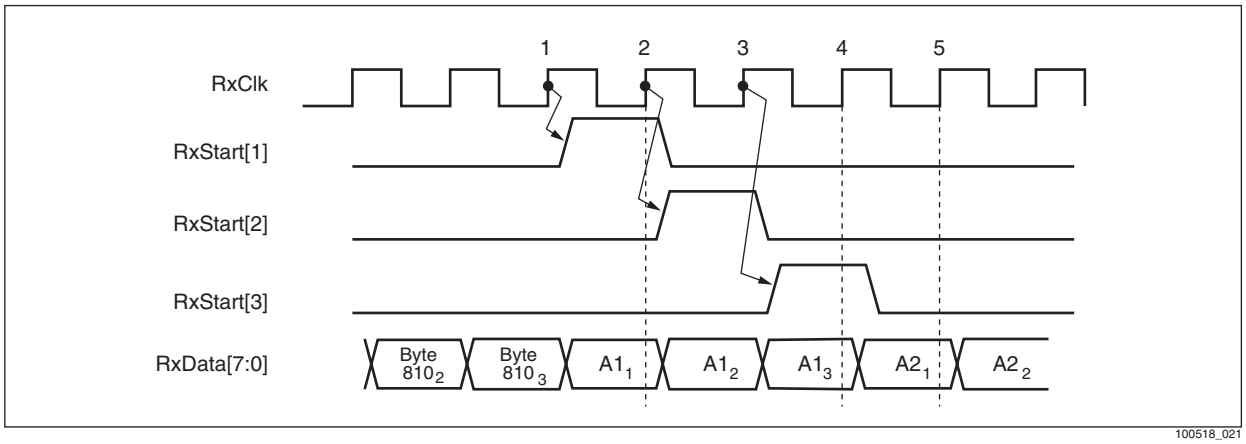
Figure 2-22. Mode Transmit Signal Relationship



Receive Interface

The CX29610 device generates RxHSClk, RxClk, RxStart[3:1], and RxData signals to control the slave devices. The RxStart[3:1] and RxData signals are provided synchronously with the rising edge of RxClk. Figure 2-23 illustrates these data relationships. Each RxStart signal indicates the position of the A1 octet in the STS-1 frame that corresponds to its number. RxStart[1] indicates the A1 position in the first STS-1 frame, RxStart[2] indicates the A1 position in the second STS-1 frame, and RxStart[3] indicates the A1 position in the third STS-1 frame. Each slave device samples data on every third clock relative to the rising edge of its RxStart signal. One RxClk edge is present for each of the 2430 octets in the 3 interleaved STS-1 frames. The RxPrty signal is not shown but has the same relationship as RxData. Slaves should ignore data during the overhead timeslots.

Figure 2-23. Mode Receive Signal Relationship

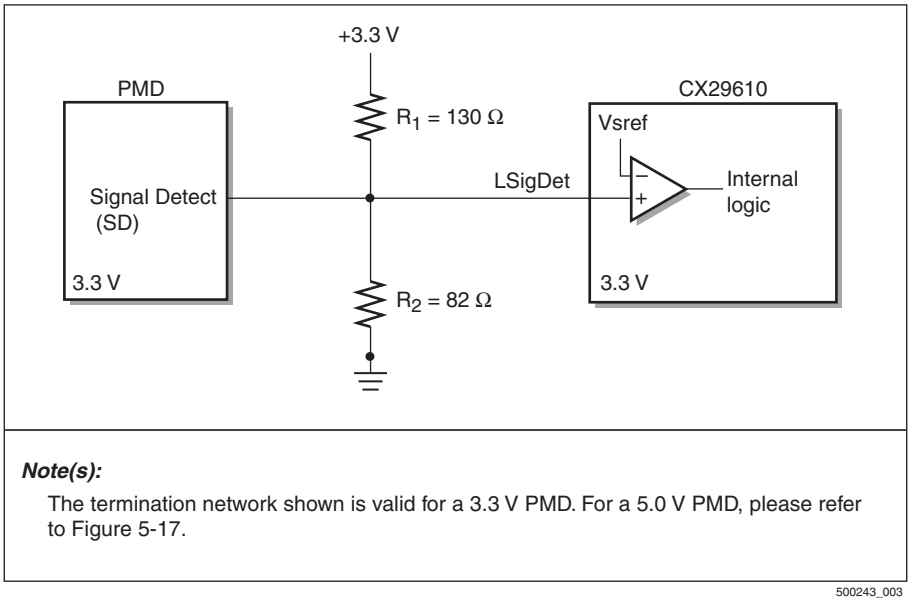


2.7 TTL/PECL Interface

The LSigDet pin on the CX29610 line interface can be driven by TTL or PECL drivers. The CX29610 can be connected directly to a TTL interface without external components. When using a single-ended PECL interface, the input signal must be centered around V_{sref} as shown in Table 5-18.

A typical LIU/PECL interface is shown in Figure 2-24. This block diagram assumes a 3.3 V LIU. Resistors R1 and R2 are used set the low-level input voltage, V_{il}, going to the CX29610. The values shown set V_{il} at 2.019 V, which is well below the minimum required by the CX29610. If an external driver/buffer is used, it must provide a current return path to V_{DD} to reduce noise issues.

Figure 2-24. Single-ended PECL Diagram



Note(s):

The termination network shown is valid for a 3.3 V PMD. For a 5.0 V PMD, please refer to Figure 5-17.

2.7.1 PECL Bias Network

The CX29610 can utilize a new PECL bias network as shown in Figure 2-25. This simplifies board layout by eliminating the pull-up resistors used in previous PECL interfaces. The CX29610 is backward compatible with legacy layouts as shown in Appendix A.

All PECL traces must be treated as transmission lines. Therefore, standard high-speed practices must be followed:

- Keep traces as short as reasonable.
- Do not allow traces to cross discontinuities in the ground/power planes.
- Use separate Power and Ground planes.
- Terminate all inputs and outputs as described above.
- Place the terminating resistors as close to the destination IC as possible.
- Do not route signal traces through the board through vias.
- Check that each IC has two high-quality RF bypass capacitors that are at least an order of magnitude apart; e.g., 200 pF and 0.1 µF.
- Avoid 90 degree turns in trace routing.
- Ensure that the trace width results in a line impedance that matches the input impedance of the load. Trace width can be calculated from the following equation:

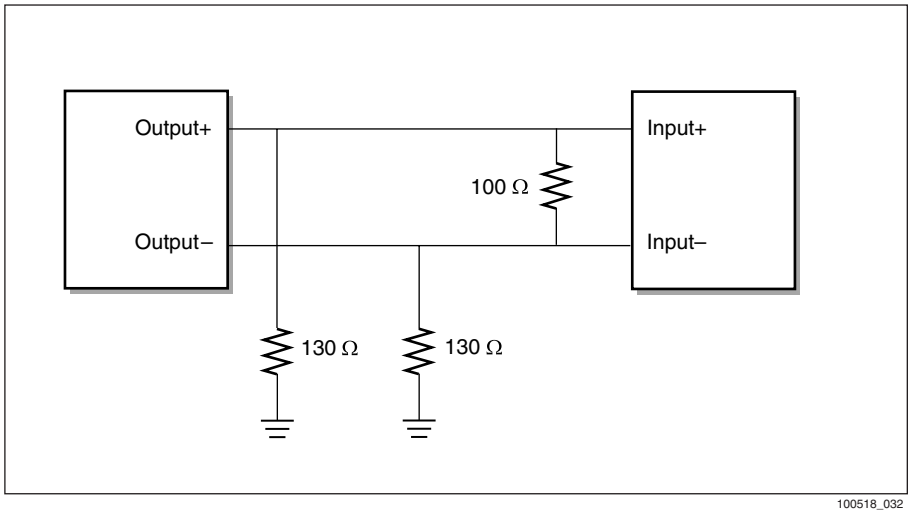
$$w = \left(7.745 \times h \times e^{-\left[\frac{\sqrt{e_r + 1.41} \times Z_0}{87}\right]}\right) - \frac{t}{0.8}$$

where:

w = trace width
Z_0 = characteristic line impedance
h = board thickness (not including copper layers)
t = thickness of copper layers
e_r = relative dielectric constant of the board

Using the generic values Z_0 = 50 Ω, h = 0.060, t = 0.0015 and e_r = 4.8 results in a width (w) of 0.11 inches.

Figure 2-25. PECL Bias Network



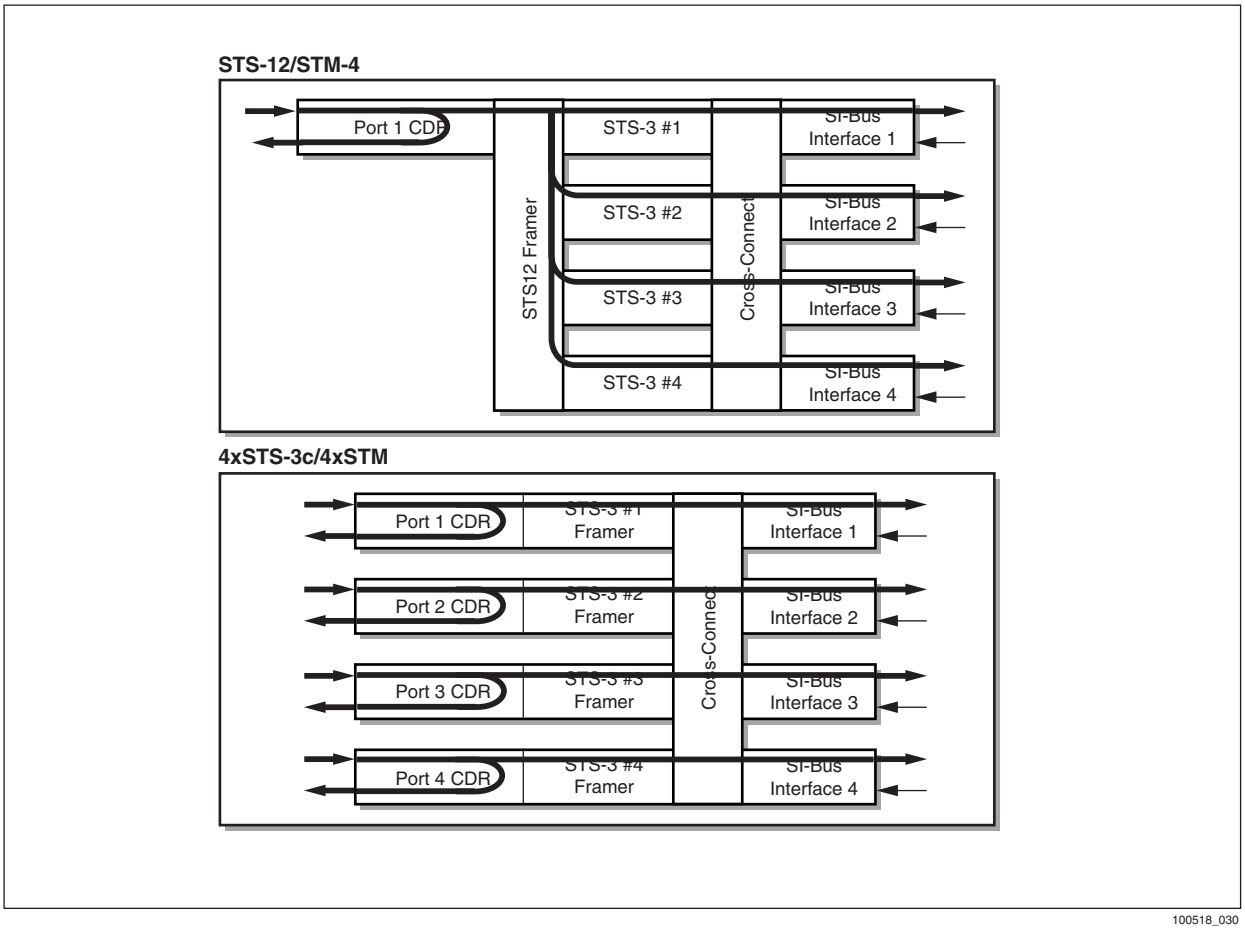
2.8 Loopback Modes

Loopbacks are diagnostic tools used to verify the data path. The CX29610 has two loopback modes: Line Loopback (which checks the line between a remote device and the PHY) and Source Loopback (which checks that the host (the SI-Bus) is communicating with the PHY).

2.8.1 Line Loopback

Line loopback is enabled or disabled in bit 0 of the CLKREC register. When Line loopback is enabled, all incoming data on the Receive Line Interface is retransmitted out the Transmit Line Interface. The received data is also passed through the PHY's normal path to be output on the SI-Bus interface.

Figure 2-26. Line Loopback Diagram



2.8.2 Source Loopback

Source loopback is enabled and disabled in bit 1 the CLKREC register. When source loopback is enabled, all data transmitted by the CX29610 is also looped back through the Receive Line Interface. Data from the LIU is ignored.

Figure 2-27. Source Loopback Diagram

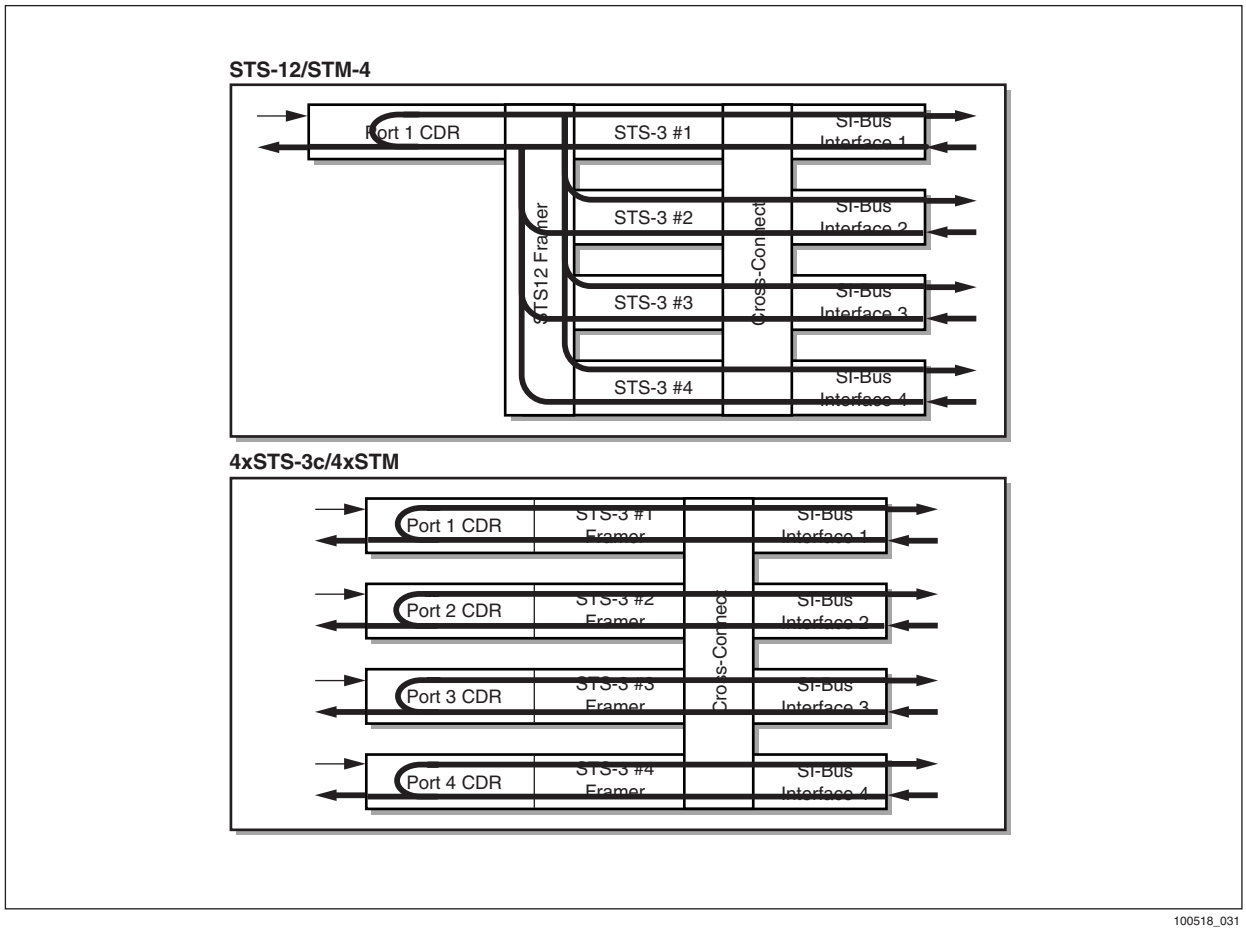


Figure 2-28. Line Loopback—Receive

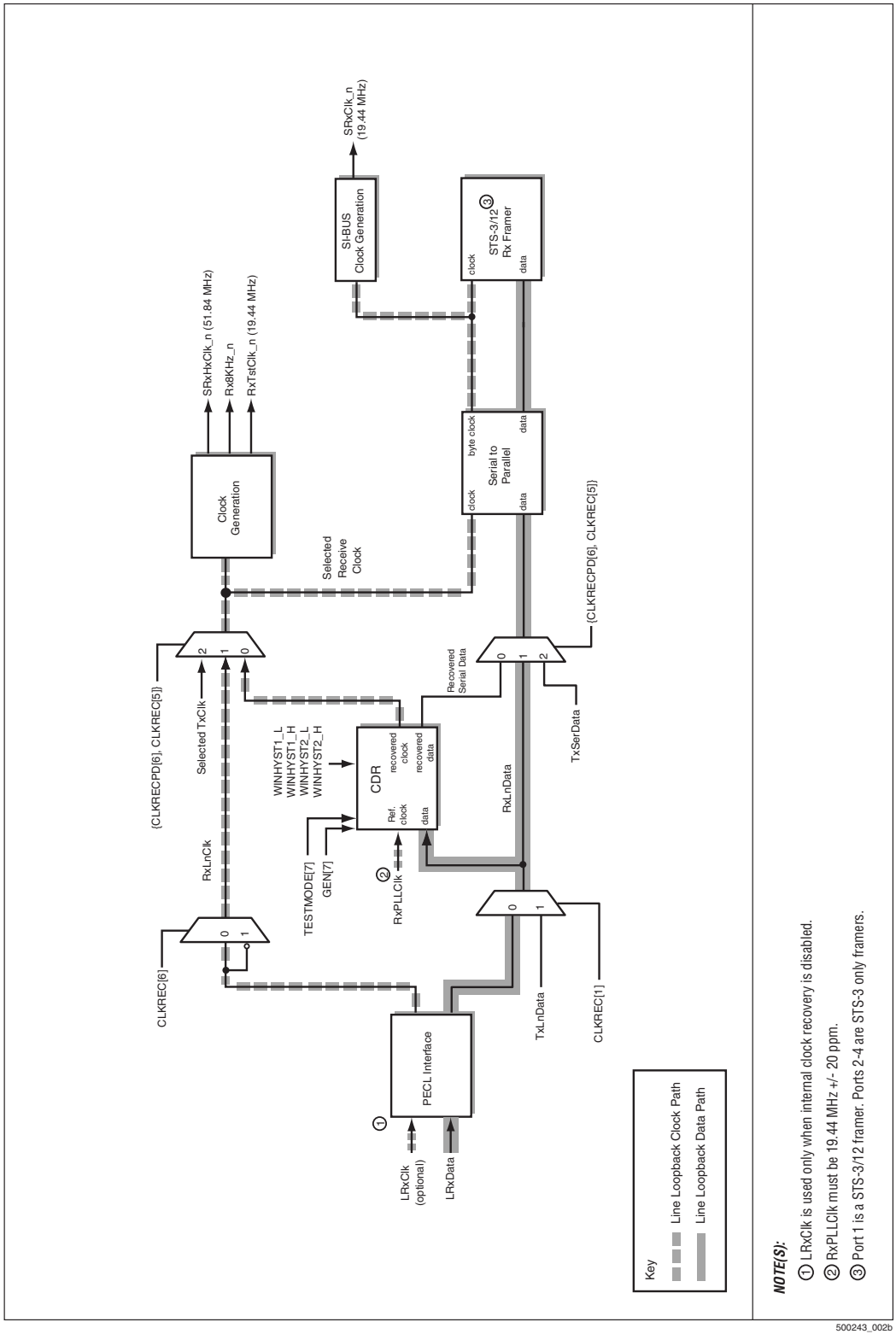


Figure 2-29. Line Loopback—Transmit

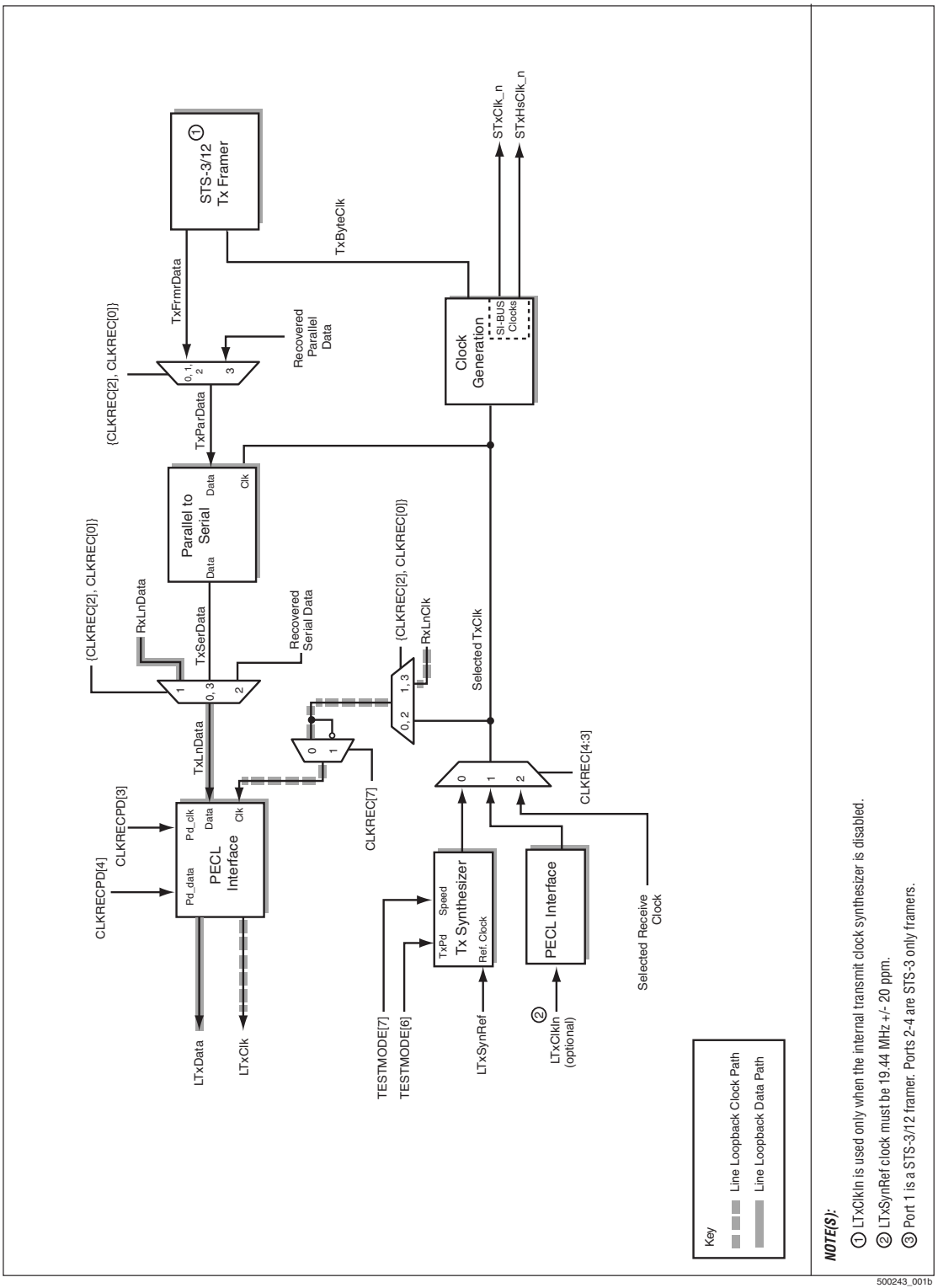


Figure 2-30. Local Source Loopback—Receive

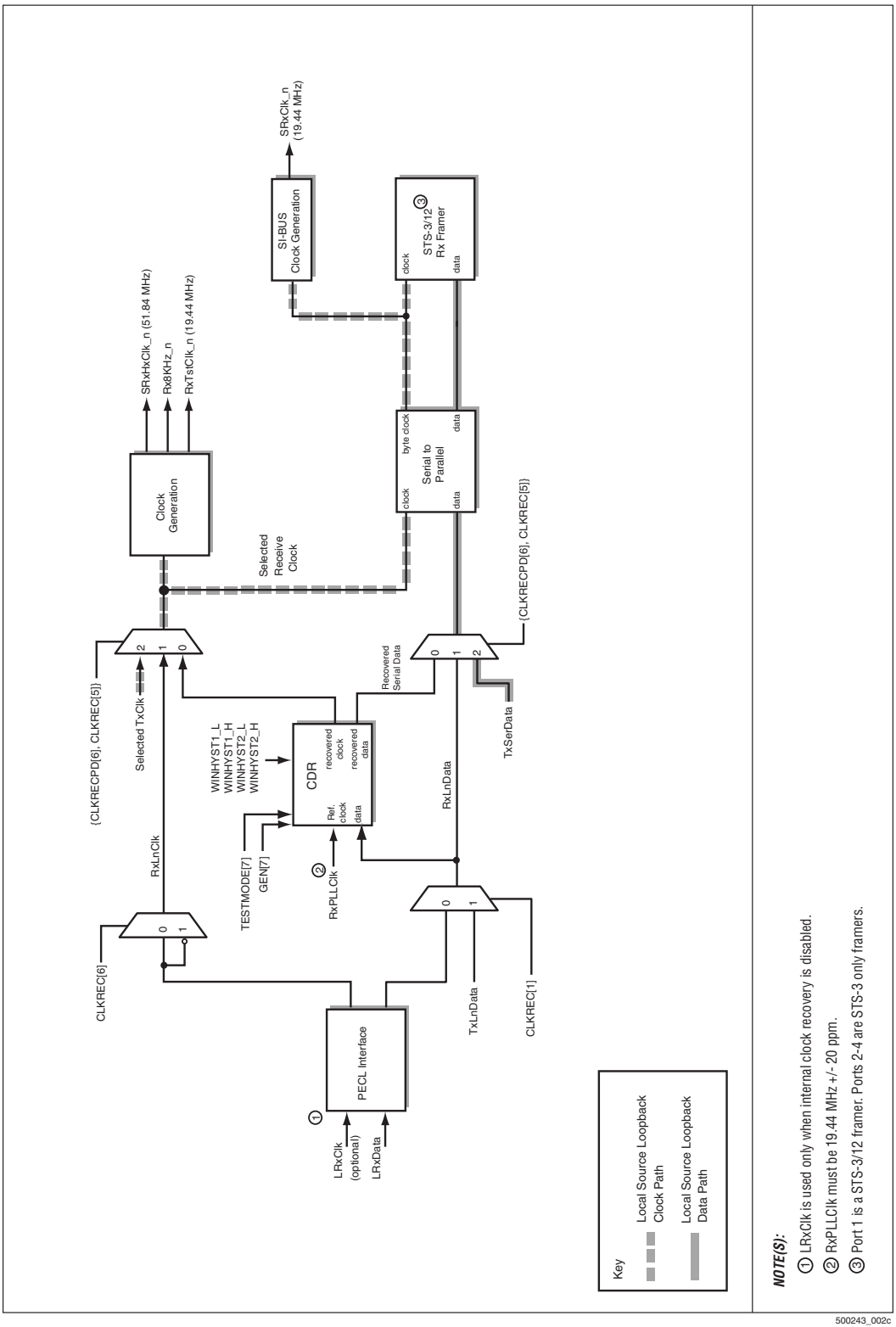


Figure 2-31. Local Source Loopback—Transmit

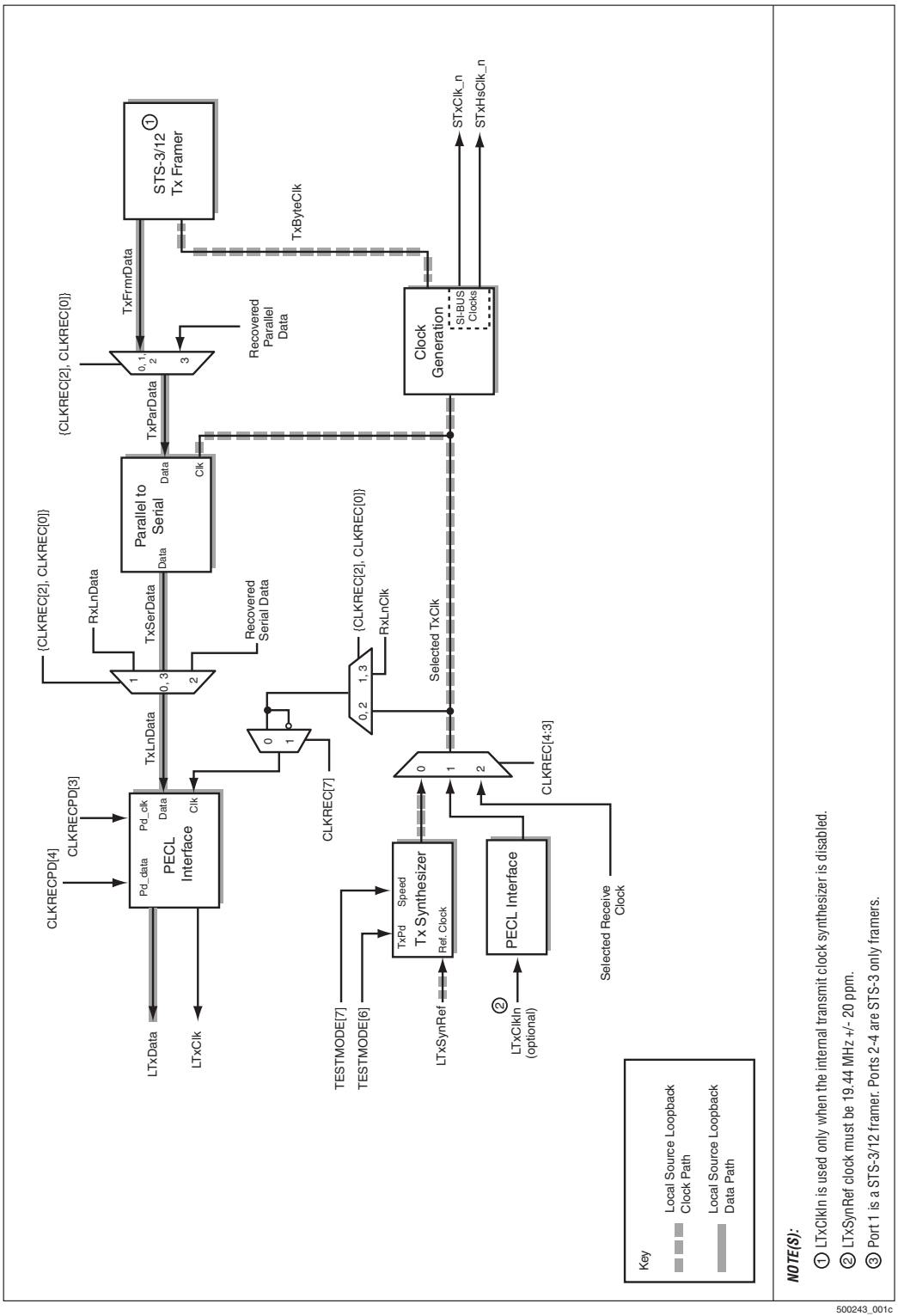


Figure 2-32. Source Loopback—Receive

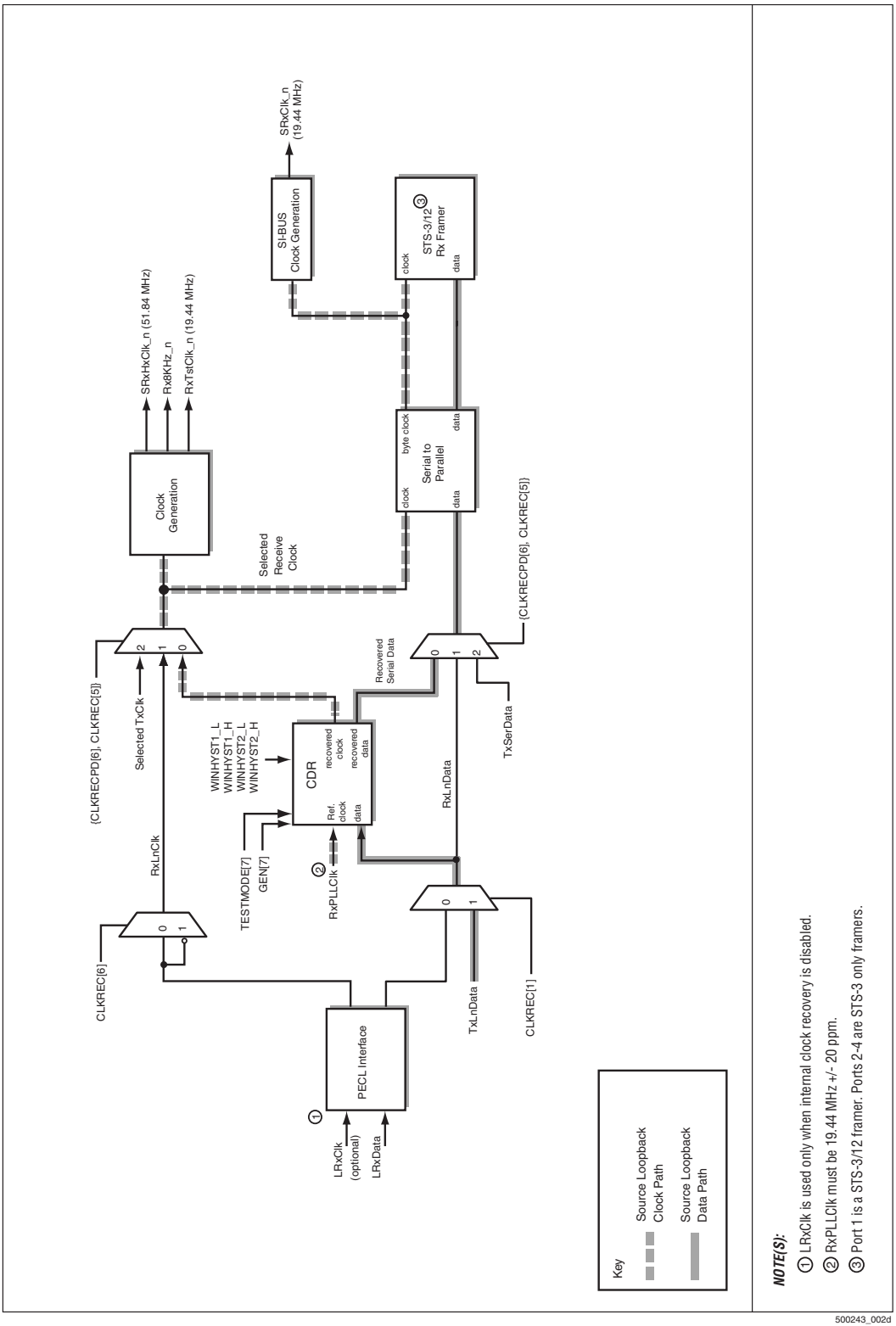
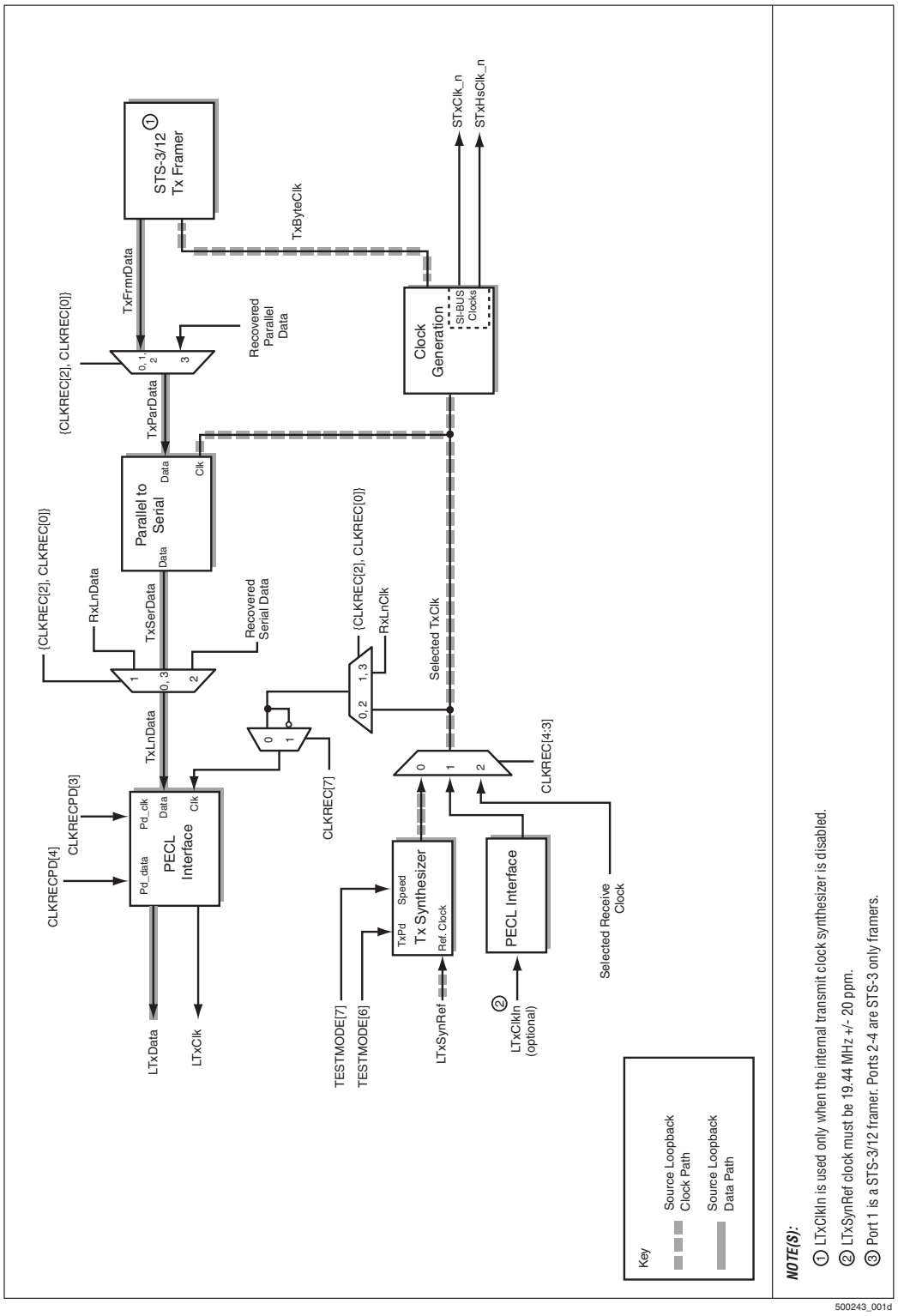


Figure 2-33. Source Loopback—Transmit



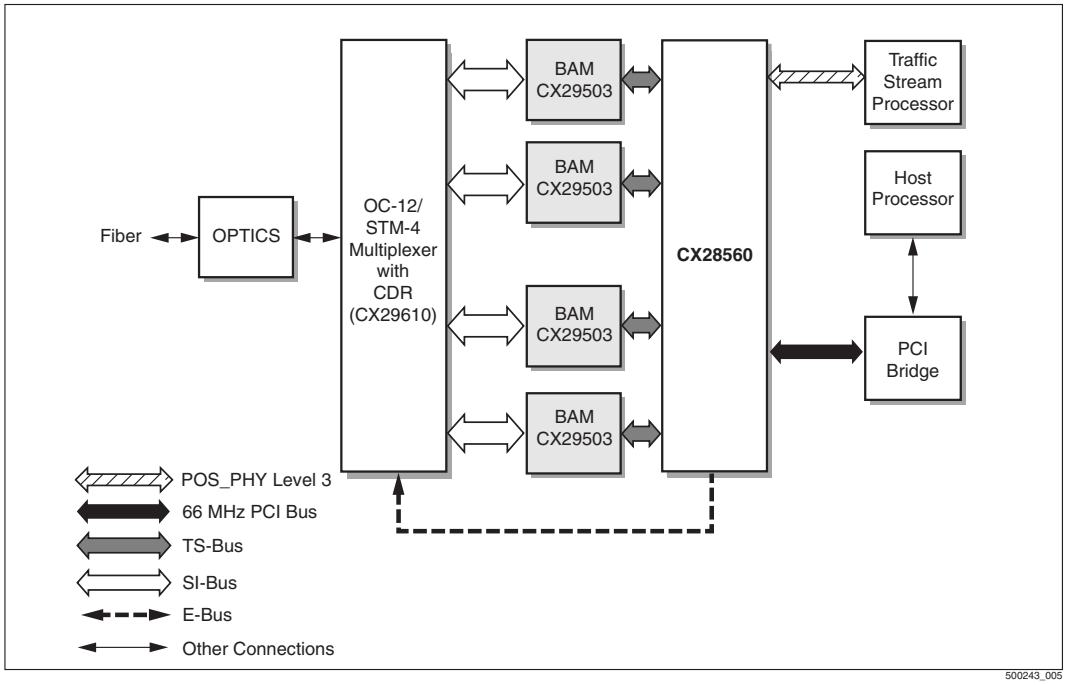
3.0 Applications

The CX29610 is targeted for network edge applications where SONET OC-12/OC-3 or SDH STM-4/STM-1 traffic is terminated for STS-1 payload processing. For HDLC processing applications, Mindspeed's CX28560 interfaces to the CX29610 for processing of 2,047 HDLC channels. Typical applications are illustrated in Figures 3-1 and 3-2.

3.1 OC-12/STM-4 Path Termination for HDLC Application

In the OC-12/STM-4 application, four CX29503 Broadband Access Multiplexer devices are used with a single CX29610 OC-12 SONET/SDH Multiplexer, and one CX28560 2,047 HDLC controller. This application allows for a termination of tributary signals down to DS1/E1.

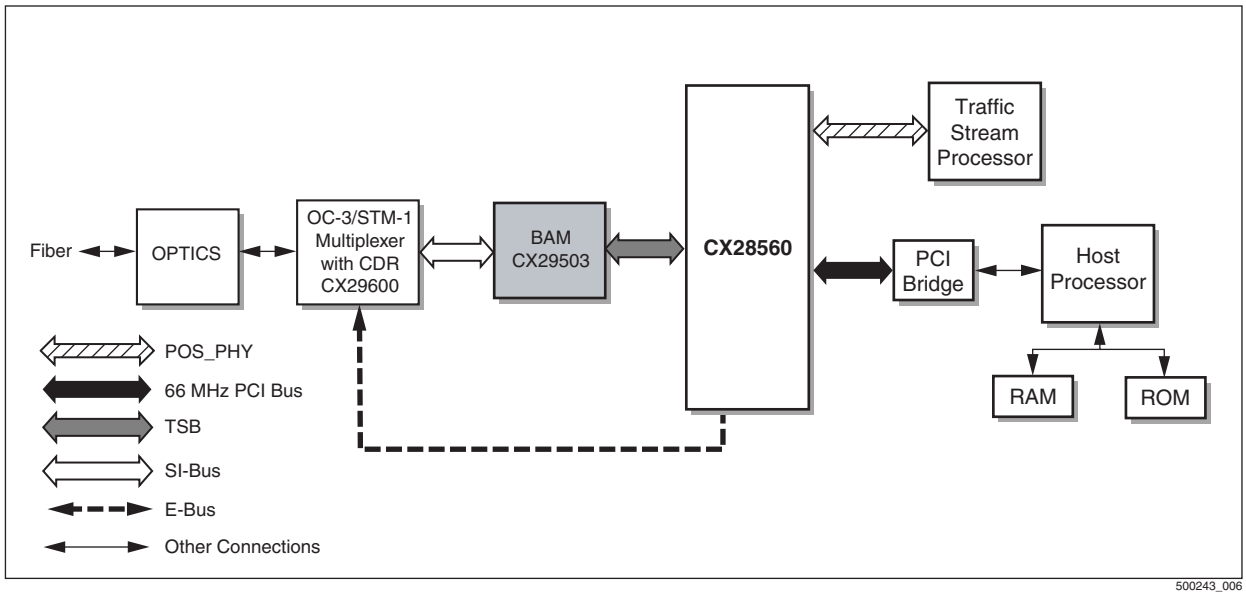
Figure 3-1. OC-12/STM-4 Channeled to DS1/E1 Application



3.2 OC-3/STM-1 Path Termination for HDLC Application

In the OC-3/STM-1 application, one CX29503 Broadband Access Multiplexer is used with a single OC-3 channel of the CX29610 SONET/SDH Multiplexer and one CX28560 2,047 Channel HDLC controller. This application allows for a termination of tributary signals down to DS1/E1.

Figure 3-2. OC-3/STM-1 Full DS0/E0 Channelization Application



4.0 Registers

4.1 Memory Map

The CX29610 memory space consists of 2048 bytes divided into 5 sections as shown in Table 4-1.

Table 4-1. Port Register Address Sections

Address	Description
0x000-00D	General Control/Status Registers
0x010-170	STS-12/STS-3 Port 1 Control/Status Registers
0x210-370	STS-3 Port 2 Control/Status Registers
0x410-570	STS-3 Port 3 Control/Status Registers
0x610-770	STS-3 Port 4 Control/Status Registers

The control/status register name assignments are the same for each port and are shown in Table 4-2. Some of the individual control bits are different between port 1 and the other ports due to the dual function of port 1 for STS-3 and STS-12 formats. These differences are noted in a later section.

Addresses not listed in Table 4-2 are currently not defined and should be treated as reserved for future use. Write operations to reserved addresses should not be performed and reads from reserved addresses produce undefined results.

Multi-byte registers (primarily counters) should be read least significant byte first to ensure proper latching of the count values during the read operation.

Section and Path Buffers

The section and path trace circular buffers each consist of 64 bytes arranged as a circular buffer accessible from a single read/write address. Each circular buffer is independent of the others. An internal, mod-64 address counter increments for each read/write operation to a particular circular buffer. Thus, 64 consecutive writes to the same address fills the buffer and returns to the starting address. The 64-byte J0 and J1 transmit circular buffers are implemented with a 16-bit wide internal buffer, **therefore two writes to the TXSECBUF or TXPTHBUF registers must be executed before the entire 16-bits is written to the internal buffers**. Reading the section and path buffers 64 consecutive times produces the current contents of the entire buffer and returns you to the starting address. The mod-64 address counters are set to 0 via reset; otherwise, the read/write position in the buffer is indeterminate. This does not matter in operation of the trace messages, however, since they do not have a particular start/end relationship to the SONET/SDH frame structure.

Register Map

The register map details the registers for 4xSTS-3 mode. Some registers take on different functionality in STS-12 mode vs. STS-3 mode. STS-3 numbering remains the same in either mode as shown in Figure 1-4 and Figure 1-5.

- TXSEC register—in STS-12 mode, only bit 3 of TXSEC is active for ports 2–4.
- TXLIN register—in STS-12 mode, only bit 4 of TXLIN is active for ports 2–4. This bit only controls the B2 bytes that are associated with the corresponding STS-3.
- In STS-12 mode, the TXF1/RXF1, TXK1/RXK1, and TXK2/RXK2 registers are inactive for ports 2–4.
- In STS-12 mode, the TXS1/RXS1 registers for ports 2–4 become TXZ1/RXZ1 registers for the corresponding STS-1 positions. There are no registers for the TXZ2/RXZ2 positions in STS-1 numbers 6, 9, and 12 in STS-12 mode (since these were formerly M1 bytes in 4xSTS-3 mode).
- In STS-12 mode, the B2 error insertion functions in the ERRINS registers for ports 2, 3, and 4 map to B2 bytes 4–6, 7–9, and 10–12, respectively. Other bits in the ERRINS register for ports 2–4 are inactive.

Table 4-2. Processor Memory Map *(1 of 12)*

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x000				GEN	R/W	—	General Control Register	page 4-28
0x001				PORTMAP	R/W	—	Port Mapping Control Register	page 4-35
0x002				BUSMODE	R/W	—	SI-Bus Mode Control Register	page 4-17
0x003				PWRDWN	R/W	—	Powerdown/Tristate Control Register	page 4-41
0x004				ENSUMINT	R/W	—	Summary Interrupt Mask Control Register	page 4-26
0x005				SUMINT	R	—	Summary Interrupt Indication Register	page 4-58
0x006				VERSION	R	—	Part Number/Version Status Register	page 4-70
0x007				TESTMODE	R/W	—	Test Mode for Counters	page 4-58
0x008				WINDOW_L	R/W	—	CDR window register (low byte)	page 4-71
0x009				WINDOW_H	R/W	—	CDR window register (high byte)	page 4-71
0x00A				WINHYST1_L	R/W	—	CDR hysteresis (low byte)	page 4-71
0x00B				WINHYST1_H	R/W	—	CDR hysteresis (high byte)	page 4-71
0x00C				WINHYST2_L	R/W	—	CDR hysteresis (low byte)	page 4-72
0x00D				WINHYST2_H	R/W	—	CDR hysteresis (high byte)	page 4-72
0x00E						—	Reserved	
0x00F						—	Reserved	
0x010	0x210	0x410	0x610	CNTMODE	R/W	—	Counter Mode Control Register	page 4-20
0x011	0x211	0x411	0x611	STATUS	R/W	—	Status Output Control Register	page 4-57
0x012	0x212	0x412	0x612			—	Reserved	
0x013	0x213	0x413	0x613	CLKRECPD	R/W	—	Clock Recovery/Power Down Control Register	page 4-19
0x014	0x214	0x414	0x614	CLKREC	R/W	—	Clock Recovery/Loopback Control Register	page 4-18

Table 4-2. Processor Memory Map *(2 of 12)*

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x015	0x215	0x415	0x615	ERRINS	R/W	—	Error Insertion Control Register	page 4-27
0x016	0x216	0x416	0x616	ERRPAT	R/W	—	Error Pattern Control Register	page 4-27
0x017	0x217	0x417	0x617	PRBS	R/W	—	Pseudo-Random Bit Sequence Control Register	
0x018	0x218	0x418	0x618	ENPORTINT	R	—	Summary Port Interrupt Mask Control Register	page 4-24
0x019	0x219	0x419	0x619	PORTINT	R	—	Summary Port Interrupt Indication Register	page 4-34
0x01A	0x21A	0x41A	0x61A			—	Reserved	
0x01B	0x21B	0x41B	0x61B			—	Reserved	
0x01C	0x21C	0x41C	0x61C	TXSEC	R/W	—	Transmit Section Overhead Control Register	page 4-68
0x01D	0x21D	0x41D	0x61D	TXLIN	R/W	—	Transmit Line Overhead Control Register	page 4-63
0x01E	0x21E	0x41E	0x61E	APSTHRESH	R/W	—	APS Threshold Control Register	page 4-14
0x01F	0x21F	0x41F	0x61F	DOWNALM	R/W	—	Downstream Alarm Control Register	page 4-21
0x020	0x220	0x420	0x620			—	Reserved	
0x021	0x221	0x421	0x621			—	Reserved	
0x022	0x222	0x422	0x622			—	Reserved	
0x023	0x223	0x423	0x623			—	Reserved	
0x024	0x224	0x424	0x624	TXF1	R/W	—	Transmit F1 Overhead Control Register	page 4-60
0x025	0x225	0x425	0x625	TXK1	R/W	—	Transmit K1 Overhead Control Register	page 4-62
0x026	0x226	0x426	0x626	TXK2	R/W	—	Transmit K2 Overhead Control Register	page 4-62
0x027	0x227	0x427	0x627	TXS1	R/W	—	Transmit S1 Overhead Control Register	page 4-67
0x028	0x228	0x428	0x628	TXZ1b	R/W	—	Transmit Z1b Overhead Control Register	page 4-69
0x029	0x229	0x429	0x629	TXZ1c	R/W	—	Transmit Z1c Overhead Control Register	page 4-69
0x02A	0x22A	0x42A	0x62A	TXZ2a	R/W	—	Transmit Z2a Overhead Control Register	page 4-69
0x02B	0x22B	0x42B	0x62B	TXZ2b	R/W	—	Transmit Z2b Overhead Control Register	page 4-70
0x02C	0x22C	0x42C	0x62C	TXZ2c	R/W	—	Transmit Z2c Overhead Control Register	page 4-70
0x02D	0x22D	0x42D	0x62D	RXF1	R	—	Receive F1 Overhead Status Register	page 4-45
0x02E	0x22E	0x42E	0x62E	RXK1	R	—	Receive K1 Overhead Status Register	page 4-47
0x02F	0x22F	0x42F	0x62F	RXK2	R	—	Receive K2 Overhead Status Register	page 4-48
0x030	0x230	0x430	0x630	RXS1	R	—	Receive S1 Overhead Status Register	page 4-53
0x031	0x231	0x431	0x631	RXZ1b	R	—	Receive Z1b Overhead Status Register	page 4-54
0x032	0x232	0x432	0x632	RXZ1c	R	—	Receive Z1c Overhead Status Register	page 4-54
0x033	0x233	0x433	0x633	RXZ2a	R	—	Receive Z2a Overhead Status Register	page 4-55

Table 4-2. Processor Memory Map (3 of 12)

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x034	0x234	0x434	0x634	RXZ2b	R	—	Receive Z2b Overhead Status Register	page 4-55
0x035	0x235	0x435	0x635	RXZ2c	R	—	Receive Z2c Overhead Status Register	page 4-55
0x036	0x236	0x436	0x636				Reserved	
0x037	0x237	0x437	0x637				Reserved	
0x038	0x238	0x438	0x638	ENSEC	R/W	—	Receive Section Interrupt Mask Control Register	page 4-26
0x039	0x239	0x439	0x639	ENLIN	R/W	—	Receive Line Interrupt Mask Control Register	page 4-22
0x03A	0x23A	0x43A	0x63A	ENAPS	R/W	—	APS Interrupt Mask Control Register	page 4-22
0x03B	0x23B	0x43B	0x63B				Reserved	
0x03C	0x23C	0x43C	0x63C	SECINT	R	—	Receive Section Interrupt Indication Status Register	page 4-56
0x03D	0x23D	0x43D	0x63D	LININT	R	—	Receive Line Interrupt Indication Status Register	page 4-29
0x03E	0x23E	0x43E	0x63E	APSINT	R	—	APS Interrupt Indication Status Register	page 4-14
0x03F	0x23F	0x43F	0x63F				Reserved	
0x040	0x240	0x440	0x640				Reserved	
0x041	0x241	0x441	0x641				Reserved	
0x042	0x242	0x442	0x642				Reserved	
0x043	0x243	0x443	0x643				Reserved	
0x044	0x244	0x444	0x644	RXSEC	R	Status	Receive Section Overhead Status Register	page 4-53
0x045	0x245	0x445	0x645	RXLIN	R	Status	Receive Line Overhead Status Register	page 4-49
0x046	0x246	0x446	0x646	RXAPS	R	Status	Receive APS Status Register	page 4-44
0x047	0x247	0x447	0x647				Reserved	
0x048	0x248	0x448	0x648	SEFCNT	R	Counters	Severely Errored Frame Event Counter	page 4-56
0x049	0x249	0x449	0x649				Reserved	
0x04A	0x24A	0x44A	0x64A				Reserved	
0x04B	0x24B	0x44B	0x64B				Reserved	
0x04C	0x24C	0x44C	0x64C	B1CNTL	R	Counters	Section BIP Error Counter (low byte)	page 4-15
0x04D	0x24D	0x44D	0x64D	B1CNTH	R	Counters	Section BIP Error Counter (high byte)	page 4-15
0x04E	0x24E	0x44E	0x64E				Reserved	
0x04F	0x24F	0x44F	0x64F				Reserved	
0x050	0x250	0x450	0x650	B2CNTL	R	Counters	Line BIP Error Counter (low byte)	page 4-16
0x051	0x251	0x451	0x651	B2CNTM	R	Counters	Line BIP Error Counter (mid byte)	page 4-16

Table 4-2. Processor Memory Map *(4 of 12)*

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x052	0x252	0x452	0x652	B2CNTH	R	Counters	Line BIP Error Counter (high byte)	page 4-15
0x053							Reserved	
0x054	0x254	0x454	0x654	RLCNTL	R	Counters	REI-L Error Counter (low byte)	page 4-42
0x055	0x255	0x455	0x655	RLCNTM	R	Counters	REI-L Error Counter (mid byte)	page 4-42
0x056	0x255	0x455	0x655	RLCNTH	R	Counters	REI-L Error Counter (high byte)	page 4-41
0x057							Reserved	
0x058	0x258	0x458	0x658	TXSECBUF	R/W	—	Transmit Section Trace Circular Buffer	page 4-68
0x059	0x259	0x459	0x659				Reserved	
0x05A	0x25A	0x45A	0x65A				Reserved	
0x05B	0x25B	0x45B	0x65B				Reserved	
0x05C	0x25C	0x45C	0x65C	RXSECBUF	R/W	—	Receive Section Trace Circular Buffer	page 4-54
0x05D	0x25D	0x45D	0x65D				Reserved	
0x05E	0x25E	0x45E	0x65E				Reserved	
0x05F	0x25F	0x45F	0x65F				Reserved	
0x080	0x280	0x480	0x680	TXPNTR-1	R/W	—	Pointer Control Register for Path 1	page 4-65
0x081	0x281	0x481	0x681	TXPTH-1	R/W	—	Transmit Overhead Control Register for Path 1	page 4-66
0x082	0x282	0x482	0x682	PTHINSL-1	R/W	—	Overhead Insertion Control Register (low byte) for Path 1	page 4-39
0x083	0x283	0x483	0x683	PTHINSH-1	R/W	—	Overhead Insertion Control Register (high byte) for Path 1	page 4-38
0x084	0x284	0x484	0x684	PROVC2-1	R/W	—	Provisioned C2 Control Register for Path 1	page 4-37
0x085	0x285	0x485	0x685	TXC2-1	R/W	—	Transmit C2 Overhead Control Register for Path 1	page 4-60
0x086	0x286	0x486	0x686	TXF2-1	R/W	—	Transmit F2 Overhead Control Register for Path 1	page 4-61
0x087	0x287	0x487	0x687	TXF3-1	R/W	—	Transmit F3 Overhead Control Register for Path 1	page 4-61
0x088	0x288	0x488	0x688	TXK3-1	R/W	—	Transmit K3 Overhead Control Register for Path 1	page 4-63
0x089	0x289	0x489	0x689	TXN1-1	R/W	—	Transmit N1 Overhead Control Register for Path 1	page 4-64
0x08A	0x28A	0x48A	0x68A				Reserved	
0x08B	0x28B	0x48B	0x68B				Reserved	
0x08C	0x28C	0x48C	0x68C	ENPTH-1	R/W	—	Receive Interrupt Mask Control Register for Path 1	page 4-25

Table 4-2. Processor Memory Map (5 of 12)

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x08D	0x28D	0x48D	0x68D	ENPNTR-1	R/W	—	Pointer Interrupt Mask Control Register for Path 1	page 4-23
0x08E	0x28E	0x48E	0x68E				Reserved	
0x08F	0x28F	0x48F	0x68F				Reserved	
0x090	0x290	0x490	0x690	PTHINT-1	R	—	Receive Interrupt Indication Status Register for Path 1	page 4-40
0x091	0x291	0x491	0x691	PNTRINT-1	R	—	Pointer Interrupt Indication Status Register for Path 1	page 4-32
0x092	0x292	0x492	0x692				Reserved	
0x093	0x293	0x493	0x693				Reserved	
0x094	0x294	0x494	0x694	RXPTH-1	R	Status	Receive Overhead Status Registerfor Path 1	page 4-51
0x095	0x295	0x495	0x695	RXPNTR-1	R	—	Receive H1H2 Pointer Value Status Register for Path 1	page 4-50
0x096	0x296	0x496	0x696	PNTRSTAT-1	R	Status bits 4–7	Receive H1H2 Pointer Action Status Register for Path 1	page 4-33
0x097	0x297	0x497	0x697				Reserved	
0x098	0x298	0x498	0x698	RXC2-1	R	—	Receive C2 Overhead Status Register for Path 1	page 4-44
0x099	0x299	0x499	0x699	RXF2-1	R	—	Receive F2 Overhead Status Register for Path 1	page 4-45
0x09A	0x29A	0x49A	0x69A	RXF3-1	R	—	Receive F3 Overhead Status Register for Path 1	page 4-46
0x09B	0x29B	0x49B	0x69B	RXK3-1	R	—	Receive K3 Overhead Status Register for Path 1	page 4-48
0x09C	0x29C	0x49C	0x69C	RXN1-1	R	—	Receive N1 Overhead Status Register for Path 1	page 4-49
0x09D	0x29D	0x49D	0x69D	RXRDI-1	R	—	Receive RDI-P Status Register for Path 1	page 4-52
0x09E	0x29E	0x49E	0x69E				Reserved	
0x09F	0x29F	0x49F	0x69F				Reserved	
0x0A0	0x2A0	0x4A0	0x6A0	B3CNTL-1	R	Counters	BIP Error Counter (low byte) for Path 1	page 4-17
0x0A1	0x2A1	0x4A1	0x6A1	B3CNTH-1	R	Counters	BIP Error Counter (high byte) for Path 1	page 4-16
0x0A2	0x2A2	0x4A2	0x6A2	RPCNTL-1	R	Counters	REI-P Error Counter (low byte) for Path 1	page 4-43
0x0A3	0x2A3	0x4A3	0x6A3	RPCNTH-1	R	Counters	REI-P Error Counter (high byte) for Path 1	page 4-43
0x0A4	0x2A4	0x4A4	0x6A4	TCCNTL-1	R	Counters	Tandem Conn. Error Counter (low byte) for Path 1	page 4-59
0x0A5	0x2A5	0x4A5	0x6A5	TCCNTH-1	R	Counters	Tandem Conn. Error Counter (high byte) for Path 1	page 4-59

Table 4-2. Processor Memory Map *(6 of 12)*

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x0A6	0x2A6	0x4A6	0x6A6				Reserved	
0x0A7	0x2A7	0x4A7	0x6A7	NDFCNT-1	R	Counters	New Data Flag Counter for Path 1	page 4-29
0x0A8	0x2A8	0x4A8	0x6A8	PJCNTL-1	R	Counters	Positive Justification Counter (low byte) for Path 1	page 4-31
0x0A9	0x2A9	0x4A9	0x6A9	PJCNTH-1	R	Counters	Positive Justification Counter (high byte) for Path 1	page 4-31
0x0AA	0x2AA	0x4AA	0x6AA	NJCNTL-1	R	Counters	Negative Justification Counter (low byte) for Path 1	page 4-30
0x0AB	0x2AB	0x4AB	0x6AB	NJCNTH-1	R	Counters	Negative Justification Counter (high byte) for Path 1	page 4-30
0x0AC	0x2AC	0x4AC	0x6AC	TXPTHBUF-1	R/W	—	Transmit Trace Circular Buffer for Path 1	page 4-67
0x0AD	0x2AD	0x4AD	0x6AD				Reserved	
0x0AE	0x2AE	0x4AE	0x6AE				Reserved	
0x0AF	0x2AF	0x4AF	0x6AF				Reserved	
0x0B0	0x2B0	0x4B0	0x6B0	RXPTHBUF-1	R/W	—	Receive Trace Circular Buffer for Path 1	page 4-52
0x0B1	0x2B1	0x4B1	0x6B1				Reserved	
0x0B2	0x2B2	0x4B2	0x6B2				Reserved	
0x0B3	0x2B3	0x4B3	0x6B3				Reserved	
0x0C0	0x2C0	0x4C0	0x6C0	TXPNTR-2	R/W	—	Pointer Control Register for Path 2	page 4-65
0x0C1	0x2C1	0x4C1	0x6C1	TXPTH-2	R/W	—	Transmit Overhead Control Register for Path 2	page 4-66
0x0C2	0x2C2	0x4C2	0x6C2	PTHINSL-2	R/W	—	Overhead Insertion Control Register (low byte) for Path 2	page 4-39
0x0C3	0x2C3	0x4C3	0x6C3	PTHINSH-2	R/W	—	Overhead Insertion Control Register (high byte) for Path 2	page 4-38
0x0C4	0x2C4	0x4C4	0x6C4	PROVC2-2	R/W	—	Provisioned C2 Control Register for Path 2	page 4-37
0x0C5	0x2C5	0x4C5	0x6C5	TXC2-2	R/W	—	TransmitC2 Overhead Control Register for Path 2	page 4-60
0x0C6	0x2C6	0x4C6	0x6C6	TXF2-2	R/W	—	Transmit F2 Overhead Control Register for Path 2	page 4-61
0x0C7	0x2C7	0x4C7	0x6C7	TXF3-2	R/W	—	Transmit F3 Overhead Control Register for Path 2	page 4-61
0x0C8	0x2C8	0x4C8	0x6C8	TXK3-2	R/W	—	Transmit K3 Overhead Control Register for Path 2	page 4-63
0x0C9	0x2C9	0x4C9	0x6C9	TXN1-2	R/W	—	Transmit N1 Overhead Control Register for Path 2	page 4-64
0x0CA	0x2CA	0x4CA	0x6CA				Reserved	

Table 4-2. Processor Memory Map (7 of 12)

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x0CB	0x2CB	0x4CB	0x6CB				Reserved	
0x0CC	0x2CC	0x4CC	0x6CC	ENPTH-2	R/W	—	Receive Interrupt Mask Control Register for Path 2	page 4-25
0x0CD	0x2CD	0x4CD	0x6CD	ENPNTR-2	R/W	—	Pointer Interrupt Mask Control Register for Path 2	page 4-23
0x0CE	0x2CE	0x4CE	0x6CE				Reserved	
0x0CF	0x2CF	0x4CF	0x6CF				Reserved	
0x0D0	0x2D0	0x4D0	0x6D0	PTHINT-2	R	—	Receive Interrupt Indication Status Register for Path 2	page 4-40
0x0D1	0x2D1	0x4D1	0x6D1	PNTRINT-2	R	—	Pointer Interrupt Indication Status Register for Path 2	page 4-32
0x0D2	0x2D2	0x4D2	0x6D2				Reserved	
0x0D3	0x2D3	0x4D3	0x6D3				Reserved	
0x0D4	0x2D4	0x4D4	0x6D4	RXPTH-2	R	Status	Receive Overhead Status Register for Path 2	page 4-51
0x0D5	0x2D5	0x4D5	0x6D5	RXPNTR-2	R	—	Receive H1H2 Pointer Value Status Register for Path 2	page 4-50
0x0D6	0x2D6	0x4D6	0x6D6	PNTRSTAT-2	R	Status bits 4–7	Receive H1H2 Pointer Action Status Register for Path 2	page 4-33
0x0D7	0x2D7	0x4D7	0x6D7				Reserved	
0x0D8	0x2D8	0x4D8	0x6D8	RXC2-2	R	—	Receive C2 Overhead Status Register for Path 2	page 4-44
0x0D9	0x2D9	0x4D9	0x6D9	RXF2-2	R	—	Receive F2 Overhead Status Register for Path 2	page 4-45
0x0DA	0x2DA	0x4DA	0x6DA	RXF3-2	R	—	Receive F3 Overhead Status Register for Path 2	page 4-46
0x0DB	0x2DB	0x4DB	0x6DB	RXK3-2	R	—	Receive K3 Overhead Status Register for Path 2	page 4-48
0x0DC	0x2DC	0x4DC	0x6DC	RXN1-2	R	—	Receive N1 Overhead Status Register for Path 2	page 4-49
0x0DD	0x2DD	0x4DD	0x6DD	RXRDI-2	R	—	Receive RDI-P Status Register for Path 2	page 4-52
0x0DE	0x2DE	0x4DE	0x6DE				Reserved	
0x0DF	0x2DF	0x4DF	0x6DF				Reserved	
0x0E0	0x2E0	0x4E0	0x6E0	B3CNTL-2	R	Counters	BIP Error Counter (low byte) for Path 2	page 4-17
0x0E1	0x2E1	0x4E1	0x6E1	B3CNTH-2	R	Counters	BIP Error Counter (high byte) for Path 2	page 4-16
0x0E2	0x2E2	0x4E2	0x6E2	RPCNTL-2	R	Counters	REI-P Error Counter (low byte) for Path 2	page 4-43
0x0E3	0x2E3	0x4E3	0x6E3	RPCNTH-2	R	Counters	REI-P Error Counter (high byte) for Path 2	page 4-43
0x0E4	0x2E4	0x4E4	0x6E4	TCCNTL-2	R	Counters	Tandem Conn. Error Counter (low byte)	page 4-59

Table 4-2. Processor Memory Map *(8 of 12)*

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x0E5	0x2E5	0x4E5	0x6E5	TCCNTH-2	R	Counters	Tandem Conn. Error Counter (high byte) for Path 2	page 4-59
0x0E6	0x2E6	0x4E6	0x6E6				Reserved	
0x0E7	0x2E7	0x4E7	0x6E7	NDFCNT-2	R	Counters	New Data Flag Counter for Path 2	page 4-29
0x0E8	0x2E8	0x4E8	0x6E8	PJCNTL-2	R	Counters	Positive Justification Counter (low byte) for Path 2	page 4-31
0x0E9	0x2E9	0x4E9	0x6E9	PJCNTH-2	R	Counters	Positive Justification Counter (high byte) for Path 2	page 4-31
0x0EA	0x2EA	0x4EA	0x6EA	NJCNTL-2	R	Counters	Negative Justification Counter (low byte) for Path 2	page 4-30
0x0EB	0x2EB	0x4EB	0x6EB	NJCNTH-2	R	Counters	Negative Justification Counter (high byte) for Path 2	page 4-30
0x0EC	0x2EC	0x4EC	0x6EC	TXPTHBUF-2	R/W	—	Transmit Trace Circular Buffer for Path 2	page 4-67
0x0ED	0x2ED	0x4ED	0x6ED				Reserved	
0x0EE	0x2EE	0x4EE	0x6EE				Reserved	
0x0EF	0x2EF	0x4EF	0x6EF				Reserved	
0x0F0	0x2F0	0x4F0	0x6F0	RXPTHBUF-2	R/W	—	Receive Trace Circular Buffer for Path 2	page 4-52
0x0F1	0x2F1	0x4F1	0x6F1				Reserved	
0x0F2	0x2F2	0x4F2	0x6F2				Reserved	
0x0F3	0x2F3	0x4F3	0x6F3				Reserved	
0x100	0x300	0x500	0x700	TXPNTR-3	R/W	—	Pointer Control Register for Path 3	page 4-65
0x101	0x301	0x501	0x701	TXPTH-3	R/W	—	Transmit Overhead Control Register for Path 3	page 4-66
0x102	0x302	0x502	0x702	PTHINSL-3	R/W	—	Overhead Insertion Control Register (low byte) for Path 3	page 4-39
0x103	0x303	0x503	0x703	PTHINSH-3	R/W	—	Overhead Insertion Control Register (high byte) for Path 3	page 4-38
0x104	0x304	0x504	0x704	PROVC2-3	R/W	—	Provisioned C2 Control Register for Path 3	page 4-37
0x105	0x305	0x505	0x705	TXC2-3	R/W	—	Transmit C2 Overhead Control Register for Path 3	page 4-60
0x106	0x306	0x506	0x706	TXF2-3	R/W	—	Transmit F2 Overhead Control Register for Path 3	page 4-61
0x107	0x307	0x507	0x707	TXF3-3	R/W	—	Transmit F3 Overhead Control Register for Path 3	page 4-61
0x108	0x308	0x508	0x708	TXK3-3	R/W	—	Transmit K3 Overhead Control Register for Path 3	page 4-63
0x109	0x309	0x509	0x709	TXN1-3	R/W	—	Transmit N1 Overhead Control Register for Path 3	page 4-64

Table 4-2. Processor Memory Map (9 of 12)

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x10A	0x30A	0x50A	0x70A				Reserved	
0x10B	0x30B	0x50B	0x70B				Reserved	
0x10C	0x30C	0x50C	0x70C	ENPTH-3	R/W	—	Receive Interrupt Mask Control Register for Path 3	page 4-25
0x10D	0x30D	0x50D	0x70D	ENPNTR-3	R/W	—	Pointer Interrupt Mask Control Register for Path 3	page 4-23
0x10E	0x30E	0x50E	0x70E				Reserved	
0x10F	0x30F	0x50F	0x70F				Reserved	
0x110	0x310	0x510	0x710	PTHINT-3	R	—	Receive Interrupt Indication Status Register for Path 3	page 4-40
0x111	0x311	0x511	0x711	PNTRINT-3	R	—	Pointer Interrupt Indication Status Register for Path 3	page 4-32
0x112	0x312	0x512	0x712				Reserved	
0x113	0x313	0x513	0x713				Reserved	
0x114	0x314	0x514	0x714	RXPTH-3	R	Status	Receive Overhead Status Register for Path 3	page 4-51
0x115	0x315	0x515	0x715	RXPNTR-2	R	—	Receive H1H2 Pointer Value Status Register for Path 3	page 4-50
0x116	0x316	0x516	0x716	PNTRSTAT-2	R	Status bits 4–7	Receive H1H2 Pointer Action Status Register for Path 3	page 4-33
0x117	0x317	0x517	0x717				Reserved	
0x118	0x318	0x518	0x718	RXC2-2	R	—	Receive C2 Overhead Status Register for Path 3	page 4-44
0x119	0x319	0x519	0x719	RXF2-2	R	—	Receive F2 Overhead Status Register for Path 3	page 4-45
0x11A	0x31A	0x51A	0x71A	RXF3-2	R	—	Receive F3 Overhead Status Register for Path 3	page 4-46
0x11B	0x31B	0x51B	0x71B	RXK3-2	R	—	Receive K3 Overhead Status Register for Path 3	page 4-48
0x11C	0x31C	0x51C	0x71C	RXN1-2	R	—	Receive N1 Overhead Status Register for Path 3	page 4-49
0x11D	0x31D	0x51D	0x71D	RXRDI-2	R	—	Receive RDI-P Status Register for Path 3	page 4-52
0x11E	0x31E	0x51E	0x71E				Reserved	
0x11F	0x31F	0x51F	0x71F				Reserved	
0x120	0x320	0x520	0x720	B3CNTL-3	R	Counters	BIP Error Counter (low byte) for Path 3	page 4-17
0x121	0x321	0x521	0x721	B3CNTH-3	R	Counters	BIP Error Counter (high byte) for Path 3	page 4-16
0x122	0x322	0x522	0x722	RPCNTL-3	R	Counters	REI-P Error Counter (low byte) for Path 3	page 4-43
0x123	0x323	0x523	0x723	RPCNTH-3	R	Counters	REI-P Error Counter (high byte) for Path 3	page 4-43

Table 4-2. Processor Memory Map *(10 of 12)*

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x124	0x324	0x524	0x724	TCCNTL-3	R	Counters	Tandem Conn. Error Counter (low byte) for Path 3	page 4-59
0x125	0x325	0x525	0x725	TCCNTH-3	R	Counters	Tandem Conn. Error Counter (high byte) for Path 3	page 4-59
0x126	0x326	0x526	0x726				Reserved	
0x127	0x327	0x527	0x727	NDFCNT-3	R	Counters	New Data Flag Counter for Path 3	page 4-29
0x128	0x328	0x528	0x728	PJCNTL-3	R	Counters	Positive Justification Counter (low byte) for Path 3	page 4-31
0x129	0x329	0x529	0x729	PJCNTH-3	R	Counters	Positive Justification Counter (high byte) for Path 3	page 4-31
0x12A	0x32A	0x52A	0x72A	NJCNTL-3	R	Counters	Negative Justification Counter (low byte) for Path 3	page 4-30
0x12B	0x32B	0x52B	0x72B	NJCNTH-3	R	Counters	Negative Justification Counter (high byte) for Path 3	page 4-30
0x12C	0x32C	0x52C	0x72C	TXPTHBUF-3	R/W	—	Transmit Trace Circular Buffer for Path 3	page 4-67
0x12D	0x32D	0x52D	0x72D				Reserved	
0x12E	0x32E	0x52E	0x72E				Reserved	
0x12F	0x32F	0x52F	0x72F				Reserved	
0x130	0x330	0x530	0x730	RXPTHBUF-3	R/W	—	Receive Trace Circular Buffer for Path 3	page 4-52
0x131	0x331	0x531	0x731				Reserved	
0x0132	0x332	0x532	0x732				Reserved	
0x133	0x333	0x533	0x733				Reserved	
0x134	0x334	0x534	0x734				Reserved	
0x135	0x335	0x535	0x735				Reserved	
0x136	0x336	0x536	0x736				Reserved	
0x137	0x337	0x537	0x737				Reserved	
0x140	0x340	0x540	0x740	TXPNTR-4	R/W	—	Pointer Control Register for Path 4	page 4-65
0x141	0x341	0x541	0x741	TXPTH-4	R/W	—	Transmit Overhead Control Register for Path 4	page 4-66
0x142	0x342	0x542	0x742	PTHINSL-4	R/W	—	Overhead Insertion Control Register (low byte) for Path 4	page 4-39
0x143	0x343	0x543	0x743	PTHINSH-4	R/W	—	Overhead Insertion Control Register (high byte) for Path 4	page 4-38
0x144	0x344	0x544	0x744	PROVC2-4	R/W	—	Provisioned C2 Control Register for Path 4	page 4-37
0x145	0x345	0x545	0x745	TXC2-4	R/W	—	Transmit C2 Overhead Control Register for Path 4	page 4-60

Table 4-2. Processor Memory Map (11 of 12)

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x146	0x346	0x546	0x746	TXF2-4	R/W	—	Transmit F2 Overhead Control Register for Path 4	page 4-61
0x147	0x347	0x547	0x747	TXF3-4	R/W	—	Transmit F3 Overhead Control Register for Path 4	page 4-61
0x148	0x348	0x548	0x748	TXK3-4	R/W	—	Transmit K3 Overhead Control Register for Path 4	page 4-63
0x149	0x349	0x549	0x749	TXN1-4	R/W	—	Transmit N1 Overhead Control Register for Path 4	page 4-64
0x14A	0x34A	0x54A	0x74A				Reserved	
0x14B	0x34B	0x54B	0x74B				Reserved	
0x14C	0x34C	0x54C	0x74C	ENPTH-4	R/W	—	Receive Interrupt Mask Control Register for Path 4	page 4-25
0x14D	0x34D	0x54D	0x74D	ENPNTR-4	R/W	—	Pointer Interrupt Mask Control Register for Path 4	page 4-23
0x14E	0x34E	0x54E	0x74E				Reserved	
0x14F	0x34F	0x54F	0x74F				Reserved	
0x150	0x350	0x550	0x750	PTHINT-4	R	—	Receive Interrupt Indication Status Register for Path 4	page 4-40
0x151	0x351	0x551	0x751	PNTRINT-4	R	—	Pointer Interrupt Indication Status Register for Path 4	page 4-32
0x152	0x352	0x552	0x752				Reserved	
0x153	0x353	0x553	0x753				Reserved	
0x154	0x354	0x554	0x754	RXPTH-4	R	Status	Receive Overhead Status Register for Path 4	page 4-51
0x155	0x355	0x555	0x755	RXPNTR-4	R	—	Receive H1H2 Pointer Value Status Register for Path 4	page 4-50
0x156	0x356	0x556	0x756	PNTRSTAT-4	R	Status bits 4–7	Receive H1H2 Pointer Action Status Register for Path 4	page 4-33
0x157	0x357	0x557	0x757				Reserved	
0x158	0x358	0x558	0x758	RXC2-4	R	—	Receive C2 Overhead Status Register for Path 4	page 4-44
0x159	0x359	0x559	0x759	RXF2-4	R	—	Receive F2 Overhead Status Register for Path 4	page 4-45
0x15A	0x35A	0x55A	0x75A	RXF3-4	R	—	Receive F3 Overhead Status Register for Path 4	page 4-46
0x15B	0x35B	0x55B	0x75B	RXK3-4	R	—	Receive K3 Overhead Status Register for Path 4	page 4-48
0x15C	0x35C	0x55C	0x75C	RXN1-4	R	—	Receive N1 Overhead Status Register for Path 4	page 4-49

Table 4-2. Processor Memory Map *(12 of 12)*

Address				Name	Type	OneSec Latching	Description	Page Number
Port 1	Port 2	Port 3	Port 4					
0x15D	0x35D	0x55D	0x75D	RXRDI-4	R	—	Receive RDI-P Status Register for Path 4	page 4-52
0x15E	0x35E	0x55E	0x75E				Reserved	
0x15F	0x35F	0x55F	0x75F				Reserved	
0x160	0x360	0x560	0x760	B3CNTL-4	R	Counters	BIP Error Counter (low byte) for Path 4	page 4-17
0x161	0x361	0x561	0x761	B3CNTH-4	R	Counters	BIP Error Counter (high byte) for Path 4	page 4-16
0x162	0x362	0x562	0x762	RPCNTL-4	R	Counters	REI-P Error Counter (low byte) for Path 4	page 4-43
0x163	0x363	0x563	0x763	RPCNTH-4	R	Counters	REI-P Error Counter (high byte) for Path 4	page 4-43
0x164	0x364	0x564	0x764	TCCNTL-4	R	Counters	Tandem Conn. Error Counter (low byte) for Path 4	page 4-59
0x165	0x365	0x565	0x765	TCCNTH-4	R	Counters	Tandem Conn. Error Counter (high byte) for Path 4	page 4-59
0x166	0x366	0x566	0x766				Reserved	
0x167	0x367	0x567	0x767	NDFCNT-4	R	Counters	New Data Flag Counter for Path 4	page 4-29
0x168	0x368	0x568	0x768	PJCNTL-4	R	Counters	Positive Justification Counter (low byte) for Path 4	page 4-31
0x169	0x369	0x569	0x769	PJCNTH-4	R	Counters	Positive Justification Counter (high byte) for Path 4	page 4-31
0x16A	0x36A	0x56A	0x76A	NJCNTL-4	R	Counters	Negative Justification Counter (low byte) for Path 4	page 4-30
0x16B	0x36B	0x56B	0x76B	NJCNTH-4	R	Counters	Negative Justification Counter (high byte) for Path 4	page 4-30
0x16C	0x36C	0x56C	0x76C	TXPTHBUF-4	R/W	—	Transmit Trace Circular Buffer for Path 4	page 4-67
0x16D	0x36D	0x56D	0x76D				Reserved	
0x16E	0x36E	0x56E	0x76E				Reserved	
0x16F	0x36F	0x56F	0x76F				Reserved	
0x170	0x370	0x570	0x770	RXPTHBUF-4	R/W	—	Receive Trace Circular Buffer for Path 4	page 4-52

NOTE: The registers in the following pages are presented in alphabetical order.

APSINT (APS/Pointer Interrupt Indication Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x03E	0x23E	0x43E	0x63E

The APSINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7-3	00000	—	Reserved, set to zero.
2	x	PSBFInt[1]	This bit indicates a Protection Switch Byte Failure interrupt has occurred.
1	x	SigFailInt[1]	This bit indicates a Signal Fail interrupt has occurred.
0	x	SigDegradeInt[1]	This bit indicates a Signal Degrade interrupt has occurred.
(1) Dual event interrupt—either a positive or negative transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.			

APSTHRESH (APS Threshold Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x01E	0x21E	0x41E	0x61E

The APSTHRESH register sets the threshold value for Signal Fail and Signal Degrade Alarm generation. Bits 7–4 are the signal fail threshold exponent (default = 10^{-3}) and bits 3–0 are the signal degrade threshold exponent (default = 10^{-6}). The valid is from three to nine; values less than three can be treated equal to three, values greater than nine can be treated as nine.

Bit	Default	Name	Description
7-4	0011	SFThresh[3:0]	Threshold exponent value for setting signal failed status—default is 10^{-3}.
3-0	0110	SDThresh[3:0]	Threshold exponent value for setting signal degraded status—default is 10^{-6}.

B1CNTH (Section BIP Error Counter [High Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x04D	0x24D	0x44D	0x64D

The B1CNTH counter tracks the number of Section BIP errors.

Bit	Default	Name	Description
7-0	xxh	B1Cnt[15:8]	Section BIP error counter high byte.

B1CNTL (Section BIP Error Counter [Low Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x04C	0x24C	0x44C	0x64C

The B1CNTL counter tracks the number of Section BIP errors.

Bit	Default	Name	Description
7-0	xxh	B1Cnt[7:0]	Section BIP error counter low byte.

B2CNTH (Line BIP Error Counter [High Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x052	0x252	0x452	0x652

The B2CNTH counter tracks the number of Line BIP errors.

Bit	Default	Name	Description
7-4	—	—	Reserved.
3-0	xxh	B2Cnt[19:16]	Line BIP error counter high byte.

B2CNTL (Line BIP Error Counter [Low Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x050	0x250	0x450	0x650

The B2CNTL counter tracks the number of Line BIP errors.

Bit	Default	Name	Description
7-0	xxh	B2Cnt[7:0]	Line BIP error counter low byte.

B2CNTM (Line BIP Error Counter [Mid Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x051	0x251	0x451	0x651

The B2CNTM counter tracks the number of Line BIP errors.

Bit	Default	Name	Description
7-0	xxh	B2Cnt[15:8]	Line BIP error counter mid byte.

B3CNTH (Path BIP Error Counter [High Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A1	0x2A1	0x4A1	0x6A1
Path 2	0x0E1	0x2E1	0x4E1	0x6E1
Path 3	0x121	0x321	0x521	0x721
Path 4	0x161	0x361	0x561	0x761

The B3CNTH counter tracks the number of Path BIP errors.

Bit	Default	Name	Description
7-0	xxh	B3Cnt[15:8]	Path BIP error counter high byte

B3CNTL (Path BIP Error Counter [Low Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A0	0x2A0	0x4A0	0x6A0
Path 2	0x0E0	0x2E0	0x4E0	0x6E0
Path 3	0x120	0x320	0x520	0x720
Path 4	0x160	0x360	0x560	0x760

The B3CNTL counter tracks the number of Path BIP errors. a payload defect.

Bit	Default	Name	Description
7-0	xxh	B3Cnt[7:0]	Path BIP error counter low byte.

BUSMODE (SI-Bus Mode Control Register)

The BUSMODE register controls the operating mode of the SI-Bus. Must be set to 0xAA for proper operation of the device

hex address: 0x002

Bit	Default	Name	Description
7-6	10	BusMode4[1:0]	Determines the operating mode of SI-Bus interface 4. Must be set to 10.
5-4	10	BusMode3[1:0]	Determines the operating mode of SI-Bus interface 3. Must be set to 10.
3-2	10	BusMode2[1:0]	Determines the operating mode of SI-Bus interface 2. Must be set to 10.
1-0	10	BusMode1[1:0]	Determines the operating mode of SI-Bus interface 1. Must be set to 10.

CLKREC (Clock Recovery/Loopback Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x014	0x214	0x414	0x614

The CLKREC register controls the clock recovery and loopback testing capabilities of the device.

Bit	Default	Name	Description
7	0	InvTxClk	When written to 1, the Transmit Clock output is inverted.
6	0	InvRxClk	When written to 1, the receiver uses the falling edge of the Receive Clock input to sample data.
5	0	ExtClkRec	When written to 0, internal clock recovery is enabled. When written to 1, the internal clock recovery circuit is bypassed.
4-3	00	TxClkSel[1:0]	Transmit clock source selection. 00—synthesized from external 19.44 MHz reference 01—provided externally on LTXCLKINp/n input pins 10—sourced from recovered receive clock (loop timing) TxFrameIn = pin 11—sourced from recovered receive clock (loop timing) TxFrameIn = RxFrameOut. This is useful for DCC and E1/E2 byte loopback mode where the received section and line DCC and E1/E2 overhead bytes are inserted into the transmit frame.
2	0	TxDataSel	When written to 1, the recovered serial data from the CDR is looped back to the transmit LTxDatap/n outputs.
1	0	SrcLoop	When written to 1, Source Loopback is enabled. This loopback connects the line-side transmitter clock/data outputs to the line-side receiver clock/data inputs.
0	0	NELnLoop	When written to 1, Near End Line Loopback is enabled. This loopback connects the line-side receive PECL clock/data inputs to the line-side transmit PECL clock/data outputs.

CLKRECPD (Clock Recovery/Power Down Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x013	0x213	0x413	0x613

The CLKRECPD register controls the CDR powerdown logic and VCO clock select.

Bit	Default	Name	Description
7	0	VcoTstClk_sel	VCO test clock select 0—normal 1—LRxClk is selected.
6	0	LclSrcLoop	Enable local source loopback. In this mode the CDR is bypassed. The SONET/SDH transmit frame data is looped to the SONET/SDH receiver internally.
5	0	—	Reserved
4	0	PD_Data	Powerdown LTxData buffer
3	1	PD_Clk	When written to 1, powerdown LTxClk buffer
2	0	PD_Ser	Powerdown serializer
1	0	PD_Des	Powerdown de-serializer
0	0	PD_CDR	Powerdown CDR

CNTMODE (Counter Mode Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x010	0x210	0x410	0x610

The CNTMODE register controls the controls the counter modes and enables one-second latching of status and counters.

Bit	Default	Name	Description
7	0	SecBIPCnt	When written to 0, the actual number of B1 BIP errors received are added to the respective error counter. When written to 1, B1 BIP errors received increment the respective error counter by 1 count for each errored frame.
6	0	LinBIPCnt	When written to 0, the actual number of B2 BIP errors received are added to the respective error counter. When written to 1, B2 BIP errors received increment the respective error counter by 1 count for each errored frame.
5	0	PthBIPCnt	When written to 0, the actual number of B3 BIP errors received are added to the respective error counter. When written to 1, B3 BIP errors received increment the respective error counter by 1 count for each errored frame.
4	0	LinREICnt	When written to 0, the actual number of REI-L errors received are added to the respective error counter. When written to 1, REI-L errors received increment the respective error counter by 1 count for each errored frame.
3	0	PthREICnt	When written to 0, the actual number of REI-P errors received are added to the respective error counter. When written to 1, REI-P errors received increment the respective error counter by 1 count for each errored frame.
2	0	EnStatLat	When written to 1, one-second status latching is enabled for all status registers. When written to 0, status registers are updated continuously.
1	0	EnCntrLat	When written to 1, one-second latching is enabled for all error counters. When written to 0, error count information is updated continuously.
0	0	—	Reserved, set to zero.

DOWNALM (Downstream Alarm Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x01F	0x21F	0x41F	0x61F

The DOWNALM register controls the downstream AIS options, receive scrambler disable, and receive pointer replication.

Bit	Default	Name	Description
7	1	AutoDownAIS-L	When written to 1, automatic generation of downstream AIS-L is enabled. When written to 0, automatic generation is disabled.
6	1	AutoDownAIS-P1	When written to 1, automatic generation of downstream AIS-P for STS path 1 is enabled. When written to 0, automatic generation is disabled.
5	1	AutoDownAIS-P2	When written to 1, automatic generation of downstream AIS-P for STS path 2 is enabled. When written to 0, automatic generation is disabled.
4	1	AutoDownAIS-P3	When written to 1, automatic generation of downstream AIS-P for STS path 3 is enabled. When written to 0, automatic generation is disabled.
3	0	DisRxScr	When written to 1, the receive frame scrambler is disabled.
2	0	RptPntr	When written to 1, the H1, H2, and H4 bytes in the first STS-1 are replicated into the second and third STS-1 H1, H2, and H4 positions. When written to 0, the H1, H2, and H4 bytes in the second and third STS-1s are passed as received.
1	0	LabelAIS-P	When written to 1, downstream AIS-P is also generated on reception of PLM-P or Uneq-P. This bit controls all three STS-1s in this STS-3. When written to 0, AIS-P is generated only on reception of LOP-P.
0	1	AutoDownAIS-P4	When written to 1, automatic generation of downstream AIS-P for STS path 4 is enabled. When written to 0, automatic generation is disabled.

ENAPS (APS Interrupt Mask Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x03A	0x23A	0x43A	0x63A

The ENAPS register controls APS interrupt enables.

Bit	Default	Name	Description
7-3	00000	—	Reserved, set to zero.
2	0	EnPSBF	This bit enables the Protection Switch Byte Failure interrupt.
1	0	EnSigFail	This bit enables the Signal Fail interrupt.
0	0	EnSigDegrade	This bit enables the Signal Degrade interrupt.

ENLIN (Receive Line Interrupt Mask Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x039	0x239	0x439	0x639

The ENLIN register controls line interrupt enables.

Bit	Default	Name	Description
7	0	EnK1K2	This bit enables the K1K2 interrupt.
6	0	EnAIS-L	This bit enables the AIS-L interrupt.
5	0	EnRDI-L	This bit enables the RDI-L interrupt.
4	0	EnB2Err	This bit enables the Line BIP Error interrupt.
3	0	EnREI-L	This bit enables the REI-L interrupt.
2	0	EnS1Intr	This bit enables the S1 byte change interrupt.
1	0	EnS1_UnstableIntr	This bit enables the S1_Unstable byte change interrupt.
0	0	EnZ1Z2Intr	This bit enables the Z1 or Z2 byte change interrupt.

ENPNTR (Pointer Interrupt Mask Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x08D	0x28D	0x46D	0x66D
Path 2	0x0CD	0x2CD	0x4CD	0x6CD
Path 3	0x10D	0x30D	0x50D	0x70D
Path 4	0x14D	0x34D	0x54D	0x74D

The ENPNTR register controls the pointer interrupt enables.

Bit	Default	Name	Description
7	0	EnNDFInt	This bit enables the RxNDF interrupt.
6	0	EnIncrInt	This bit enables the RxIncr interrupt.
5	0	EnDecrInt	This bit enables the RxDecr interrupt.
4	0	EnNewPntrInt	This bit enables the NewPntr interrupt.
3	0	EnF2Int	This bit enables the F2 byte change interrupt.
2	0	EnF3Int	This bit enables the F3 byte change interrupt.
1	0	EnK3Int	This bit enables the K3 byte change interrupt.
0	0	EnISFInt	This bit enables the ISF Error interrupt.

ENPORTINT (Summary Port Interrupt Mask Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x018	0x218	0x418	0x618

The ENPORTINT register controls the summary port interrupt enables.

Bit	Default	Name	Description
7	0	EnSectionIntr	This bit is a global enable for SONET Section interrupt sources in this port when set to 1.
6	0	EnLineIntr	This bit is a global enable for SONET Line interrupt sources in this port when set to 1.
5	0	EnAPSIntr	This bit is a global enable for APS/Pointer interrupt sources in this port when set to 1.
4	0	EnPath1Intr	This bit is a global enable for SONET Path/Pointer 1 interrupt sources in this port when set to 1.
3	0	EnPath2Intr	This bit is a global enable for SONET Path/Pointer 2 interrupt sources in this port when set to 1.
2	0	EnPath3Intr	This bit is a global enable for SONET Path/Pointer 3 interrupt sources in this port when set to 1.
1	0	EnPath4Intr	This bit is a global enable for SONET Path/Pointer 4 interrupt sources in this port when set to 1.
0	0	EnSIParIntr	This bit enables the SI-Bus parity error interrupt.

ENPTH (Receive Path Interrupt Mask Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x08C	0x28C	0x46C	0x66C
Path 2	0x0CC	0x2CC	0x4CC	0x6CC
Path 3	0x10C	0x30C	0x50C	0x70C
Path 4	0x14C	0x34C	0x54C	0x74C

The ENPTH register controls receive path interrupt enables.

Bit	Default	Name	Description
7	0	EnLOP-P	This bit enables the LOP-P interrupt.
6	0	EnAIS-P	This bit enables the AIS-P interrupt.
5	0	EnRDI-P	This bit enables the RDI-P interrupt.
4	0	EnB3Err	This bit enables the Path BIP Error interrupt.
3	0	EnREI-P	This bit enables the REI-P interrupt.
2	0	EnPLM-P	This bit enables the PLM-P interrupt.
1	0	EnUneq-P	This bit enables the Uneq-P interrupt.
0	0	EnPthTrace	This bit enables the Path Trace interrupt.

ENSEC (Receive Section Interrupt Mask Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x038	0x238	0x438	0x638

The ENSEC register controls section interrupt enables.

Bit	Default	Name	Description
7	0	EnSigDet	This bit enables the Signal Detect interrupt.
6	0	EnLOL	This bit enables the Loss of Lock interrupt.
5	0	EnLOS	This bit enables the Loss of Signal interrupt.
4	0	EnSEF	This bit enables the Out of Frame interrupt.
3	0	EnLOF	This bit enables the Loss of Frame interrupt.
2	0	EnB1Err	This bit enables the Section BIP Error interrupt.
1	0	EnSecTrace	This bit enables the Section Trace interrupt.
0	0	EnF1Intr	This bit enables the F1 byte change interrupt.

ENSUMINT (Summary Interrupt Mask Control Register)

hex address: 0x004

The ENSUMINT register determines which of the interrupts listed in SUMINT are observed on MIntr*.

Bit	Default	Name	Description
7-6	00	—	Reserved, set to zero.
5	0	EnPLLRefInt	Enables the PLL Reference status interrupt to appear on the MIntr* pin.
4	0	EnOneSecInt	Enables the One Second Interrupt to appear on the MIntr* pin.
3	0	EnPort4Int	This bit is a global enable for Port4 interrupt sources when set to 1.
2	0	EnPort3Int	This bit is a global enable for Port3 interrupt sources when set to 1.
1	0	EnPort2Int	This bit is a global enable for Port2 interrupt sources when set to 1.
0	0	EnPort1Int	This bit is a global enable for Port1 interrupt sources when set to 1.

ERRINS (Error Insertion Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x015	0x215	0x415	0x615

The ERRINS register controls error insertion into various octets for diagnostic purposes. These bits are automatically cleared by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register.

Bit	Default	Name	Description
7	0	InsFrErr	When written to 1, this bit causes the last A1 byte to be inverted for 1 transmit frame. When written to 0, the A1 byte is not inverted.
6	0	InsB1Err	When written to 1, this bit causes the B1 BIP calculation to be XORed with the value in the ERRPAT register for 1 transmit frame.
5	0	InsB2Err1	When written to 1, this bit causes the B2-1 BIP calculation to be XORed with the value in the ERRPAT register for 1 transmit frame.
4	0	InsB2Err2	When written to 1, this bit causes the B2-2 BIP calculation to be XORed with the value in the ERRPAT register for 1 transmit frame.
3	0	InsB2Err3	When written to 1, this bit causes the B2-3 BIP calculation to be XORed with the value in the ERRPAT register for 1 transmit frame.
2	0	InsREI-L	When written to 1, this bit causes the contents of the ERRPAT register to be transmitted as the REI-L value in the M1 byte for 1 transmit frame.
1	0	InsPrbsErr	Force a prbs error to be generated by the PRBS generator.
0	0	—	Reserved, set to zero.

ERRPAT (Error Pattern Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x016	0x216	0x416	0x616

The ERRPAT register provides the error pattern for the error insertion functions listed in the ERRINS register. Each bit in the error pattern register is XORed with the corresponding bit of the octet to be errored.

Bit	Default	Name	Description
7-0	00h	ErrPat[7:0]	Error pattern used by Error Insertion Control Register.

GEN (General Control Register)

hex address: 0x000

The GEN register controls the receiver hold input pin, one-second latch enables, block mode error counting, status pin selection, and device reset.

Bit	Default	Name	Description
7	1	PrtMode	When written to 0, the mode of operation is 4 independent STS-3 interfaces. When written to 1, the mode of operation is a single STS-12 interface on port 1. The other ports should be powered down.
6	0	FrmMode	When written to 0, the mode of operation is SONET. When written to 1, the mode of operation is SDH. This mode only affects Z0 insertion.
5	0	AU4Mode	When written to 0, the payload mapping is via AU-3. When written to 1, the payload mapping is via AU-4.
4	0	EnIntPin	When written to 1, the interrupt output pin Mint* is enabled. When written to 0, the interrupt output is three-stated.
3	0	TU3Mode	When written to 0, the payload mapping is via TUG-2. When written to 1, the payload mapping is via TU-3.[1]
2	0	CDRReset	Active high reset control to the CDR. Since the CDR is not reset by the chip reset pin, use this register to reset the CDR.
1	0	LogicReset	When written to 1, all internal state machines are held in reset mode but register contents are not affected.
0	0	MasterReset	When written to 1, all internal state machines are held in reset mode AND all control registers are set to their default values (except bit 0 in this register).

NOTE(S):
(1) This is only valid when mapping the payload in SDH and AU-4 modes.

LININT (Receive Line Interrupt Indication Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x03D	0x23D	0x43D	0x63D

The LININT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	K1K2Int[1]	This bit indicates that a K1K2 interrupt has occurred.
6	x	AIS-LInt[2]	This bit indicates that an AIS-L interrupt has occurred.
5	x	RDI-LInt[2]	This bit indicates that an RDI-L interrupt has occurred.
4	x	B2ErrInt[1]	This bit indicates that a Line BIP Error interrupt has occurred.
3	x	REI-LInt[1]	This bit indicates that an REI-L interrupt has occurred.
2	x	S1Int[1]	This bit indicates that an S1 byte change interrupt has occurred.
1	x	S1_UnstableInt[1]	This bit indicates that a S1_Unstable byte change interrupt has occurred.
0	x	Z1Z2Int[1]	This bit indicates that a Z1 or Z2 byte change interrupt has occurred.

NOTE(S):
(1) Single event interrupt—only a positive transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.
(2) Dual event interrupt—either a positive or negative transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.

NDFCNT (New Data Flag Counter)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A7	0x2A7	0x4A7	0x6A7
Path 2	0x0E7	0x2E7	0x4E7	0x6E7
Path 3	0x127	0x327	0x527	0x727
Path 4	0x167	0x367	0x567	0x767

The NDFCNT counter implements the 8-bit New Data Flag Event Counter.

Bit	Default	Name	Description
7-0	xxh	NDFCnt[7:0]	New Data Flag Event Counter

NJCNTH (Negative Pointer Justification Counter [High Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0AB	0x2AB	0x4AB	0x6AB
Path 2	0x0EB	0x2EB	0x4EB	0x6EB
Path 3	0x12B	0x32B	0x52B	0x72B
Path 4	0x16B	0x36B	0x56B	0x76B

The NJCNTH counter controls the high bits of the 11-bit Negative Pointer Justification Counter.

Bit	Default	Name	Description
7-3	—	—	Reserved, set to zero.
2-0	xxh	NJCnt[10:8]	Negative pointer justification counter high byte

NJCNTL (Negative Pointer Justification Counter [Low Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0AA	0x2AA	0x4AA	0x6AA
Path 2	0x0EA	0x2EA	0x4EA	0x6EA
Path 3	0x12A	0x32A	0x52A	0x72A
Path 4	0x16A	0x36A	0x56A	0x76A

The NJCNTL counter controls the low byte of the 11-bit Negative Pointer Justification Counter.

Bit	Default	Name	Description
7-0	xxh	NJCnt[7:0]	Negative pointer justification counter low byte

PJCNTH (Positive Pointer Justification Counter [High Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A9	0x2A9	0x4A9	0x6A9
Path 2	0x0E9	0x2E9	0x4E9	0x6E9
Path 3	0x129	0x329	0x529	0x729
Path 4	0x169	0x369	0x569	0x769

The PJCNTH counter controls the high bits of the 11-bit Positive Pointer Justification Counter.

Bit	Default	Name	Description
7-3	—	—	Reserved, set to zero.
2-0	xxh	PJCnt[10:8]	Positive pointer justification counter high byte

PJCNTL (Positive Pointer Justification Counter [Low Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A8	0x2A8	0x4A8	0x6A8
Path 2	0x0E8	0x2E8	0x4E8	0x6E8
Path 3	0x128	0x328	0x528	0x728
Path 4	0x168	0x368	0x568	0x768

The PJCNTL counter controls the low bits of the 11-bit Positive Pointer Justification Counter.

Bit	Default	Name	Description
7-0	xxh	PJCnt[7:0]	Positive pointer justification counter low byte

PNTRINT (Pointer Interrupt Indication Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x091	0x291	0x491	0x691
Path 2	0x0D1	0x2D1	0x4D1	0x6D1
Path 3	0x111	0x311	0x511	0x711
Path 4	0x151	0x351	0x551	0x751

The PNTRINT register indicates that a receive path pointer interrupt or other path interrupt has occurred.

Bit	Default	Name	Description
7	x	RxNDFInt[1]	This bit indicates that a RxNDF interrupt has occurred.
6	x	RxIncrInt[1]	This bit indicates that a RxIncr interrupt has occurred.
5	x	RxDecrInt[1]	This bit indicates that a RxDecr interrupt has occurred.
4	x	RxNewPntrInt[1]	This bit indicates that a RxNewPntr interrupt has occurred.
3	x	F2Int[1]	This bit indicates that an F2 byte change interrupt has occurred.
2	x	F3Int[1]	This bit indicates that an F3 byte change interrupt has occurred.
1	x	K3Int[1]	This bit indicates that a K3 byte change interrupt has occurred.
0	x	ISFInt[2]	This bit indicates that an ISF interrupt has occurred.

NOTE(S):
(1) Single event interrupt—only a positive transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.
(2) Dual event interrupt—either a positive or negative transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.

PNTRSTAT (Receive H1/H2 Pointer Action Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x096	0x296	0x496	0x696
Path 2	0x0D6	0x2D6	0x4D6	0x6D6
Path 3	0x116	0x316	0x516	0x716
Path 4	0x156	0x356	0x556	0x756

The PNTRSTAT register reports that the corresponding path event has occurred or is active.

Bit	Default	Name	Description
7	x	NDF[1]	This bit indicates that a pointer New Data Flag was received.
6	x	Incr[1]	This bit indicates that a pointer increment operation occurred.
5	x	Decr[1]	This bit indicates that a pointer decrement operation occurred.
4	x	NewPntr[1]	This bit indicates that a new pointer value w/o NDF was received.
3-2	xx	SS[1:0][2]	These bits indicate the value of the receive pointer SS bits.
1-0	xx	RxPntr[9:8][2]	These bits are the two MSBs of the receive pointer.

NOTE(S):
(1) This status shows an event that has occurred since the register was last read.
(2) This status reflects the current state of the circuit.

PORTINT (Summary Port Interrupt Indication Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x019	0x219	0x419	0x619

The PORTINT register reports that the respective section, line, path, or SI-Bus parity interrupt has occurred.

Bit	Default	Name	Description
7	x	SectionIntr	This bit indicates that a Section interrupt has occurred in this port.
6	x	LineIntr	This bit indicates that a Line interrupt has occurred in this port.
5	x	APSIntr	This bit indicates that an APS interrupt has occurred in this port.
4	x	Path1Intr	This bit indicates that a Path/Pointer 1 interrupt has occurred in this port.
3	x	Path2Intr	This bit indicates that a Path/Pointer 2 interrupt has occurred in this port.
2	x	Path3Intr	This bit indicates that a Path/Pointer 3 interrupt has occurred in this port.
1		Path4Intr	This bit indicates that a Path/Pointer 4 interrupt has occurred in this port.
0	x	SIParIntr	This bit indicates that a parity error occurred on the receive SI-Bus interface for this port.

PORTMAP (Port Mapping Control Register)

hex address: 0x001

The PORTMAP register controls the SI-Bus cross-connect mappings. These controls connect the respective SONET line side ports to the desired SI-Bus ports. Note that only one SONET port should be connected to each SI-Bus port for reliable operation. As this is a logical switch function, temporary connection of more than one SONET port to an SI-Bus port will not harm the part.

Bit	Default	Name	Description
7-6	11	Port4[1:0]	Determines the source/destination for STS-3 port 4. 00—STS-3 4 connects to SI-Bus interface 1 01—STS-3 4 connects to SI-Bus interface 2 10—STS-3 4 connects to SI-Bus interface 3 11—STS-3 4 connects to SI-Bus interface 4
5-4	10	Port3[1:0]	Determines the source/destination for STS-3 port 3. 00—STS-3 3 connects to SI-Bus interface 1 01—STS-3 3 connects to SI-Bus interface 2 10—STS-3 3 connects to SI-Bus interface 3 11—STS-3 3 connects to SI-Bus interface 4
3-2	01	Port2[1:0]	Determines the source/destination for STS-3 port 2. 00—STS-3 2 connects to SI-Bus interface 1 01—STS-3 2 connects to SI-Bus interface 2 10—STS-3 2 connects to SI-Bus interface 3 11—STS-3 2 connects to SI-Bus interface 4
1-0	00	Port1[1:0]	Determines the source/destination for STS-3 port 1. 00—STS-3 1 connects to SI-Bus interface 1 01—STS-3 1 connects to SI-Bus interface 2 10—STS-3 1 connects to SI-Bus interface 3 11—STS-3 1 connects to SI-Bus interface 4

PRBS (Pseudo-Random Bit Sequence Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x017	0x217	0x417	0x617

The PRBS register controls the transmit and receive PRBS generation/rececception.

Bit	Default	Name	Description
7-2	0		Reserved, set to zero.
1	0	EnTxPrbs	Enable the PRBS generator in the Transmit SONET/SDH framer.
0	0	EnRxPrbs	Enable the PRBS checker in the Receive SONET/SDH framer.

PROVC2 (Provisioned C2 Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x084	0x284	0x484	0x684
Path 2	0x0C4	0x2C4	0x4C4	0x6C4
Path 3	0x104	0x304	0x504	0x704
Path 4	0x144	0x344	0x544	0x744

The PROVC2 register sets the provisioned C2 value.

Bit	Default	Name	Description
7-0	01h	ProvC2[1:8]	Provisioned value for C2. This is the value compared to the received C2 value to determine PLM-P and UNEQ-P alarms.

PTHINSH (Path Overhead Insertion Control Register [High Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x083	0x283	0x483	0x683
Path 2	0x0C3	0x2C3	0x4C3	0x6C3
Path 3	0x103	0x303	0x503	0x703
Path 4	0x143	0x343	0x543	0x743

The PTHINSH register controls the Transmit Path Overhead octets.

Bit	Default	Name	Description
7-6	00	InsN1hi[1:0]	The N1 byte (high nibble) is generated as follows: 00—contains value from TXN1 bits 1–4 01—contains error count from incoming B3 byte for tandem conn. 10—contains value from SI-Bus 11—ISF value (1111) inserted in N1 high nibble and SPE conditioned.
5	0	InsN1lo	When written to 0, the N1 byte (low nibble) is the value from TXN1 bits 5–8. When written to 1, the N1 byte (low nibble) is accepted from the SI-Bus.
4	0	—	Reserved, set to zero.
3	0	InsB3Err[1]	When written to 1, this bit causes the B3 BIP calculation to be XORed with the value in the ERRPAT register for one transmit frame.
2	0	InsREI-P[1]	When written to 1, this bit causes the contents of ERRPAT bits 7–4 to be transmitted as the REI-P value in the G1 byte for one transmit frame.
1-0	00	—	Reserved, set to zero.

NOTE(S):
(1) Internal circuitry clears these control bits after the indicated error insertion has taken place.

PTHINSL (Path Overhead Insertion Control Register [Low Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x082	0x282	0x482	0x682
Path 2	0x0C2	0x2C2	0x4C2	0x6C2
Path 3	0x102	0x302	0x502	0x702
Path 4	0x142	0x342	0x542	0x742

The PTHINSL register controls the source of the transmit Path Overhead octets.

Bit	Default	Name	Description
7	0	InsJ1	When written to 0, the J1 byte is generated in the CX29610. When written to 1, the J1 byte is accepted from the SI-Bus.
6	0	InsB3	When written to 0, the B3 byte is generated in the CX29610. When written to 1, the B3 byte is accepted from the SI-Bus.
5	1	InsC2	When written to 0, the C2 byte is generated in the CX29610. When written to 1, the C2 byte is accepted from the SI-Bus.
4	0	InsG1	When written to 0, the G1 byte is generated in the CX29610. When written to 1, the G1 byte is accepted from the SI-Bus.
3	0	InsF2	When written to 0, the F2 byte is generated in the CX29610. When written to 1, the F2 byte is accepted from the SI-Bus.
2	1	InsH4	When written to 0, the H4 byte is generated in the CX29610. When written to 1, the H4 byte is accepted from the SI-Bus.
1	0	InsF3	When written to 0, the F3 byte is generated in the CX29610. When written to 1, the F3 byte is accepted from the SI-Bus.
0	0	InsK3	When written to 0, the K3 byte is generated in the CX29610. When written to 1, the K3 byte is accepted from the SI-Bus.

PTHINT (Receive Path Interrupt Indication Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x090	0x290	0x490	0x690
Path 2	0x0D0	0x2D0	0x4D0	0x6D0
Path 3	0x110	0x310	0x510	0x710
Path 4	0x150	0x350	0x550	0x750

The PTHINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	LOP- Pint[2]	This bit indicates that an LOP-P interrupt has occurred.
6	x	AIS-Pint[2]	This bit indicates that an AIS-P interrupt has occurred.
5	x	RDI-Pint[2]	This bit indicates that an RDI-P interrupt has occurred.
4	x	B3ErrInt[1]	This bit indicates that a Path BIP Error interrupt has occurred.
3	x	REI-Pint[1]	This bit indicates that an REI-P interrupt has occurred.
2	x	PLM-Pint[2]	This bit indicates that a PLM-P interrupt has occurred.
1	x	Uneq-Pint[2]	This bit indicates that an Uneq-P interrupt has occurred.
0	x	PthTraceInt[1]	This bit indicates that a Path Trace interrupt has occurred.

NOTE(S):
(1) Single event interrupt—only a positive transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.
(2) Dual event interrupt—either a positive or negative transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.

PWRDWN (PowerDown/Three-State Control Register)

The PWRDWN register controls the powerdown of ports and SI-Bus three-stating.

hex address: 0x003

Bit	Default	Name	Description
7	0	BusTri3	When written to 0, SI-Bus interface 3 is operational. When written to 1, SI-Bus interface 3 is three-stated.
6	0	BusTri2	When written to 0, SI-Bus interface 2 is operational. When written to 1, SI-Bus interface 2 is three-stated.
5	0	BusTri1	When written to 0, SI-Bus interface 1 is operational. When written to 1, SI-Bus interface 1 is three-stated.
4	0	BusTri0	When written to 0, SI-Bus interface 0 is operational. When written to 1, SI-Bus interface 0 is three-stated.
3	1	PowerDown4	When written to 1, Port 4 is placed into a power-down mode.
2	1	PowerDown3	When written to 1, Port 3 is placed into a power-down mode.
1	1	PowerDown2	When written to 1, Port 2 is placed into a power-down mode.
0	0	PowerDown1	When written to 1, Port 1 is placed into a power-down mode.

RLCNTH (REI-L Error Counter [High Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x056	0x256	0x456	0x656

High byte of the Line REI error counter.

Bit	Default	Name	Description
7-4	—	—	Reserved, set to zero.
3-0	xxh	RLCnt[19:16]	REI-L error counter high byte.

RLCNTM (REI-L Error Counter [Mid Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x055	0x255	0x455	0x655

Mid byte of the Line REI error counter.

Bit	Default	Name	Description
7-0	xxh	RLCnt[15:8]	REI-L error counter mid byte.

RLCNTL (REI-L Error Counter [Low Byte])

hex address:

Port 1	Port 2	Port 3	Port 4
0x054	0x254	0x454	0x654

Low byte of the Line REI error counter.

Bit	Default	Name	Description
7-0	xxh	RLCnt[7:0]	REI-L error counter low byte.

RPCNTH (REI-P Error Counter [High Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A3	0x2A3	0x4A3	0x6A3
Path 2	0x0E3	0x2E3	0x4E3	0x6E3
Path 3	0x123	0x323	0x523	0x723
Path 4	0x163	0x363	0x563	0x763

High byte of the Path REI error counter.

Bit	Default	Name	Description
7-0	xxh	RPCnt[15:8]	REI-P error counter high byte.

RPCNTL (REI-P Error Counter [Low Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A2	0x2A2	0x4A2	0x6A2
Path 2	0x0E2	0x2E2	0x4E2	0x6E2
Path 3	0x122	0x322	0x522	0x722
Path 4	0x162	0x362	0x562	0x762

Low byte of the Path REI error counter.

Bit	Default	Name	Description
7-0	xxh	RPCnt[7:0]	REI-P error counter low byte.

RXAPS (Receive APS Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x046	0x246	0x44A	0x64A

The RXAPS register contains status information for the receiver APS functions.

Bit	Default	Name	Description
7-3	00000	—	Reserved, set to zero.
2	x	PSBF[1]	This bit indicates a Protection Switch Byte Failure.
1	x	SigFail[1]	This bit indicates a Signal Fail condition.
0	x	SigDegrade[1]	This bit indicates a Signal Degrade condition.
(1) This status reflects the current state of the circuit.			

RXC2 (Receive C2 Path Overhead Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x098	0x298	0x498	0x698
Path 2	0x0D8	0x2D8	0x4D8	0x6D8
Path 3	0x118	0x318	0x518	0x718
Path 4	0x158	0x358	0x558	0x758

The RXC2 register contains the recevied C2 Path Overhead byte. This byte identifies the construction and content of the STS-level SPE, and STS Path Defect Indication (PDI-P). PDI-P indicates to downstream equipment that there is a payload defect.

Bit	Default	Name	Description
7-0	xx	RxC2[1:8]	Receive value for the C2 Path Overhead byte.

RXF1 (Receive F1 Section Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x02D	0x22D	0x42D	0x62D

The RXF1 register contains the received F1 Section Overhead byte. An F1INT in the SECINT is reported when this byte changes, if enabled. No integration is performed on this byte, so any change in the received by is reflected here.

Bit	Default	Name	Description
7-0	xxh	RxF1[1:8]	Receive value for the F1 Section Overhead byte.

RXF2 (Receive F2 Path Overhead Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x099	0x299	0x499	0x699
Path 2	0x0D9	0x2D9	0x4D9	0x6D9
Path 3	0x119	0x319	0x519	0x719
Path 4	0x159	0x359	0x559	0x759

The RXF2 register contains the received F2 Path Overhead byte. An F2INT in the PNTRINT is reported when this byte changes, if enabled. No integration is performed on this byte, so any change in the received by is reflected here.

Bit	Default	Name	Description
7-0	xx	RxF2[1:8]	Receive value for the F2 Path Overhead byte.

RXF3 (Receive Z3/F3 Path Overhead Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x09A	0x29A	0x49A	0x69A
Path 2	0x0DA	0x2DA	0x4DA	0x6DA
Path 3	0x11A	0x31A	0x51A	0x71A
Path 4	0x15A	0x35A	0x55A	0x75A

The RXF3 register contains the received Z3/F3 Path Overhead byte. An F3INT in the PNTRINT is reported when this byte changes, if enabled. No integration is performed on this byte, so any change in the received by is reflected here.

Bit	Default	Name	Description
7-0	xx	RxF3[1:8]	Receive value for the Z3/F3 Path Overhead byte.

RXFRMREF (Receive Frame Reference Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x020	0x220	0x420	0x620

The RXFRMREF register controls the receive rx8khz_n clock outputs.

Bit	Default	Name	Description
7	0	RXFRMLOL_DIS	Prevents a LOL event from disabling the 8 kHz clock output.
6	0	RXFRMLOS_DIS	Prevents a LOS event from disabling the 8 kHz clock output.
5	0	RXFRMSEF_DIS	Prevents a SEF event from disabling the 8 kHz clock output.
4	0	RXFRMLOF_DIS	Prevents a LOF event from disabling the 8 kHz clock output.
3	0	RXFRMAISL_DIS	Prevents a AIS-L event from disabling the 8 kHz clock output.
2	0	RXFRMREF_DIS	Disables the rx8kz clock output.
1-0	00	RXFRMREF_SEL[1:0]	Selects the mode of the rx8khz clock operation: 00—Switched 8 kHz output from the CDR. The clock will be disabled to a low level when one of the register controlled events occur as selected by bits [7-2] of this register. 01—8 kHz receive frame reference output. 10—19.44 MHz clock output from the CDR. 11—8 kHz output from CDR

RXK1 (Receive K1 Line Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x02E	0x22E	0x42E	0x62E

The RXK1 register contains the received K1 Line Overhead byte. The K1 and K2 bytes are allocated for APS signaling between line level entities. These bytes are defined only for the first STS-1 of the STS-3/STS-12 signal.

Bit	Default	Name	Description
7-0	xxh	RxK1[1:8]	Receive value for the K1 Line Overhead byte.

RXK2 (Receive K2 Line Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x02F	0x22F	0x42F	0x62F

The RXK2 register contains the received K2 Line Overhead byte. The K1 byte and bits 0–5 of the K2 byte are allocated for APS signaling between line level entities. Bits 6-8 of the K2 byte indicate bidirectional or unidirectional APS. Bits 6-8 are also used to indicate Line AIS and RDI conditions. These bytes are defined only for the first STS-1 of the STS-3/STS-12 signal.

Bit	Default	Name	Description
7-0	xx	RxK2[1:8]	Receive value for the K2 Line Overhead byte.

RXK3 (Receive Z4/K3 Path Overhead Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x09B	0x29B	0x49B	0x69B
Path 2	0x0DB	0x2DB	0x4DB	0x6DB
Path 3	0x11B	0x31B	0x51B	0x71B
Path 4	0x15B	0x35B	0x55B	0x75B

The RXK3 register contains the received Z4/K3 Path Overhead byte.

Bit	Default	Name	Description
7-0	00h	RxK3[1:8]	Receive value for the Z4/K3 Path Overhead byte.

RXLIN (Receive Line Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x045	0x245	0x449	0x649

The RXLIN register contains status information for the receive Line Overhead.

Bit	Default	Name	Description
7	0	—	Reserved, set to zero.
6	x	AIS-L[2]	This bit indicates that an AIS-L condition exists.
5	x	RDI-L[2]	This bit indicates that an RDI-L condition exists.
4	x	B2Err[1]	This bit indicates that a Line BIP Error was received.
3	x	REI-L[1]	This bit indicates that an REI-L condition was received.
2	0	—	Reserved, set to zero.
1	x	S1_Unstable[2]	This bit indicates that an S1 Unstable condition exists.
0	x	PrbsErr	This bit indicates that a PRBS error was received.

NOTE(S):
(1) This status shows an event that has occurred since the register was last read.
(2) This status reflects the current state of the circuit.

RXN1 (Receive Z5/N1 Path Overhead Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x09C	0x29C	0x49C	0x69C
Path 2	0x0DC	0x2DC	0x4DC	0x6DC
Path 3	0x11C	0x31C	0x51C	0x71C
Path 4	0x15C	0x35C	0x55C	0x75C

The RXN1 register holds the received Z5/N1 Path Overhead byte.

Bit	Default	Name	Description
7-0	xx	RxN1[1:8]	Receive value for the Z5/N1 Path Overhead byte.

RXPNTR (Receive H2 Pointer Value Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x095	0x295	0x495	0x695
Path 2	0x0D5	0x2D5	0x4D5	0x6D5
Path 3	0x115	0x315	0x515	0x715
Path 4	0x155	0x355	0x555	0x755

The RXPNTR register contains the received H2 Line Overhead pointer byte. The PNTRSTAT register contains the upper two bits of the ten bit pointer value.

Bit	Default	Name	Description
7-0	xxh	RxPntr[7:0][1]	Receive value for the H2 Line Overhead pointer byte.
(1) This status reflects the current state of the circuit.			

RXPTH (Receive Path Overhead Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x094	0x294	0x494	0x694
Path 2	0x0D4	0x2D4	0x4D4	0x6D4
Path 3	0x114	0x314	0x514	0x714
Path 4	0x154	0x354	0x554	0x754

The RXPTH register contains status information for the receiver Path Overhead.

Bit	Default	Name	Description
7	x	LOP-P[2]	This bit indicates that an LOP-P condition exists.
6	x	AIS-P[2]	This bit indicates that an AIS-P condition exists.
5	x	RDI-P[2]	This bit indicates that an RDI-P condition exists.
4	x	B3Err[1]	This bit indicates that a Path BIP Error was received.
3	x	REI-P[1]	This bit indicates that an REI-P condition was received.
2	x	PLM-P[2]	This bit indicates that a PLM-P condition exists.
1	x	Uneq-P[2]	This bit indicates that an Uneq-P condition exists.
0	0	—	Reserved, set to zero.

NOTE(S):
(1) This status shows an event that has occurred since the register was last read.
(2) This status reflects the current state of the circuit.

RXPTHBUF (Receive Path Trace Circular Buffer)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0B0	0x2B0	0x4B0	0x6B0
Path 2	0x0F0	0x2F0	0x4F0	0x6F0
Path 3	0x130	0x330	0x530	0x730
Path 4	0x170	0x370	0x570	0x770

The RXSECBUF buffer is used to repeatedly receive a 64-byte, fixed-length string so a receiving terminal in a path can verify its continued connection to the intended transmitter.

Bit	Default	Name	Description
7-0	xxh	RxPthBuf[7:0]	Receive path trace circular buffer.

RXRDI (Receive RDI-P Status Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x09D	0x29D	0x49D	0x69D
Path 2	0x0DD	0x2DD	0x4DD	0x6DD
Path 3	0x11D	0x31D	0x51D	0x71D
Path 4	0x15D	0x35D	0x55D	0x75D

The RXRDI register contains the received bits of the G1 octet.

Bit	Default	Name	Description
7-4	0000	—	Reserved, set to zero.
3-1	xxx	RxG1[5,6,7]	Receive value for G1 byte bits 5,6,7 in the path overhead.
0	0	—	Reserved, set to zero.

RXS1 (Receive S1 Line Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x030	0x230	0x430	0x630

The RXS1 register contains the received S1 Line Overhead byte. This byte is allocated for transporting synchronization status messages. This byte is defined only for the first STS-1 of the STS-3/STS-12 signal. These messages provide an indication of the quality level of the synchronization source of the SONET signal.

Bit	Default	Name	Description
7-0	xxh	RxS1[1:8]	Receive value for S1 overhead byte.

RXSEC (Receive Section Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x044	0x244	0x444	0x644

The RXSEC register provides section overhead status.

Bit	Default	Name	Description
7	x	SigDet[2]	This bit indicates that a Signal Detect condition exists.
6	x	LOL[2]	This bit indicates that a Loss of Lock condition exists.
5	x	LOS[2]	This bit indicates that a Loss of Signal condition exists.
4	x	SEF[2]	This bit indicates that an Out of Frame condition exists.
3	x	LOF[2]	This bit indicates that a Loss of Frame condition exists.
2	x	B1Err[1]	This bit indicates that a Section BIP Error was received.
1	0	—	Reserved, set to zero.
0	0	—	Reserved, set to zero.

NOTE(S):
(1) This status shows an event that has occurred since the register was last read.
(2) This status reflects the current state of the circuit.

RXSECBUF (Receive Section Trace Circular Buffer)

hex address:

Port 1	Port 2	Port 3	Port 4
0x05C	0x25C	0x45C	0x65C

The RXSECBUF buffer, the J0 byte, is used to repeatedly receive a 64-byte, fixed-length string so a receiving terminal in a section can verify its continued connection to the intended transmitter. This buffer is also used as a section trace for SDH.

Bit	Default	Name	Description
7-0	xxh	RxSecBuf[7:0]	Receive section trace circular buffer.

RXZ1b (Receive Z1b Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x031	0x231	0x431	0x631

The RXZ1b register contains the first received Z1 octet.

Bit	Default	Name	Description
7-0	xxh	RxZ1b[1:8]	Receive value for the first Z1 overhead byte.

RXZ1c (Receive Z1c Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x032	0x232	0x432	0x632

The RXZ1c register contains the second received Z1 octet.

Bit	Default	Name	Description
7-0	xxh	RxZ1c[1:8]	Receive value for the second Z1 overhead byte.

RXZ2a (Receive Z2a Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x033	0x233	0x433	0x633

The RXZ2a register contains the first received Z2 octet.

Bit	Default	Name	Description
7-0	xxh	RxZ2a[1:8]	Receive value for the first Z2 overhead byte.

RXZ2b (Receive Z2b Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x034	0x234	0x434	0x634

The RXZ2b register contains the second received Z2 octet.

Bit	Default	Name	Description
7-0	xxh	RxZ2b[1:8]	Receive value for the second Z2 overhead byte.

RXZ2c (Receive Z2c Overhead Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x035	0x235	0x435	0x635

The RXZ2c register contains the third received Z2 octet.

Bit	Default	Name	Description
7-0	xxh	RxZ2c[1:8]	Receive value for the second Z2 overhead byte.

SECINT (Receive Section Interrupt Indication Status Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x03C	0x23C	0x43C	0x63C

The SECINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	SigDetInt[2]	This bit indicates that a Signal Detect interrupt has occurred.
6	x	LOLInt[2]	This bit indicates that a Loss of Lock interrupt has occurred.
5	x	LOSInt[2]	This bit indicates that a Loss of Signal interrupt has occurred.
4	x	SEFInt[2]	This bit indicates that an Out of Frame interrupt has occurred.
3	x	LOFInt[2]	This bit indicates that a Loss of Frame interrupt has occurred.
2	x	B1ErrInt[1]	This bit indicates that a Section BIP Error interrupt has occurred.
1	x	SecTraceInt[1]	This bit indicates that a Section Trace interrupt has occurred.
0	x	F1Int[1]	This bit indicates that an F1 byte change interrupt has occurred.

NOTE(S):
(1) Single event interrupt—only a positive transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.
(2) Dual event interrupt—either a positive or negative transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.

SEFCNT (Out of Frame Event Counter)

hex address:

Port 1	Port 2	Port 3	Port 4
0x048	0x248	0x448	0x648

The SEFCNT counter tracks the number of out of frame (SEF) events.

Bit	Default	Name	Description
7-0	xxh	SEFCnt[7:0]	Out of frame event counter.

STATUS (Status Output Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x011	0x211	0x411	0x611

The STATUS register controls the functionality of the StatOut pins.

Bit	Default	Name	Description
7	0	—	Reserved, set to zero.
6	0	StatPinMode	When written to 0, the StatOut[1:0] pins for this port reflect the internal status selected in bits 5–2 of this register. When written to 1, the StatOut[1:0] pins for this port reflect the values from bits 1–0 of this register.
5-4	00	Stat0Sel[1:0]	00—Loss of Lock 01—OR function of LOS, LOF, AIS-L is output on StatOut[1] 10—SigFail 11—SigDegrade
3-2	00	Stat1Sel[1:0]	00—Path 1 LOP-P, AIS-P, UNEQ-P, or PLM-P is output on StatOut[0] 01—Path 2 LOP-P, AIS-P, UNEQ-P, or PLM-P is output on StatOut[0] 10—Path 3 LOP-P, AIS-P, UNEQ-P, or PLM-P is output on StatOut[0] 11—Path 4 LOP-P, AIS-P, UNEQ-P, or PLM-P is output on StatOut[0]
1-0	00	StatOut[1:0]	Output value for StatOut[1:0] pins when bit 6 is set to 1.

SUMINT (Summary Interrupt Indication Register)

hex address: 0x005

The SUMINT register indicates data link interrupts, one-second interrupts, and additional summary interrupts.

Bit	Default	Name	Description
7-6	00	—	Reserved, set to zero.
5	x	PLLRefInt	PLL Reference has occurred.
4	x	OneSecInt[1]	This bit indicates that a one-second interrupt has occurred.
3	x	Port4Int	This bit indicates that an interrupt has occurred in a Port 4 interrupt register.
2	x	Port3Int	This bit indicates that an interrupt has occurred in a Port 3 interrupt register.
1	x	Port2Int	This bit indicates that an interrupt has occurred in a Port 2 interrupt register.
0	x	Port1Int	This bit indicates that an interrupt has occurred in a Port 1 interrupt register.

(1) Reading this register clears the interrupt indication.

TESTMODE (Test Mode Control Register)

hex address: 0x007

The TESTMODE register controls various circuits of the device. The most important one is the Speed_CP bit which controls the receive CDR charge pump frequency. This bit must be set to the correct mode for proper device operation.

Bit	Default	Name	Description
7	1	Speed_CP	CDR charge pump frequency select 0—155 (250 μA). Set to 0 for 4xOC-3 mode. 1—622 (1 mA). Set to 1 for 1xOC-12 mode.
6	0	Pd_TxSyn	When written to 1, powerdown transmit synthesizer.
5	0	RxLosAllOnes	When written to 1, LOS is genererated when 100us of all ones is received.
4	0	SONET_Bypass	Bypasses the SONET transmission/reception used to debug and test the CDR block.
3	0	LDCC_loopback_mode	Line DCC internal reception-to-transmission loopback.
2	0	SDCC_Loopback_mode	Section DCC internal reception-to-transmission loopback.
1	0	E1E2_Loopback_mode	E1 and E2 orderwire internal transmission-to-reception loopback.
0	0	—	Reserved

TCCNTH (Tandem Connection Error Counter [High Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A5	0x2A5	0x4A5	0x6A5
Path 2	0x0E5	0x2E5	0x4E5	0x6E5
Path 3	0x125	0x325	0x525	0x725
Path 4	0x165	0x365	0x565	0x765

The TCCNTH counter counts tandem connection errors.

Bit	Default	Name	Description
7-0	xxh	TCCnt[15:8]	Tandem connection error counter high byte.

TCCNTL (Tandem Connection Error Counter [Low Byte])

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0A4	0x2A4	0x4A4	0x6A4
Path 2	0x0E4	0x2E4	0x4E4	0x6E4
Path 3	0x124	0x324	0x524	0x724
Path 4	0x164	0x364	0x564	0x764

The TCCNTL counter counts tandem connection errors.

Bit	Default	Name	Description
7-0	xxh	TCCnt[7:0]	Tandem connection error counter low byte.

TXC2 (Transmit C2 Path Overhead Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x085	0x285	0x485	0x685
Path 2	0x0C5	0x2C5	0x4C5	0x6C5
Path 3	0x105	0x305	0x505	0x705
Path 4	0x145	0x345	0x545	0x745

The TXC2 register holds the value of the C2 Path overhead byte that is inserted into the transmit frame. This byte is allocated to identify the construction and content of the STS-level SPE.

Bit	Default	Name	Description
7-0	01h	TxC2[1:8]	Transmit value for C2 overhead byte.

TXF1 (Transmit F1 Section Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x024	0x224	0x424	0x624

The TXF1 register holds the value of the F1 Section overhead byte that is inserted into the transmit frame.

Bit	Default	Name	Description
7-0	00h	TxF1[1:8]	Transmit value for F1 section overhead byte.

TXF2 (Transmit F2 Path Overhead Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x086	0x286	0x486	0x686
Path 2	0x0C6	0x2C6	0x4C6	0x6C6
Path 3	0x106	0x306	0x506	0x706
Path 4	0x146	0x346	0x546	0x746

The TXF2 register holds the value of the F2 path overhead byte that is inserted into the transmit frame. Insertion of the F2 path overhead byte is controlled by the PTHINSL control register bit 3.

Bit	Default	Name	Description
7-0	00h	TxF2[1:8]	Transmit value for F2 path overhead byte.

TXF3 (Transmit Z3/F3 Path Overhead Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x087	0x287	0x467	0x667
Path 2	0x0C7	0x2C7	0x4C7	0x6C7
Path 3	0x107	0x307	0x507	0x707
Path 4	0x147	0x347	0x547	0x747

The TXF3 register holds the value of the Z3/F3 path overhead byte that is inserted into the transmit frame. Insertion of the Z3/F3 path overhead byte is controlled by the PTHINSL control register bit 1.

Bit	Default	Name	Description
7-0	00h	TxF3[1:8]	Transmit value for F3 path overhead byte.

TXK1 (Transmit K1 Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x025	0x225	0x425	0x625

The TXK1 register controls the K1 byte in the transport overhead. The K1 and K2 bytes are allocated for APS signaling between line level entities. These bytes are defined only for the first STS-1 of the STS-3c signal.

Bit	Default	Name	Description
7-0	00h	TxK1[1:8]	Transmit value for K1 overhead byte.

TXK2 (Transmit K2 Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x026	0x226	0x426	0x626

The TXK2 register controls the K2 byte in the transport overhead. The K1 byte and bits 0–5 of the K2 byte are allocated for APS signaling between line level entities. These bytes are defined only for the first STS-1 of the STS-3c signal.

Bits 6–8 of the K2 byte are allocated for AIS and RDI. These bytes are defined only for the first STS-1 of the STS-3c signal.

Bit	Default	Name	Description
7-0	00h	TxK2[1:8]	Transmit value for K2 overhead byte.

TXK3 (Transmit K3 Overhead Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x088	0x288	0x468	0x668
Path 2	0x0C8	0x2C8	0x4C8	0x6C8
Path 3	0x108	0x308	0x508	0x708
Path 4	0x148	0x348	0x548	0x748

The TXK3 register controls the insertion of the K3 Path overhead byte position in the transmitter if enabled by setting PTHINSL bit 0 low.

Bit	Default	Name	Description
7-0	00h	TxK3[1:8]	Transmit value for K3 overhead byte.

TXLIN (Transmit Line Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x01D	0x21D	0x41D	0x61D

The TXLIN register controls the transmission of various octets in the Line Overhead of the SONET frame.

Bit	Default	Name	Description
7	0	EnTxLinDCC	When written to 1, the transmit line DCC is enabled for insertion from the source selected by bit 6. When written to 0, the D4–12 bytes contain 00h.
6	0	LinDCCSrc	When written to 0, the source for the line DCC is the serial interface. When written to 1, the source for the line DCC is the SI-Bus interface.
5	0	EnE2	When written to 1, the E2 byte is generated from data shifted in the TxE2 input pin. When written to 0, the E2 byte contains 00h.
4	0	DisB2	When written to 1, the B2 bytes contain 00h. When written to 0, the B2 bytes contain the calculated result for line BIP.
3	0	InsAIS-L	When written to 1, AIS-L is generated.
2	0	InsRDI-L	When written to 1, RDI-L is generated.
1	1	AutoRDI-L	When written to 1, automatic generation of RDI-L is enabled.
0	1	AutoREI-L	When written to 1, automatic generation of REI-L codes are generated.

TXN1 (Transmit N1 Overhead Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x089	0x289	0x469	0x669
Path 2	0x0C9	0x2C9	0x4C9	0x6C9
Path 3	0x109	0x309	0x509	0x709
Path 4	0x149	0x349	0x549	0x749

The TXN1 register controls the insertion of the N1 Path overhead byte position in the transmitter. Separate nibbles of this byte can be overridden by setting the control bits in the PTHINSH register.

Bit	Default	Name	Description
7-0	00h	TxN1[1:8]	Transmit value for N1 overhead byte.

TXPNTR (Transmit H1/H2/H3 Pointer Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x080	0x280	0x480	0x680
Path 2	0x0C0	0x2C0	0x4C0	0x6C0
Path 3	0x100	0x300	0x500	0x700
Path 4	0x140	0x340	0x540	0x740

The TXPNTR register controls the pointer value for the transmitted SPE. SONET STS-3 modes will have three SPEs, represented by path registers 1-3. The SONET OC-12 and SDH STM-4 AU-3 modes will use one physical line port (port 1) but have twelve SPEs. The twelve paths are controlled by path registers 1-3 and port registers 1-4. The SDH AU-4 mode can support a TUG-3 to TUG-2 mapping or TUG-3 to TU-3 mapping. In both cases, the AU-4 pointer is controlled by the path 1 registers. If the TU-3 mode is enabled, paths 2-4 control TU-3 pointers 1-3 respectively. See Figures 2-10 through 2-16.

Bit	Default	Name	Description
7-6	00	SSbits	These bits are placed in bits 5 and 6 of the H1 pointer byte to accommodate SDH. These bits should be set to 10 for the AU-4, AU-3 and TU-3 pointers as stated by ITU G.707.
5	0	DisPntr	When written to 1, the H1/H2 pointer bytes are both forced to 33h to simulate an invalid pointer value.
4	0	AU4Pntr	When written to 1, the H1/H2 pointer bytes for this path will contain the concatenation value of 93FFh. For SDH AU-4 modes, this bit must be set for each AU-4 path.
3-0	0000	—	Reserved, set to zero.

TXPTH (Transmit Path Overhead Control Register)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x081	0x281	0x481	0x681
Path 2	0x0C1	0x2C1	0x4C1	0x6C1
Path 3	0x101	0x301	0x501	0x701
Path 4	0x141	0x341	0x541	0x741

The TXPTH register controls the transmission of various octets in the Path Overhead of the SONET frame.

Bit	Default	Name	Description
7	0	EnPthTr	When written to 0, the J1 byte contains 00h. When written to 1, the Path Trace Message from the TXPTHBUF circular buffer is inserted in the J1 byte.
6	0	DisB3	When written to 0, the B3 byte contains the results of the path BIP calculation. When written to 1, the B3 byte contains 00h.
5	1	AutoREI-P	When written to 1, path REI codes are automatically inserted in the G1 byte upon reception of B3 errors. When written to 0, automatic insertion is disabled.
4	0	InsAIS-P	When written to 0, Path AIS is not generated. When written to 1, Path AIS alarm is generated.
3	0	TxRDI[5]	This bit is mapped to Transmit RDI bit 5 in the G1 byte.
2	0	TxRDI[6]	This bit is mapped to Transmit RDI bit 6 in the G1 byte.
1	1	TxRDI[7]	This bit is mapped to Transmit RDI bit 7 in the G1 byte.
0	1	AutoRDI-P	When written to 1, path RDI is automatically generated for at least 20 frames upon reception of LOS, LOF, LOP, AIS-L, AIS-P, UNEQ-P, or PLM-P. When written to 0, path RDI is inserted from bits 3–1 of this register.

TXPTHBUF (Transmit Path Trace Circular Buffer)

hex address:

	Port 1	Port 2	Port 3	Port 4
Path 1	0x0AC	0x2AC	0x4AC	0x6AC
Path 2	0x0EC	0x2EC	0x4EC	0x6EC
Path 3	0x12C	0x32C	0x52C	0x72C
Path 4	0x16C	0x36C	0x56C	0x76C

The TXPTHBUF buffer, the J1 byte, is used to repeatedly transmit a 64-byte, fixed-length string so a receiving terminal in a path can verify its continued connection to the intended transmitter. The 64-byte J1 transmit buffers are implemented with a 16-bit wide internal buffer, **therefore two writes to the TXPTHBUF register must be executed before the entire 16-bits is written to the internal buffer**.

Bit	Default	Name	Description
7-0	xxh	TxPthBuf[7:0]	Transmit path trace circular buffer.

TXS1 (Transmit S1 Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x027	0x227	0x427	0x627

The TXS1 register controls the S1 byte in the transport overhead. This byte transports synchronization status messages and is defined only for the first STS-1 of the STS-3c signal. These messages provide an indication of the quality level of the synchronization source of the SONET signal.

Bit	Default	Name	Description
7-0	00h	TxS1[1:8]	Transmit value for S1 overhead byte.

TXSEC (Transmit Section Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x01C	0x21C	0x41C	0x61C

The TXSEC register controls transmission of various octets in the Section Overhead of the SONET frame.

Bit	Default	Name	Description
7	0	DisTxScr	When written to 1, the transmit frame scrambler is disabled.
6	0	EnTxSecDCC	When written to 1, the transmit section DCC is enabled for insertion from the source selected by bit 5. When written to 0, the D1/D2/D3 bytes contain 00h.
5	0	SecDCCSrc	When written to 0, the source for the section DCC is the serial interface. When written to 1, the source for the section DCC is the SI-Bus interface.
4	0	EnSecTr	When written to 1, the section trace message from the circular buffer is enabled. When written to 0, the J0 byte contains 01h.
3	0	DisA1A2	When written to 1, the A1/A2 bytes are forced to 00h. When written to 0, the A1/A2 bytes contain their default values (F6/28).
2	0	DisB1	When written to 1, the B1 byte contains 00h. When written to 0, the B1 byte contains the calculated result for section BIP.
1	0	InsAllZer	When written to 1, all zeros data is inserted after the transmit frame scrambler.
0	0	EnE1	When written to 1, the E1 byte is generated from data shifted in the TxE1 input pin. When written to 0, the E1 byte contains 00h.

TXSECBUF (Transmit Section Trace Circular Buffer)

hex address:

Port 1	Port 2	Port 3	Port 4
0x058	0x258	0x458	0x658

The TXSECBUF buffer, the J0 byte, is used to repeatedly transmit a 64-byte, fixed-length string so a receiving terminal in a section can verify its continued connection to the intended transmitter. The 64-byte J0 transmit buffers are implemented with a 16-bit wide internal buffer, **therefore two writes to the TXSECBUF register must be executed before the entire 16-bits is written to the internal buffer**. This buffer is also used as a Section trace for SDH.

Bit	Default	Name	Description
7-0	xxh	TxSecBuf[7:0]	Transmit section trace circular buffer.

TXZ1b (Transmit Z1b Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x028	0x228	0x428	0x628

The TXZ1b register controls the insertion of the Z1 Line overhead byte position in the transmitter. Z1b is Z1-2 in STS-3 mode and Z1-5 through Z1-8 in STS-12 mode, presented in registers for ports 1–4, respectively.

Bit	Default	Name	Description
7-0	00h	TxZ1b[1:8]	Transmit value for the first Z1 overhead byte.

TXZ1c (Transmit Z1c Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x029	0x229	0x429	0x629

The TXZ1c register controls the insertion of the Z1 Line overhead byte position in the transmitter. Z1c is Z1-3 in STS-3 mode and Z1-9 through Z1-12 in STS-12 mode, presented in registers for ports 1–4, respectively.

Bit	Default	Name	Description
7-0	00h	TxZ1c[1:8]	Transmit value for the second Z1 overhead byte.

TXZ2a (Transmit Z2a Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x02A	0x22A	0x42A	0x62A

The TXZ2a register controls the insertion of the first Z2 Line overhead byte position in the transmitter. Z2a is Z2-1 in STS-3 mode and Z2-1 through Z2-4 in STS-12 mode, set in registers for ports 1–4, respectively. Note that in STS-12 mode, the value in the TXZ2a register for port 3 is overridden by the M1 value.

Bit	Default	Name	Description
7-0	00h	TxZ2a[1:8]	Transmit value for the first Z2 overhead byte.

TXZ2b (Transmit Z2b Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x02B	0x22B	0x42B	0x62B

The TXZ2b register controls the insertion of the second Z2 Line overhead byte position in the transmitter. Z2b is Z2-2 in STS-3 mode and Z2-5 through Z2-8 in STS-12 mode, set in registers for ports 1–4, respectively.

Bit	Default	Name	Description
7-0	00h	TxZ2b[1:8]	Transmit value for the second Z2 overhead byte.

TXZ2c (Transmit Z2c Overhead Control Register)

hex address:

Port 1	Port 2	Port 3	Port 4
0x02C	0x22C	0x42C	0x62C

The TXZ2c register controls the insertion of the third Z2 Line overhead byte position in the transmitter. This bit is not used in STS-3 mode as this is the M1 byte position. Z2-9 through Z2-12 in STS-12 mode, set in registers for ports 1–4, respectively.

Bit	Default	Name	Description
7-0	00h	TxZ2c[1:8]	Transmit value for the third Z2 overhead byte.

VERSION (Part Number/Version Register)

hex address: 0x006

The VERSION register is used to identify the Mindspeed device and its revision level.

Bit	Default	Name	Description
7–4	6	Part[3:0]	This is the part number that uniquely identifies the CX29610.
3-0	1	Ver[3:0]	This is the version number that uniquely identifies the specific version of the CX29610. Version numbers start at 1 for the first version and are incremented for each revision thereafter.

WINDOW_H (CDR Window Register [high byte])

hex address: 0x009

The WINDOW_H register control PLL lock and capture window settings of the CDR.

Bit	Default	Name	Description
7–0	0x03	—	Reserved.

WINDOW_L (CDR Window Register [low byte])

hex address: 0x008

The WINDOW_L register control PLL lock and capture window settings of the CDR.

Bit	Default	Name	Description
7–0	0xff	—	Window value to CDR PLL block, low byte.[1]
NOTE(S): (1) The value isn't written until after the WINDOW_H register value is written.			

WINHYST1_H (CDR Hysteresis Register [high byte])

hex address: 0x00B

The WINHYST1_H register controls the hysteresis value of the CDR.

Bit	Default	Name	Description
7–2	0x00	—	Reserved.
1-0	00	—	The first hysteresis value to CDR PLL block, high byte.

WINHYST1_L (CDR Hysteresis Register [low byte])

hex address: 0x00A

The WINHYST1_L register controls the hysteresis value of the CDR.

Bit	Default	Name	Description
7–0	0x2	—	The first hysteresis value to the CDR PLL block, low byte.[1]
NOTE(S): (1) The value is not written until after the WINHYST1_H register value is written.			

WINHYST2_H (CDR Hysteresis Register [high byte])

hex address: 0x00D

The WINHYST2_H register controls the hysteresis value of the CDR PLL.

Bit	Default	Name	Description
7–2	0x00	—	Reserved.
1-0	00	—	The second hysteresis value to CDR PLL block, high byte.

WINHYST2_L (CDR Hysteresis Register [low byte])

hex address: 0x00C

The WINHYST2_L register controls the hysteresis value of the CDR PLL.

Bit	Default	Name	Description
7–0	0x1	—	The second hysteresis value to the CDR PLL block, low byte.[1]
NOTE(S): (1) The value is not written until after the WINHYST2_H register value is written.			

4.2 Register Differences between STS-3 and STS-12 Modes

The preceding register map details the registers for 4xSTS-3 mode. Some registers take on different functionality in STS-12 mode than in STS-3 mode. STS-3 numbering remains the same in either mode as shown in Figure 1-4 and Figure 1-5.

- TXSEC register—in STS-12 mode, only bit 3 of TXSEC is active for ports 2–4.
- TXLIN register—in STS-12 mode, only bit 4 of TXLIN is active for ports 2–4. This bit controls only the B2 bytes that are associated with the corresponding STS-3.
- In STS-12 mode, the TXF1/RXF1, TXK1/RXK1, and TXK2/RXK2 registers are inactive for ports 2–4.
- In STS-12 mode, TXS1/RXS1 registers for ports 2–4 become TXZ1/RXZ1 registers for the corresponding STS-1 positions. There are no registers for the TXZ2/RXZ2 positions in STS-1 numbers 6, 9, and 12 in STS-12 mode (since these were formerly M1 bytes in 4xSTS-3 mode).
- In STS-12 mode, the B2 error insertion functions in the ERRINS registers for ports 2–4 map according to the following in order to match the SONET byte interleave structure:

Port 1	InsB2Err1 affects B2 byte 1
	InsB2Err2 affects B2 byte 5
	InsB2Err3 affects B2 byte 9
Port 2	InsB2Err1 affects B2 byte 2
	InsB2Err2 affects B2 byte 6
	InsB2Err3 affects B2 byte 10
Port 3	InsB2Err1 affects B2 byte 3
	InsB2Err2 affects B2 byte 7
	InsB2Err3 affects B2 byte 11
Port 4	InsB2Err1 affects B2 byte 4
	InsB2Err2 affects B2 byte 8
	InsB2Err3 affects B2 byte 11

- For the APS threshold registers, only port 1 is active in STS-12 mode. Other bits in the ERRINS register for ports 2–4 are inactive.

5.0 Electrical and Mechanical Specifications

This chapter describes the electrical and mechanical aspects of the CX29610. Included are timing diagrams, absolute maximum ratings, DC characteristics, and mechanical drawings.

5.1 Timing Specifications

This section provides timing diagrams and descriptions for the various interfaces of the CX29610. Table 5-1 describes the different types of timing relationships that appear in the timing diagrams. The timing relationship labels are numbered when they occur more than once in a diagram so that each label is unique. This aids in identifying the appropriate label in the timing table. Signals are measured at the 50% point of the changing edge except for those involving high impedance transitions which are measured at 10% and 90%.

The following specifications describe the conditions under which the timing specifications in this section are measured.

$3.135 \leq VDD = AVDD \leq 3.465$ V
$VDD \leq VGG \leq 5.5$ V
-40 °C ≤ Ambient Temperature ≤ +85 °C
@ 100 LFM(1)

NOTE(S):
(1) See footnote to Table 5-16 regarding airflow requirements for the device.

Table 5-1. Timing Diagram Nomenclature *(1 of 3)*

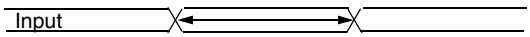
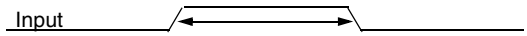
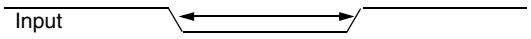
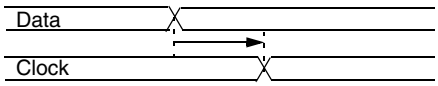
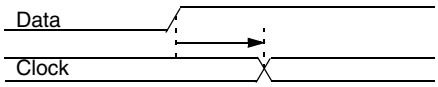
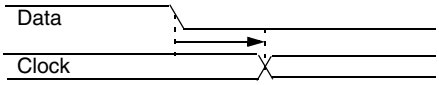
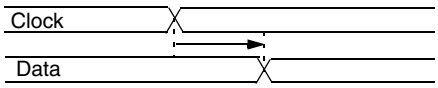
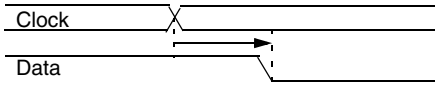
Symbol	Timing Relationship	Waveform
t_{pw}	Pulse Width	
t_{pwh}	Pulse Width High	
t_{pwl}	Pulse Width Low	
t_s	Setup Time	
t_{sh}	Setup High Time	
t_{sl}	Setup Low Time	
t_h	Hold Time	
t_{hh}	Hold High Time	

Table 5-1. Timing Diagram Nomenclature *(2 of 3)*

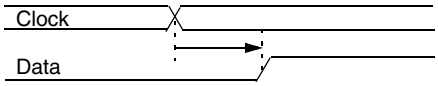
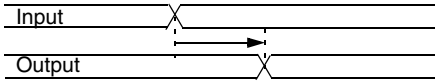
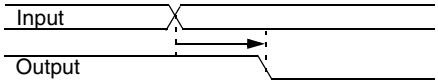
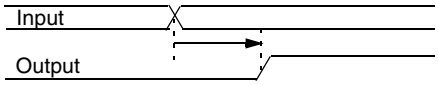
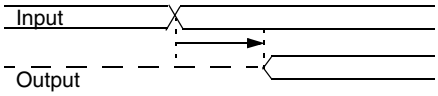
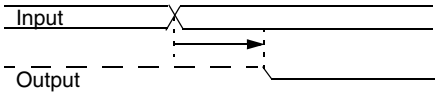
Symbol	Timing Relationship	Waveform
t_{hl}	Hold Low Time	
t_{pd}	Propagation Delay	
t_{pdhl}	Propagation Delay - High-to-Low	
t_{pdlh}	Propagation Delay - Low-to-High	
t_{en}	Enable Time	
t_{enzl}	Enable Time - High-impedance to Low Enable	

Table 5-1. Timing Diagram Nomenclature *(3 of 3)*

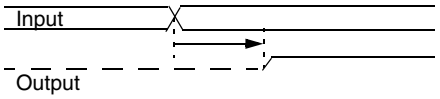
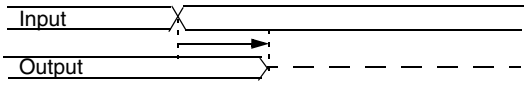
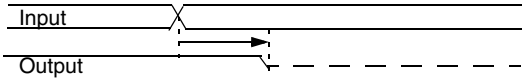
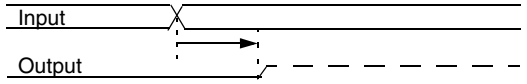
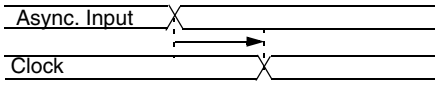
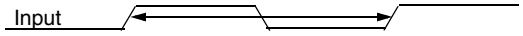
Symbol	Timing Relationship	Waveform
t_{enzh}	Enable Time - High-impedance to High Enable	
t_{dis}	Disable Time	
t_{dishz}	Disable Time - High Disable	
t_{dislz}	Disable Time - Low Disable	
t_{rec}	Recovery Time	
t_{per}	Period	

Figure 5-1 illustrates how input waveforms are defined and Figure 5-2 illustrates how output waveforms are defined.

Figure 5-1. Input Waveform

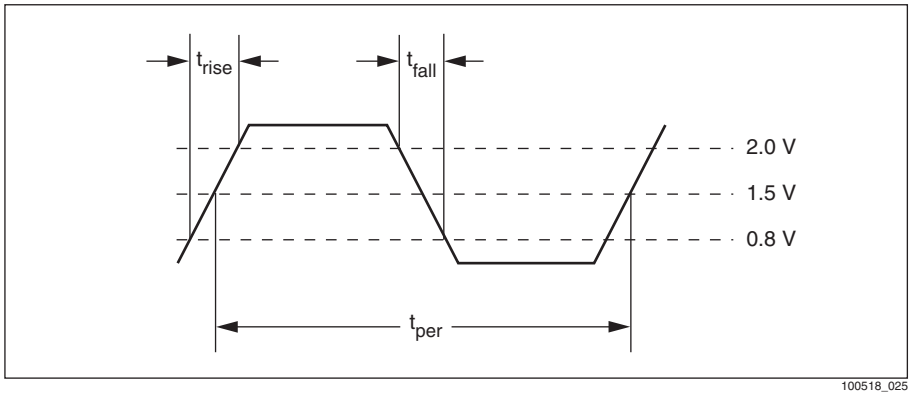
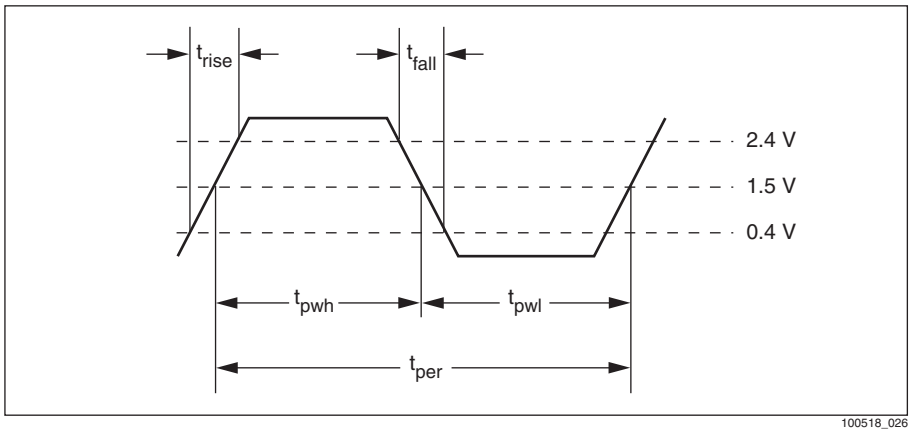


Figure 5-2. Output Waveform



5.1.1 Microprocessor Interface Timing

The tables and corresponding figures show the timing requirements and characteristics of the Motorola MPC860 Interface and the Mindspeed EBUS Interface.

5.1.1.1 Motorola MPC860 Interface

Figure 5-3. MPC 860 Read Timing Diagram

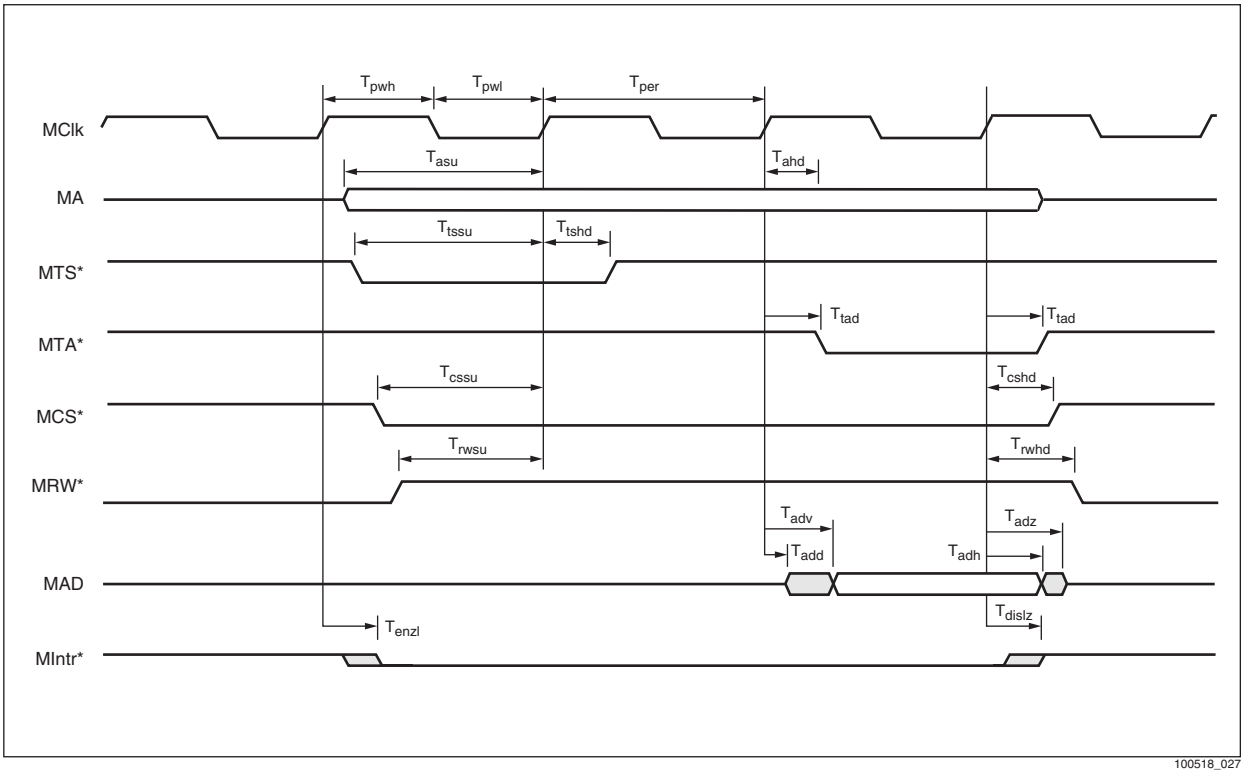


Table 5-2. MPC 860 Read Timing Table

Label	Description	Min	Max	Unit	Load
T_{pwh}	Pulse Width High, MClk	11	56	ns	—
T_{pwl}	Pulse Width Low, MClk	11	56	ns	—
T_{per}	Period, MClk	30	125	ns	—
T_{asu}	Address setup to clock rise	7.3	—	ns	—
T_{ahd}	Address hold to clock rise	3	—	ns	—
T_{tssu}	Transfer Start setup to clock rise	6	—	ns	—
T_{tshd}	Transfer Start hold to clock rise	3	—	ns	—
T_{tad}	Transfer Acknowledge delay	1	12	ns	30 pf

Table 5-2. MPC 860 Read Timing Table

Label	Description	Min	Max	Unit	Load
T_{cssu}	Chip Select setup to clock rise	6	—	ns	—
T_{cshd}	Chip Select hold to clock rise	3	—	ns	—
T_{rwsu}	Read/Write setup to clock rise	6	—	ns	—
T_{rwhd}	Read/Write hold to clock rise	3	—	ns	—
T_{add}	Data bus driven from clock rise	1	—	ns	30 pf
T_{adv}	Read data valid from clock rise	-	12	ns	30 pf
T_{adh}	Read data hold from clock rise	2	—	ns	30 pf
T_{adz}	Data bus float from clock rise	-	5	ns	30 pf
T_{enzl}	Enable, MIntr* from the rising edge of MClk	2	—	ns	30 pf
T_{dislz}	Disable, MIntr* from the rising edge of MClk	2	20	ns	30 pf

Figure 5-4. MPC 860 Write Timing Diagram

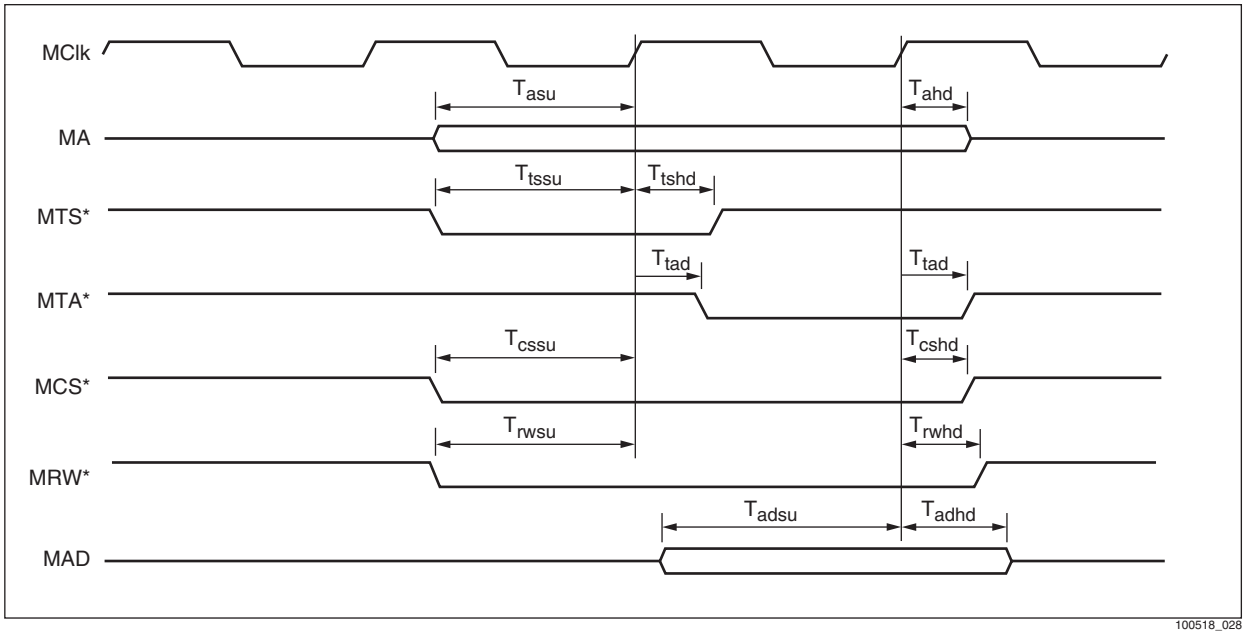
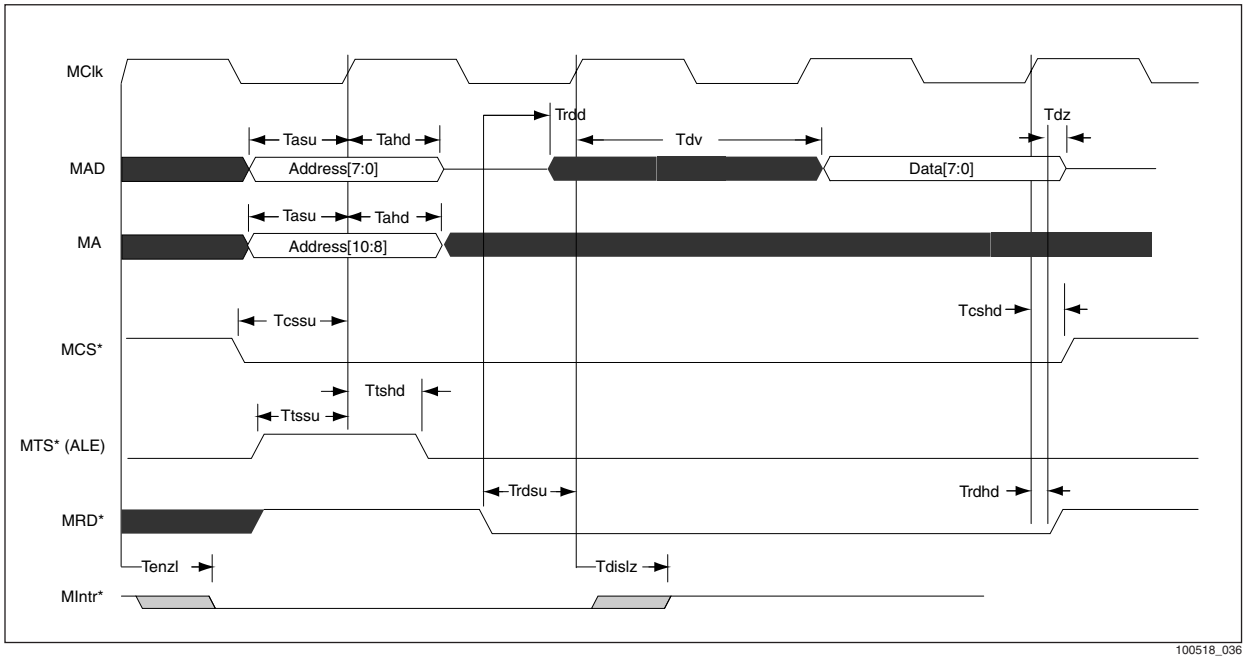


Table 5-3. MPC 860 Write Timing Table

Label	Description	Min	Max	Unit	Load
T_{asu}	Address setup to clock rise	6	—	ns	—
T_{ahd}	Address hold to clock rise	3	—	ns	—
T_{tssu}	Transfer Start setup to clock rise	6	—	ns	—
T_{tshd}	Transfer Start hold to clock rise	3	—	ns	—
T_{tad}	Transfer Acknowledge delay	1	12	ns	30 pF
T_{cssu}	Chip Select setup to clock rise	6	—	ns	—
T_{cshd}	Chip Select hold to clock rise	3	—	ns	—
T_{rwsu}	Read/Write setup to clock rise	6	—	ns	—
T_{rwhd}	Read/Write hold to clock rise	3	—	ns	—
T_{adsu}	Data (in) setup to clock rise	7	—	ns	—
T_{adhd}	Data (in) hold to clock rise	5	—	ns	—

5.1.1.2 Mindspeed EBUS Interface

Figure 5-5. EBUS Read Timing Diagram



NOTE: The chip select signal (MCS*) needs to go inactive for at least one cycle between accesses.

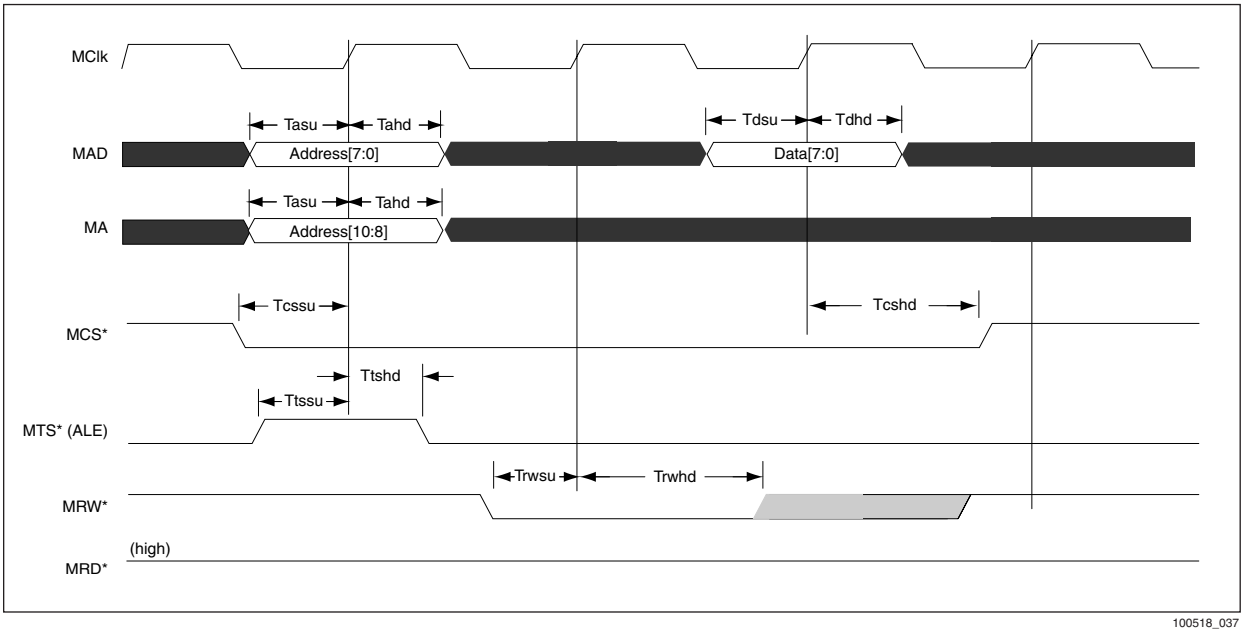
Table 5-4. EBUS Read Timing Table

Label	Description	Min	Max	Unit	Load
T_{pwh}	Pulse Width High, MClk	11	56	ns	—
T_{pwl}	Pulse Width Low, MClk	11	56	ns	—
T_{per}	Period, MClk	30	125	ns	—
T_{asu}	Address setup to clock rise	6	—	ns	—
T_{ahd}	Address hold to clock rise	3	—	ns	—
T_{cssu}	Chip Select setup to clock rise	6	—	ns	—
T_{cshd}	Chip Select hold to clock rise	3	—	ns	—
T_{tssu}	Transfer Start (ALE) setup to clock rise	6	—	ns	—
T_{tshd}	Transfer Start (ALE) hold to clock rise	3	—	ns	—
T_{rdsu}	MRD* setup to clock rise	6	—	ns	—

Table 5-4. EBUS Read Timing Table

Label	Description	Min	Max	Unit	Load
T_{rdhd}	MRD* hold to clock rise	3	—	ns	—
T_{rdd}	MRD* low to data bus driven	1	5	ns	30 pF
T_{dv}	MClk rise to data valid	3	10	ns	30 pF
T_{dz}	Data Strobe high to data bus float	1	5	ns	30 pF
T_{enzl}	Enable, MIntr* from the rising edge of MClk	2	10	ns	30 pF
T_{dislz}	Disable, MIntr* from the rising edge of MClk	2	7	ns	30 pF

Figure 5-6. EBUS Write Timing Diagram



NOTE: The chip select signal (MCS*) needs to go inactive for at least one cycle between accesses.

Table 5-5. EBUS Write Timing Table

Label	Description	Min	Max	Unit	Load
T_{asu}	Address setup to clock rise	6	—	ns	
T_{ahd}	Address hold to clock rise	3	—	ns	
T_{cssu}	Chip Select setup to clock rise	6	—	ns	
T_{cshd}	Chip Select hold to clock rise	3	—	ns	
T_{tssu}	Transfer Start (ALE) setup to clock rise	6	—	ns	
T_{tshd}	Transfer Start (ALE) hold to clock rise	3	—	ns	
T_{rwsu}	Write (MRW*) setup to clock rise	6	—	ns	
T_{rwhd}	Write (MRW*) hold to clock rise	3	—	ns	
T_{dsu}	Data (in) setup to clock rise	7	—	ns	
T_{dhd}	Data (in) hold to clock rise	5	—	ns	

5.1.2 SI-Bus Transmit Timing

The CX29610 generates clock and control signals and the slave devices respond with data/parity. The CX29610 generates control outputs synchronously with the rising edge of STxClk_n and samples returning data on the rising edge of TxClk. The nominal clock frequency is 19.44 MHz. Figure 5-7 illustrates the timing requirements for the transmit interface. The target timing values relative to TxClk are listed in Table 5-6.

Figure 5-7. Transmit Timing Parameters

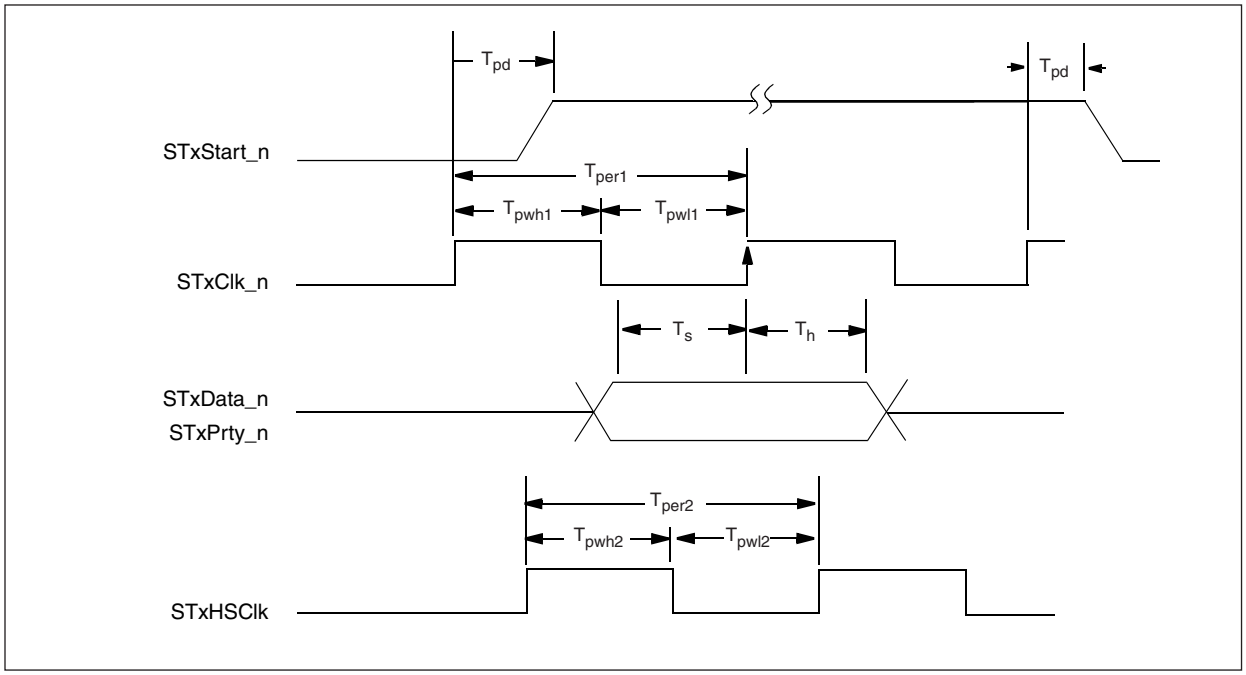


Table 5-6. Transmit Timing Values

Label	Description	Min	Typical	Max	Unit	Load
T_{per1}	Period, STxClk_n (nominal 19.44 MHz)	—	51.44	—	ns	20 pF
T_{pwh1}	Pulse width high, STxClk_n	23	—	—	ns	20 pF
T_{pwl1}	Pulse width low, STxClk_n (not including gapping)	23	—	—	ns	20 pF
T_{pd}	Propagation delay, STxStart_n from rising edge of STxClk_n	1	—	5	ns	20 pF
T_s	Setup, STxData_n/STxPrty_n to rising edge of TxClk	12	—	—	ns	20 pF
T_h	Hold, STxData_n/STxPrty_n from rising edge of TxClk	0	—	—	ns	20 pF
T_{per2}	Period, STxHSClk	—	19.29	—	ns	20 pF
T_{pwh2}	Pulse width high, STxHSClk	8.6	—	—	ns	20 pF
T_{pwl2}	Pulse width low, STxHSClk	8.2	—	—	ns	20 pF

5.1.3 SI-Bus Receive Timing

The CX29610 generates clock, data, and control signals. The CX29610 generates control and data outputs synchronously with the rising edge of RxClk. The nominal clock frequency is 19.44 MHz but will be gapped in various modes. Gapping blanks out high pulses. Figure 5-8 illustrates the timing requirements for the receive interface. The target timing values are listed in Table 5-7.

Figure 5-8. Receive Timing Parameters

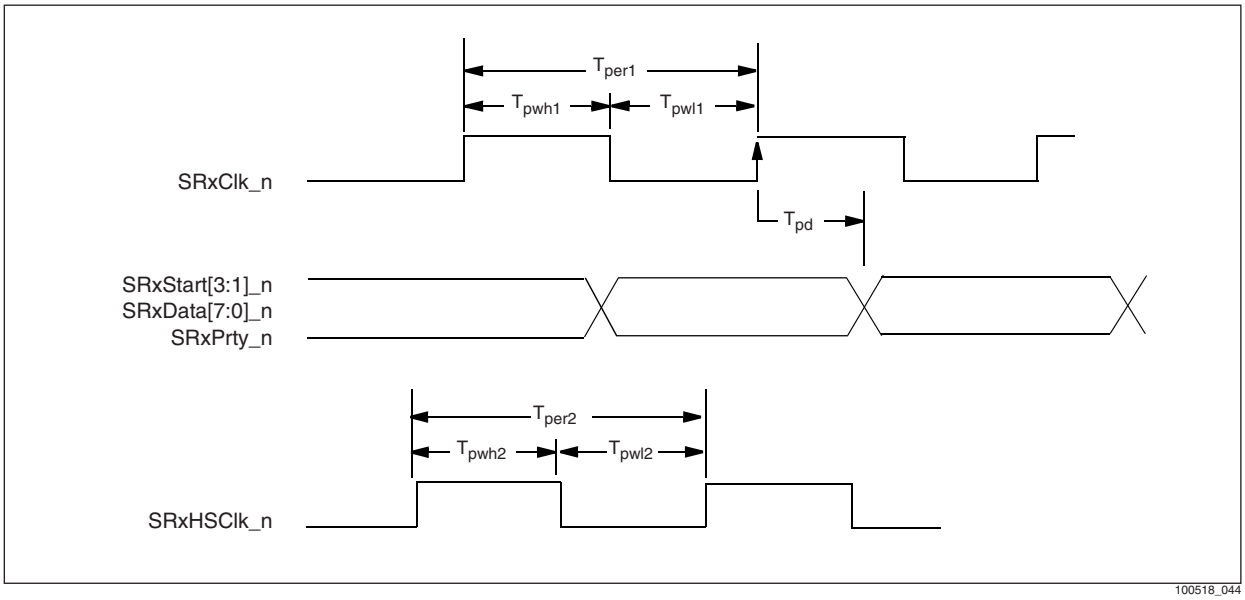


Table 5-7. Receive Timing Values

Label	Description	Min	Typical	Max	Unit	Load
T_{per1}	Period, SRxClk_n (nominal 19.44 MHz)	—	51.44	—	ns	—
T_{pwh1}	Pulse width high, SRxClk_n	23	—	—	ns	20 pF
T_{pwl1}	Pulse width low, SRxClk_n (not including gapping)	23	—	—	ns	20 pF
T_{pd}	Propagation delay, SRxStart[3:1}_n/SRxData[7:0]_n/SRxPrty_n from rising edge of SRxClk_n	0	—	5	ns	20 pF
T_{per2}	Period, SRxHSClk_n	—	19.29	—	ns	20 pF
T_{pwh2}	Pulse width high, SRxHSClk_n	8.6	—	—	ns	20 pF
T_{pwl2}	Pulse width low, SRxHSClk_n (not including gapping)	8.2	—	—	ns	20 pF

5.1.4 JTAG Interface Timing

Table 5-8 and Figure 5-9 illustrate the timing requirements and characteristics of the JTAG interface.

Figure 5-9. JTAG Timing Diagram

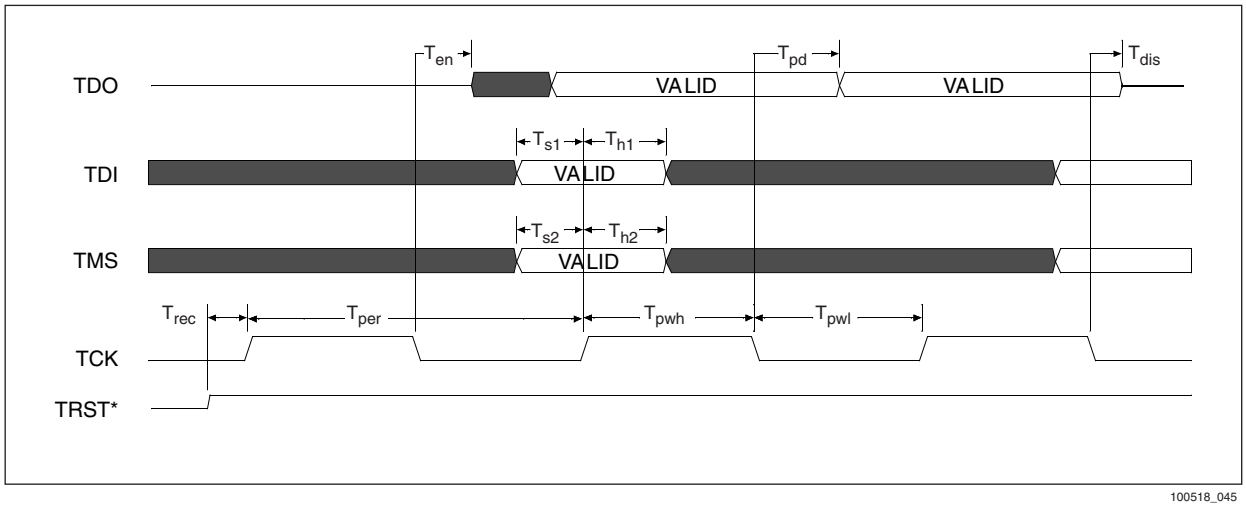


Table 5-8. JTAG Timing Table

Label	Description	Min	Max	Unit	Load
T_{s1}	Setup, TDI to the rising edge of TCK	15	—	ns	—
T_{s2}	Setup, TMS to the rising edge of TCK	15	—	ns	—
T_{h1}	Hold, TDI from the rising edge of TCK	20	—	ns	—
T_{h2}	Hold, TMS from the rising edge of TCK	20	—	ns	—
T_{pwh}	Pulse width high, TCK	80	—	ns	—
T_{pwl}	Pulse width low, TCK	80	—	ns	—
T_{en}	Enable, TDO from the falling edge of TCK	2	15	ns	—
T_{pd}	Propagation Delay, TDO from the falling edge of TCK	—	50	ns	—
T_{dis}	Disable, TDO from the falling edge of TCK	—	25	ns	—
T_{rec}	Recovery time, TCK from the rising edge of TRST*	2.5	—	ns	—
T_{per}	Period, TCK	100	—	ns	—

5.1.5 One-second Interface Timing

Figure 5-10 and Table 5-9 illustrate the timing requirements and characteristics of the One-second interface.

Figure 5-10. One-second Timing Diagram

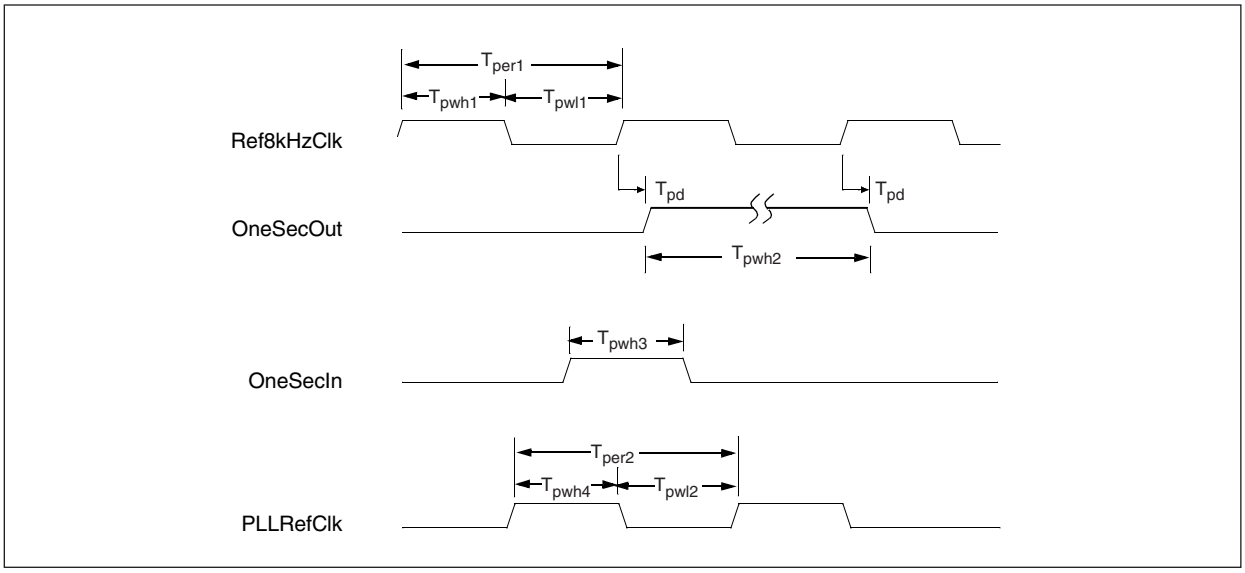


Table 5-9. One-second Timing Table

Symbol	Description	Min	Typical	Max	Unit	Load
T_{per1}	Period, Ref8kHzClk	—	125	—	µs	
T_{pwh1}	Pulse Width High, Ref8kHzClk	10	—	—	ns	—
T_{pwl1}	Pulse Width Low, Ref8kHzClk	10	—	—	ns	—
T_{pd}	Propagation Delay, OneSecOut from the rising edge of Ref8kHzClk	50	—	6	ns	20 pF
T_{pwh2}	Pulse Width High, OneSecOut	—	125	—	µs	20 pF
T_{pwl2}	Pulse Width Low, OneSecOut	—	875	—	µs	20 pF
T_{pwh3}	Pulse Width High, OneSecIn	130[1]	—	—	ns	—
T_{pwl3}	Pulse Width Low, OneSecIn	130[1]	—	—	ns	—
T_{per2}	Period, RxPLLClk	—	51.44	—	ns	—
T_{pwh4}	Pulse Width High, RxPLLClk	23	—	—	ns	—
T_{pwl2}	Pulse Width Low, RxPLLClk	23	—	—	ns	—

(1) The minimum pulse width high and low of OneSecOut, t_{pwl2} and t_{pwh2}, varies with the period of MClk, t_{per}, shown in Figure 5-4 according to the relationship t_{per} + 5.

5.1.6 DCC Interface Timing

Table 5-10 and Figure 5-11 illustrate the timing requirements and characteristics of the DCC interface.

Figure 5-11. DCC Timing Diagram

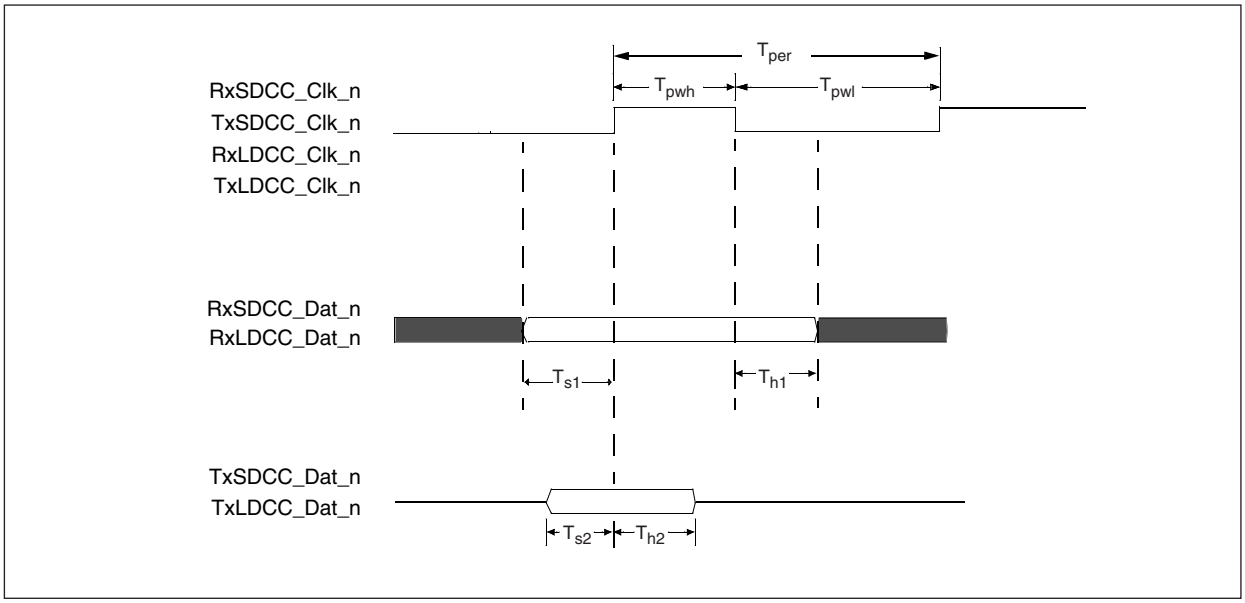


Table 5-10. LDCC Timing Table

Symbol	Description	Min	Typical	Max	Unit	Load
T_{per}	Period, RxLDCC_Clk_n/TxLDCC_Clk_n	—	1.74	—	µs	20 pF
T_{pwh}	Pulse Width High, RxLDCC_Clk_n/TxLDCC_Clk_n	0.520	—	—	µs	20 pF
T_{pwl}	Pulse Width Low, RxLDCC_Clk_n/TxLDCC_Clk_n	1.10	—	—	µs	20 pF
T_{s1}	Setup, RxLDCC_Dat_n to the rising edge of RxLDCC_Clk_n	50	—	—	ns	20 pF
T_{h1}	Hold, RxLDCC_Dat_n from the rising edge of RxLDCC_Clk_n	25	—	—	ns	20 pF
T_{s2}	Setup, TxLDCC_Dat_n to the rising edge of TxLDCC_Clk_n	50	—	—	ns	—
T_{h2}	Hold, TxLDCC_Dat_n from the rising edge of TxLDCC_Clk_n	25	—	—	ns	—

Table 5-11. SDCC Timing Table

Symbol	Description	Min	Typical	Max	Unit	Load
T_{per}	Period, RxSDCC_Clk_n/TxSDCC_Clk_n	—	5.2	—	µs	20 pF
T_{pwh}	Pulse Width High, RxSDCC_Clk_n/ TxSDCC_Clk_n	1.5	—	—	µs	20 pF
T_{pwl}	Pulse Width Low, RxSDCC_Clk_n/ TxSDCC_Clk_n	3.1	—	—	µs	20 pF
T_{s1}	Setup, RxSDCC_Dat_n to the rising edge of RxSDCC_Clk_n	50	—	—	ns	20 pF
T_{h1}	Hold, RxSDCC_Dat_n from the rising edge of RxSDCC_Clk_n	25	—	—	ns	20 pF
T_{s2}	Setup, TxSDCC_Dat_n to the rising edge of TxSDCC_Clk_n	50	—	—	ns	—
T_{h2}	Hold, TxSDCC_Dat_n from the rising edge of TxSDCC_Clk_n	25	—	—	ns	—

5.1.7 SONET Reference Timing

Figure 5-12 and Table 5-12 illustrate the timing requirements and characteristics of the SONET reference.

Figure 5-12. SONET Reference Timing Diagram

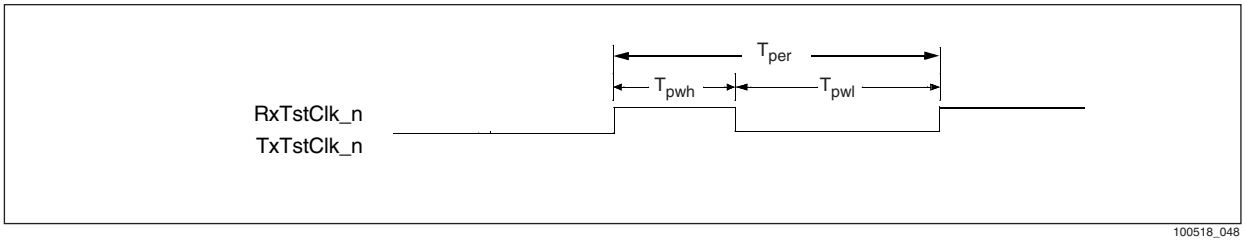


Table 5-12. SONET Reference Timing Table

Symbol	Description	Min	Typical	Max	Unit	Load
T_{per}	Period	—	51.44	—	ns	—
T_{pwh}	Pulse Width High	23	—	—	ns	20 pF
T_{pwl}	Pulse Width Low	23	—	—	ns	20 pF

5.1.8 Frame Reference Timing

Figure 5-13 and Table 5-13 illustrate the timing requirements and characteristics of the Frame reference.

Figure 5-13. Frame Reference Timing Diagram

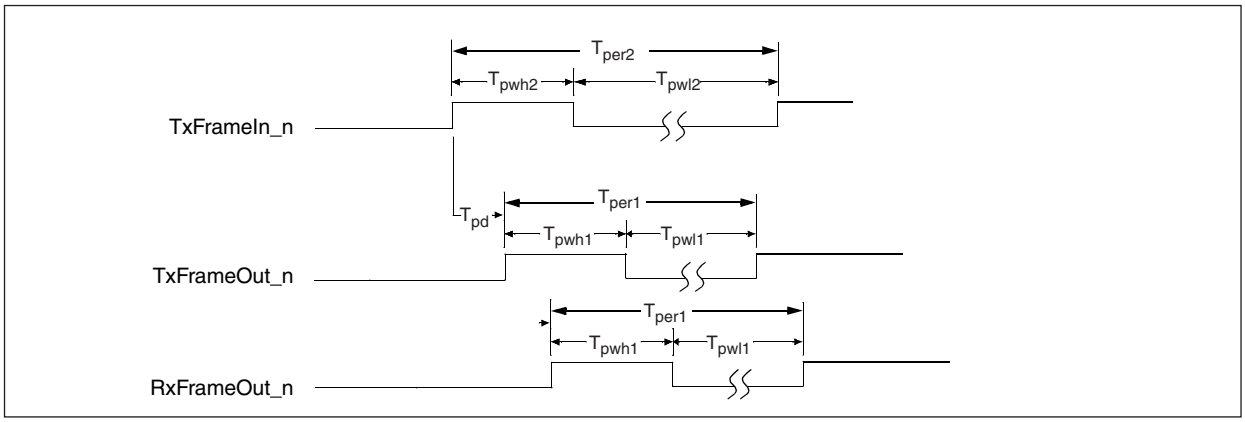


Table 5-13. Frame Timing Table

Symbol	Description	Min	Typical	Max	Unit	Load
t_{per1}	Period, RxFrameOut_n and TxFrameOut_n	—	125	—	µs	—
t_{pwh1}	Pulse Width High, RxFrameOut_n and TxFrameOut_n	12	—	—	µs	20 pF
t_{pwl1}	Pulse Width Low, RxFrameOut_n and TxFrameOut_n	100	—	—	µs	20 pF
t_{pd}	Propagation delay, RxFrameOut_n/ TxFrameOut_n from the rising edge of TxFrameIn_n	50	—	0.06	ns	20 pF
t_{per2}	Period, TxFrameIn_n	—	125	—	µs	—
t_{pwh2}	Pulse Width High, TxFrameIn_n	0.06	—	—	µs	—
t_{pwl2}	Pulse Width Low, TxFrameIn_n	0.06	—	—	µs	—

5.1.9 Rx8kHz Interface Timing

Figure 5-14 and Table 5-14 illustrate the timing requirements and characteristics of the Rx8kHz interface.

Figure 5-14. Rx8kHz Timing Diagram

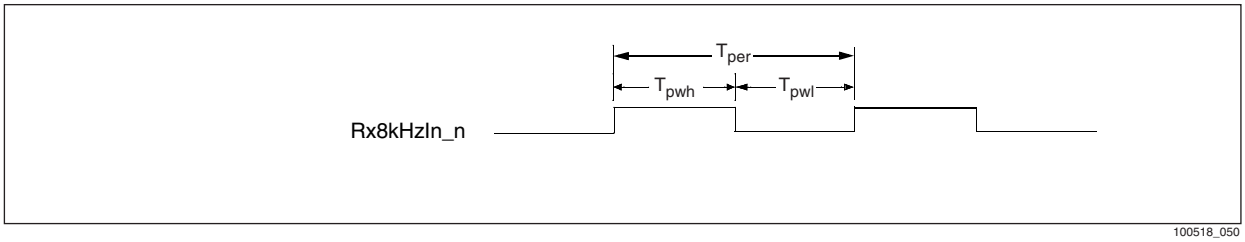


Table 5-14. Rx8kHz Timing Table

Symbol	Description	Min	Typical	Max	Unit	Load
t_{per}	Period	—	125	—	µs	20 pF
t_{pwh}	Pulse Width High	56	—	—	µs	20 pF
t_{pwl}	Pulse Width Low	56	—	—	µs	20 pF

5.1.10 E1/E2 Interface Timing

Figure 5-15 and Table 5-15 illustrate the timing requirements and characteristics of the E1/E2 interface.

Figure 5-15. E1/E2 Timing Diagram

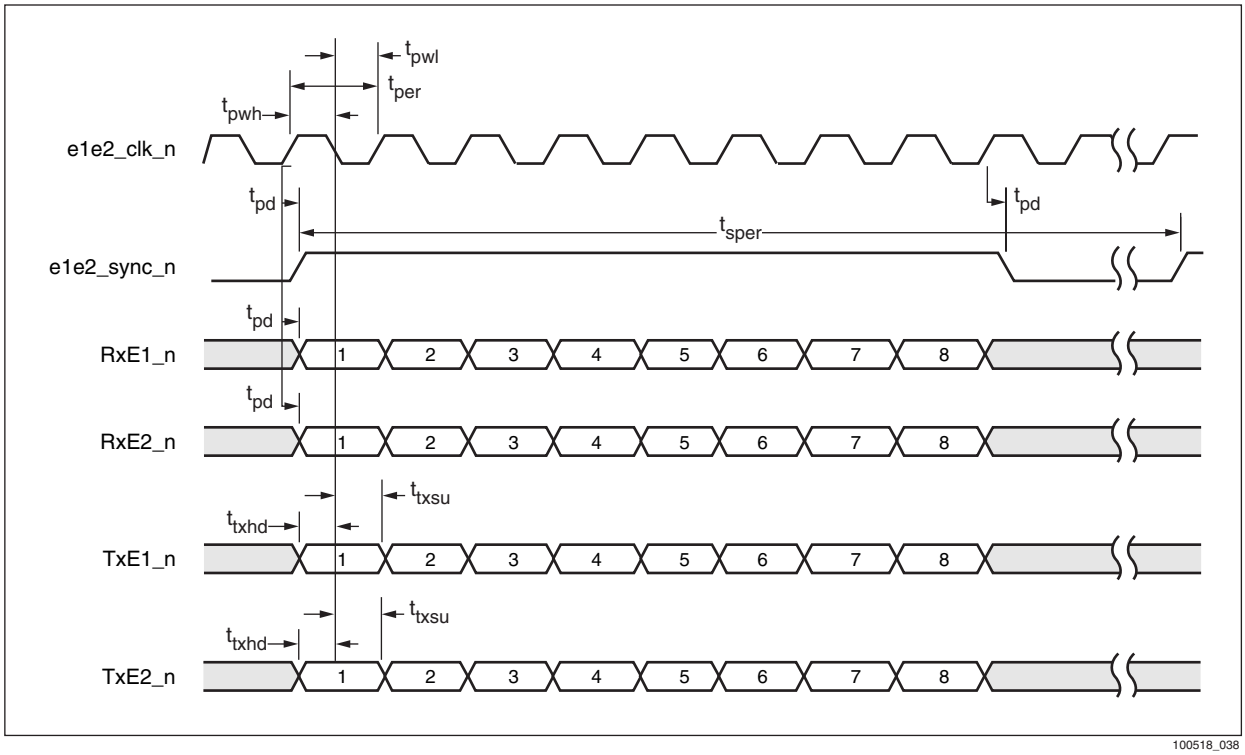


Table 5-15. E1/E2 Timing Table

Symbol	Description	Min	Typical	Max	Unit	Load
t_{per}	Period, e1e2_clk_n	—	488.28	—	ns	
t_{pwh}	Pulse Width High, e1e2_clk_n	219	—	—	ns	20 pF
t_{pwl}	Pulse Width Low, e1e2_clk_n	219	—	—	ns	20 pF
t_{sper}	Period, e1e2_sync_n	—	125	—	µs	20 pF
t_{pd}	Propagation Delay, e1e2_sync_n, RxE1_n, and RxE2_n	50	—	—	ns	20 pF
t_{txsu}	TxE1_n setup to e1e2_clk_n fall	5	—	—	ns	
t_{txhd}	TxE1_n hold from e1e2_clk_n fall	2	—	—	ns	

5.2 Absolute Maximum Ratings

The absolute maximum ratings listed in Table 5-16 are the maximum stresses that the device can tolerate without risking permanent damage. These ratings are not typical of normal operation of the device. Exposure to absolute maximum rating conditions for extended periods of time may affect the device's reliability. This device should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Table 5-16. Absolute Maximum Ratings

Parameter	Value
Supply Voltage	3.3 V ± 5% VDD and AVDD
Operating Power Consumption	2.30 W
Operating Temperature @ 100 LFM(1)	-40 ºC to +85 ºC
Storage Temperature	-40 ºC to +125 ºC
Ambient Temperature under Bias	-40 ºC to +85 ºC
Lead Temperature	+240 ºC for 10 seconds
Junction Temperature	+150 ºC
Static Discharge Voltage - Human Body Model	± 1500 V @ 25 ºC
Static Discharge Voltage - Charged Device Model	± 350 V @ 25 ºC
Latch-up Voltage - Power Supply Pin	5.5 V @ 125 ºC
Latch-up Current - I/O Pin	± 200 mA @ 125 ºC

Footnote:
(1) Airflow requirement is 0 LFM for this ambient temperature range for the following operating mode: Single OC-3 mode (one OC-3 port active and other 3 OC-3 ports powered down) - GEN register, bit 7 = 0 and PWRDWN register set appropriately. Airflow requirement is 100 LFM for this ambient temperature range if the device is operated in OC-12 mode (GEN register, bit 7 = 1) or if all four ports are active in OC-3 mode.

5.3 DC Characteristics

This section describes the DC characteristics of the CX29610. The typical conditions are listed below, and the DC characteristics are listed in Table 5-17.

Typical conditions: VDD = AVDD = 3.3 V
T_A = 25 °C
VDD ≤ VGG ≤ 5.5 V
3.135 ≤ VDD ≤ 3.465 V
VDD ≤ VGG ≤ 5.5 V
–40 °C ≤ T_A ≤ 85 °C
@ 100 LFM(1)

NOTE(S):
(1) See footnote to Table 5-16 regarding airflow requirements for the device.

Table 5-17. DC Characteristics

Parameter	Min	Max	Unit	Conditions
Input Low Voltage (VIL)				
5V-Tolerant TTL	0	0.8	V DC	
Input High Voltage (VIH)				
5V-Tolerant TTL	2.0	5.25	V DC	
TTL Output Low Voltage (VOL)		0.4	V DC	I_{OH} = 4.0 mA
TTL Output High Voltage (VOH)	2.4		V DC	I_{OH} = 1500 µA
Pull-Up Resistance (Rpu)	15	75	kOhms	
Input Leakage Current	-10	10	µA	Vin = PWR or GND
Three-state Output Leakage Current	-10	10	µA	Vout = PWR or GND
Input Capacitance		7	pF	
Output Capacitance		7	pF	
Bidirectional Capacitance		7	pF	
NOTE: All outputs are TTL drive levels and can be used with 3 V CMOS or 5 V TTL logic.				

5.3.1 PECL Input

The PECL input DC characteristics are shown in Table 5-18.

Table 5-18. PECL—Input Characteristics

Symbol	Parameter	Min.	Typical	Max.	Units
V_{cm}	Common mode voltage	V_{dd} – 1.6	V_{dd} – 1.55	V_{dd} – 1.2	V
V_{diff}	Differential mode voltage	200	400	800	mV
V_{ih}	High voltage	V_{dd} – 1.2	V_{dd} – 1.0	V_{dd} – 0.9	V
V_{il}	Low voltage	V_{dd} – 2.0	V_{dd} – 2.1	V_{dd} – 1.5	V
NOTE: All PECL voltages are referenced to ground.					

5.3.2 PECL Output

The PECL output DC characteristics are shown in Table 5-19.

Table 5-19. PECL—Output Characteristics

Symbol	Parameter	Min.	Typical	Max.	Units
V_{cm}	Common mode voltage	V_{dd} – 1.55	V_{dd} – 1.37	V_{dd} – 1.23	V
V_{diff}	Differential mode voltage	700	850	900	mV
V_{oh}	High voltage	V_{dd} – 1.10	V_{dd} – 0.95	V_{dd} – 0.80	V
V_{ol}	Low voltage	V_{dd} – 2.0	V_{dd} – 1.80	V_{dd} – 1.65	V
	Rise/fall time	—	120	150	ps
NOTE:					

5.3.3 Single-ended PECL Input (LSigDet)

The single-ended PECL input DC characteristics are shown in Table 5-20.

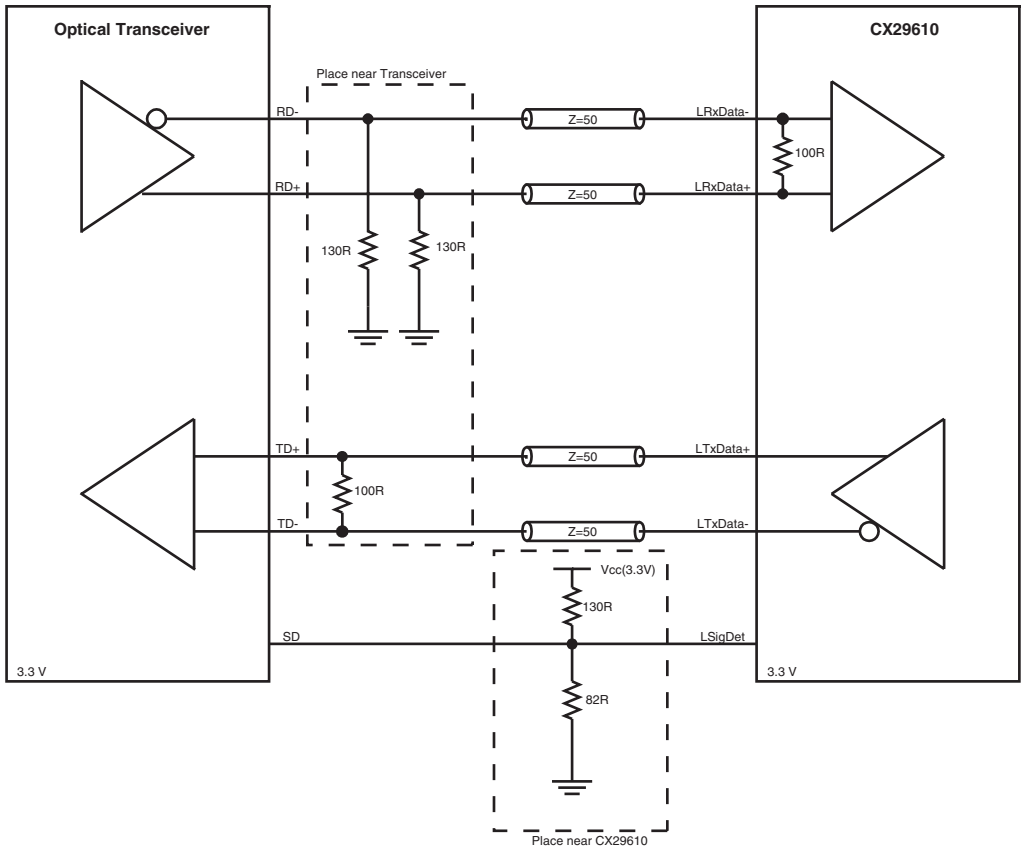
Table 5-20. Single-ended PECL Table

Symbol	Parameter	Minimum	Typical	Maximum
V_{ih}	—	2.10 V	—	—
V_{il}	—	—	—	1.86 V
I_{ih}	—	—	—	10 µA
I_{il}	—	-10 µA	—	—

5.3.4 Low Voltage PECL (LVPECL) Interface Example

Figure 5-16 illustrates interfacing a 3.3 V optical transceiver to the CX29610 device.

Figure 5-16. LVPECL Interface



Note(s):

1. The 100 ohm resistor is built in the CX29610 for LRxData+ and LRxData- termination.
2. The LTxData+ and LTxData- outputs are internally biased and therefore do not require external bias resistors.
3. The termination resistors on the LSigDet input are necessary only for transceivers with a PECL level signal detect (SD) output.

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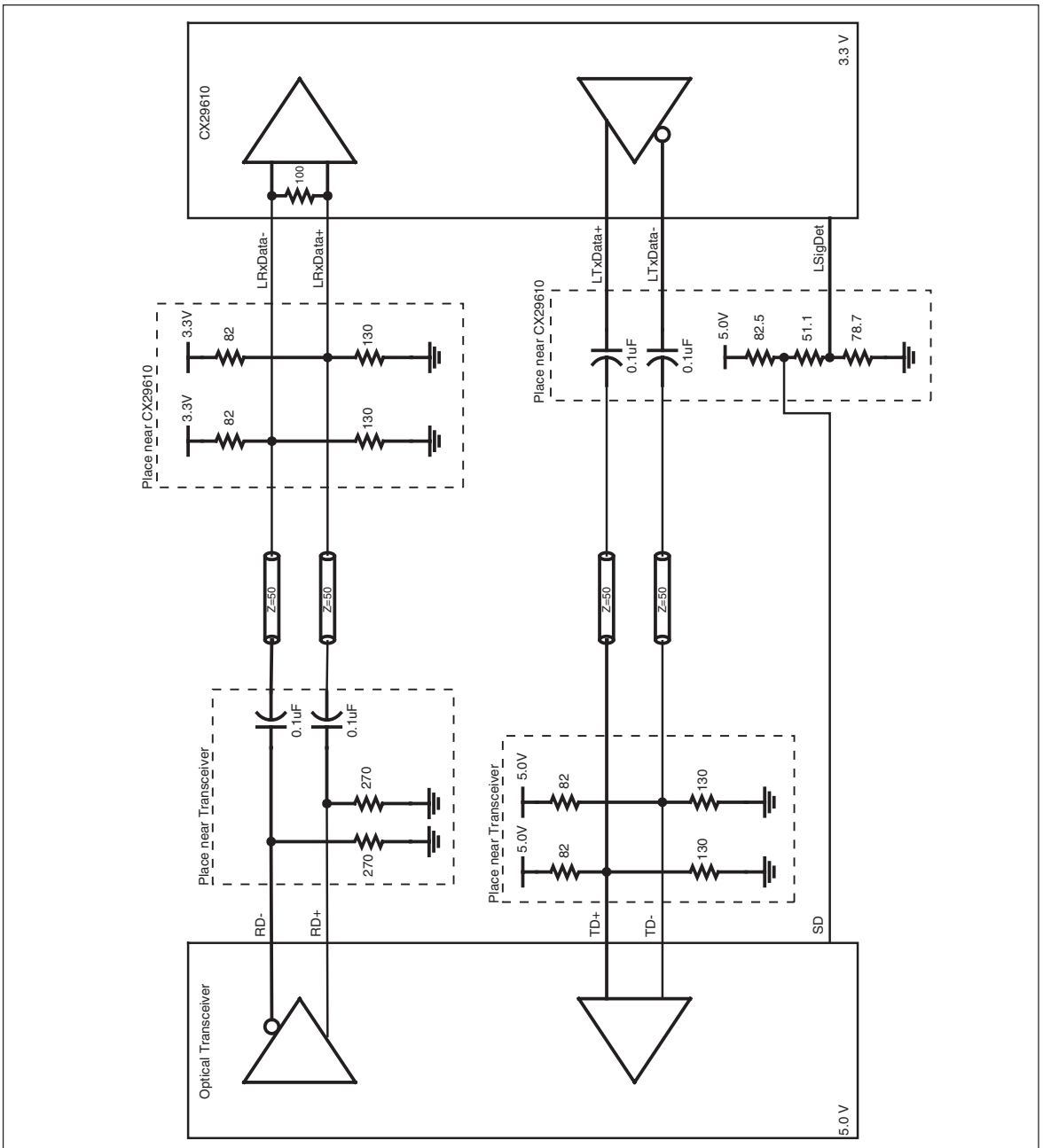
5.3.5 PECL to LVPECL Interface Example

Figure 5-17 illustrates interfacing a 5.0 V optical transceiver to the 3.3 V CX29610 device.

Figure 5-17. PECL to Low Voltage PECL (LVPECL) Interface



Note:

1. The 100 ohm resistor is built in the CX29610 for the LRxData+ and LRxData- termination.
2. The LTxData+ and LTxData- outputs are internally biased and therefore do not require external bias resistors.
3. The termination resistors on the LSigDet input are necessary only for transceivers with a PECL level signal detect (SD) output. The resistors should have a tolerance of 1%.

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5.4 Mechanical Specifications

Figure 5-19 and Figure 5-18 illustrate the ballout information for the CX29610 STS-12/4x STS-3 SONET Multiplexer from the top and bottom views. It is a single CMOS integrated circuit packaged in a 416-pin PBGA. All unused input pins should be connected to ground. Unused outputs should be left unconnected. Pin listings are provided in Table 5-21.

Figure 5-20 illustrates a mechanical drawing of the device.

Figure 5-18. CX29610 Ballout Diagram (Top View)

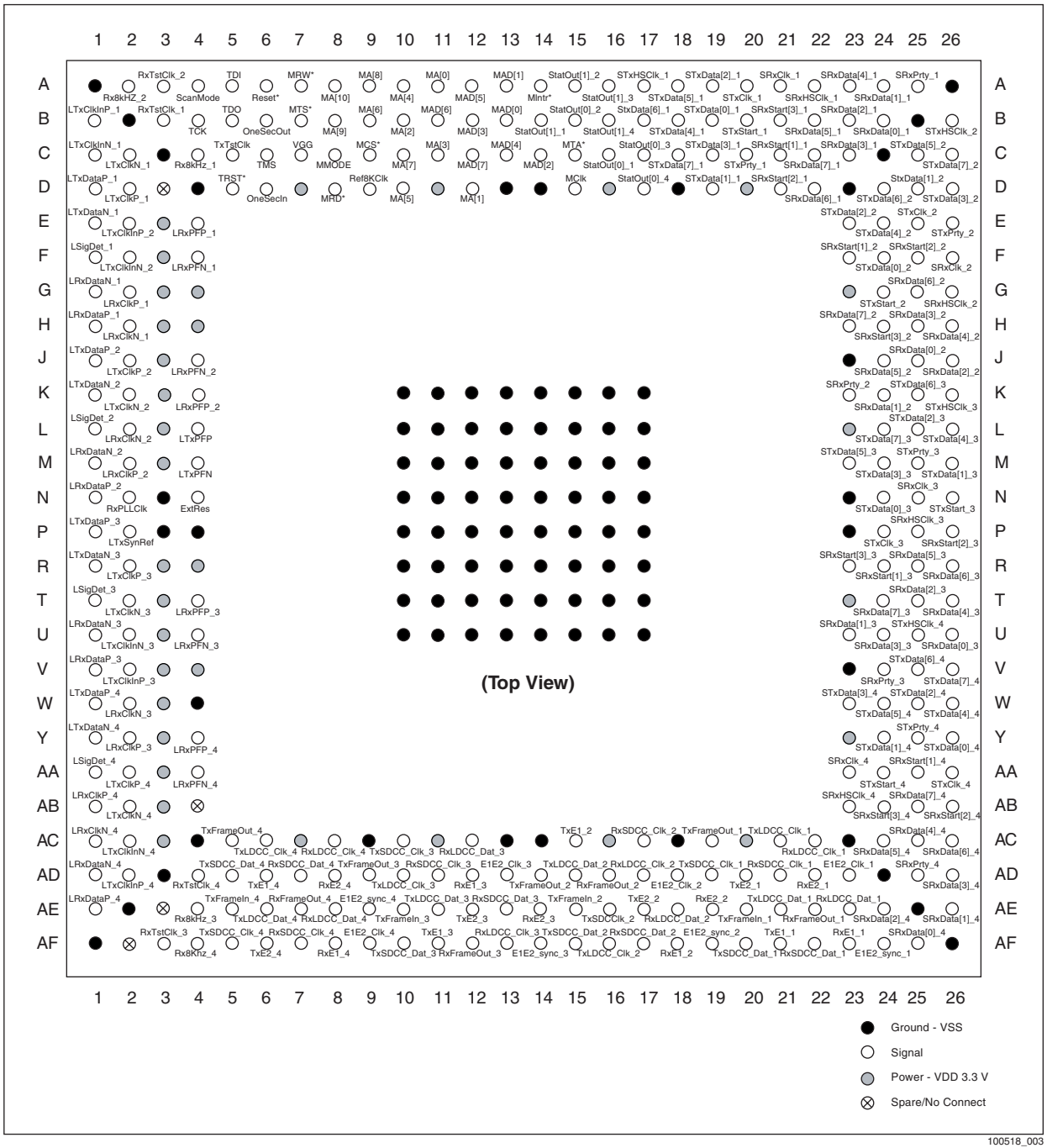


Figure 5-19. CX29610 Ballout Diagram (Bottom View)

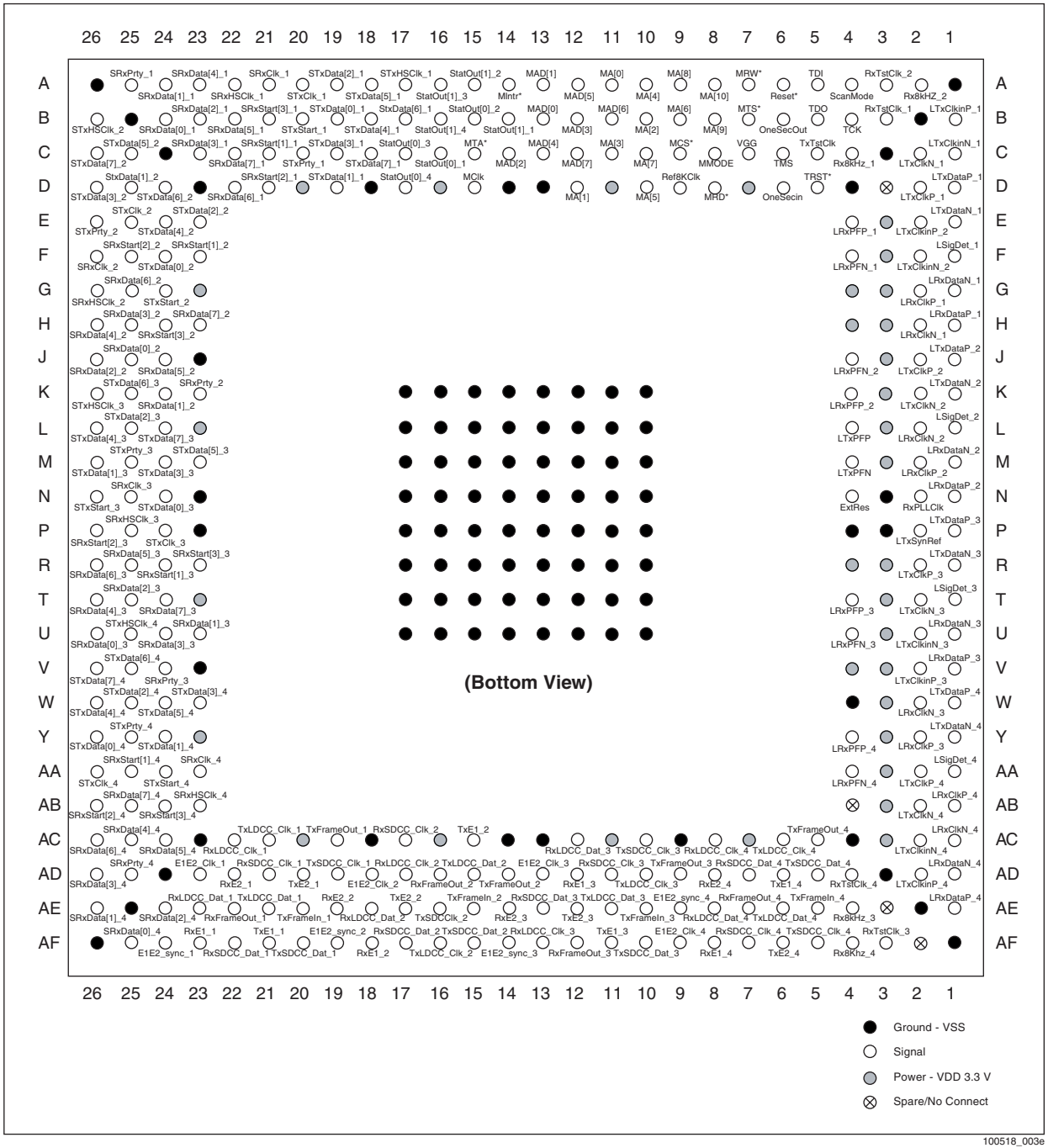


Figure 5-20. CX29610 Mechanical Drawing

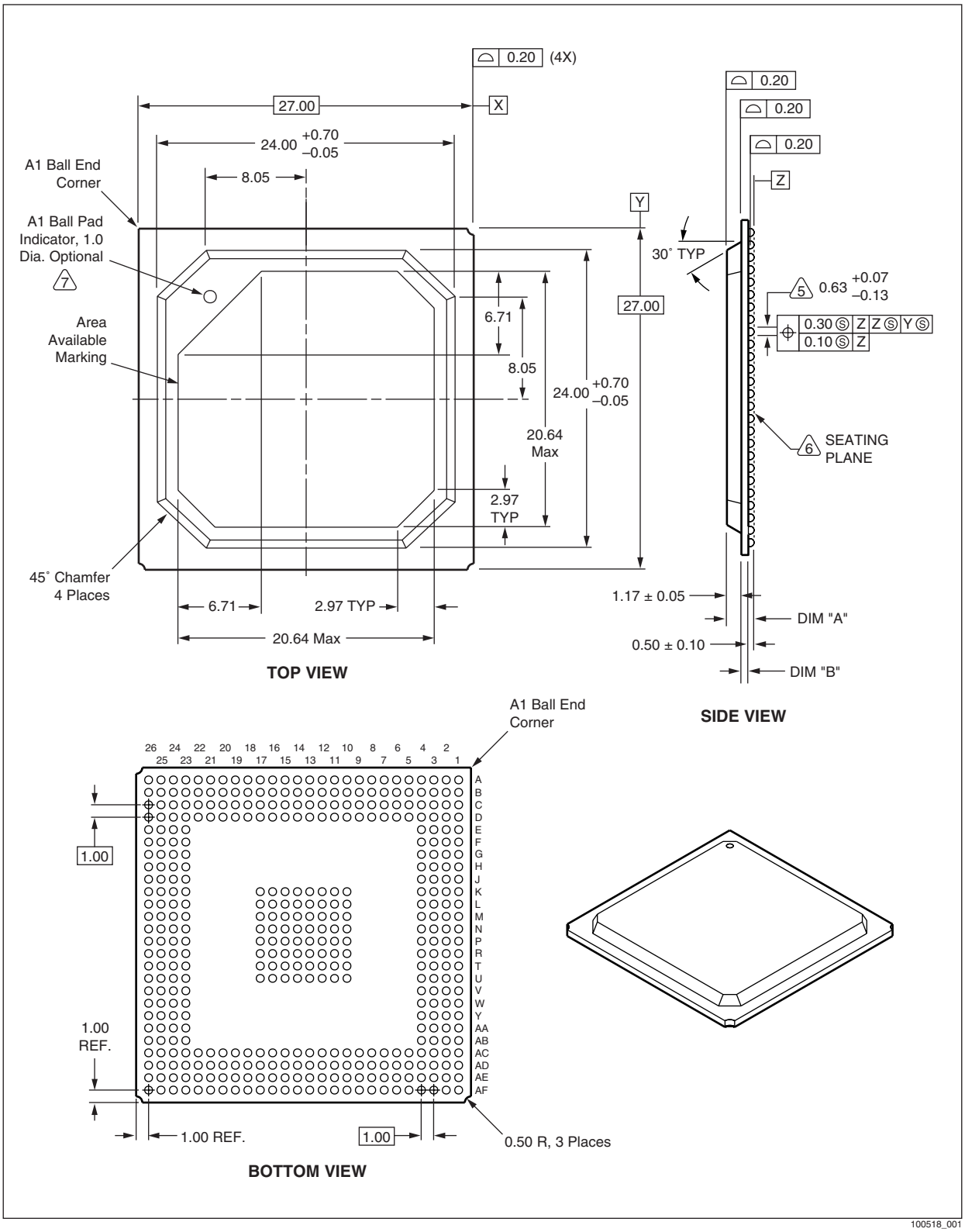


Table 5-21. Listing of Pin Numbers and Labels (Numeric Order) (1 of 4)

Pin Number	Pin Label	I/O(1)
A1	AVSS	—
A2	Rx8kHz_2	O
A3	RxTstClk_2	O
A4	ScanMode	I
A5	TDI	I
A6	Reset*	I
A7	MRW*	I
A8	MA[10]	I
A9	MA[8]	I
A10	MA[4]	I
A11	MA[0]	I
A12	MAD[5]	I/0
A13	MAD[1]	I/0
A14	MIntr*	OD
A15	StatOut[1]_2	O
A16	StatOut[1]_3	O
A17	STxHSClk_1	O
A18	STxData[5]_1	I
A19	STxData[2]_1	I
A20	STxClk_1	O
A21	SRxClk_1	O
A22	SRxHSClk_1	O
A23	SRxData[4]_1	O
A24	SRxData[1]_1	O
A25	SRxPrty_1	O
A26	VSS	—
B1	LTxClkIn+_1	I
B2	AVSS	—
B3	RxTstClk_1	O
B4	TCK	I
B5	TDO	O
B6	OneSecOut	O
B7	MTS*	I
B8	MA[9]	I
B9	MA[6]	I
B10	MA[2]	I
B11	MAD[6]	I/0
B12	MAD[3]	I/0
B13	MAD[0]	I/0
B14	StatOut[1]_1	O
B15	StatOut[0]_2	O
B16	StatOut[1]_4	O
B17	STxData[6]_1	I
B18	STxData[4]_1	I
B19	STxData[0]_1	I
B20	STxStart_1	O
B21	SRxStart[3]_1	O
B22	SRxData[5]_1	O
B23	SRxData[2]_1	O
B24	SRxData[0]_1	O
B25	VSS	—
B26	STxHSClk_2	O
C1	LTxClkIn–_1	I
C2	LTxClk–_1	O
C3	AVSS	—
C4	Rx8kHz_1	O
C5	TxTstClk	O
C6	TMS	I
C7	VGG	—
C8	MMode	I
C9	MCS*	I
C10	MA[7]	I
C11	MA[3]	I
C12	MAD[7]	I/0
C13	MAD[4]	I/0
C14	MAD[2]	I/0
C15	MTA*	O
C16	StatOut[0]_1	O
C17	StatOut[0]_3	O
C18	STxData[7]_1	I
C19	STxData[3]_1	I
C20	STxPrty_1	I
C21	SRxStart[1]_1	O
C22	SRxData[7]_1	O
C23	SRxData[3]_1	O
C24	VSS	—
C25	STxData[5]_2	I
C26	STxData[7]_2	I
D1	LTxData+_1	O
D2	LTxClk+_1	O
D3	Reserved - NC	—
D4	AVSS	—
D5	TRST*	I
D6	OneSecIn	I
D7	VDD	—
D8	MRD*	I
D9	Ref8KClk	I
D10	MA[5]	I
D11	VDD	—
D12	MA[1]	I
D13	VSS	—
D14	VSS	—
D15	MClk	I
D16	VDD	—
D17	StatOut[0]_4	O
D18	VSS	—
D19	STxData[1]_1	I
D20	VDD	—
D21	SRxStart[2]_1	O
D22	SRxData[6]_1	O
D23	VSS	—
D24	STxData[6]_2	I
D25	STxData[1]_2	I
D26	STxData[3]_2	I
E1	LTxData–_1	O

Table 5-16. Listing of Pin Numbers and Labels (Numeric Order) (2 of 4)

Pin Number	Pin Label	I/O(1)
E2	LTxClkIn+_2	I
E3	AVDD	—
E4	LRxPFP_1	I
E23	STxData[2]_2	I
E24	STxData[4]_2	I
E25	STxClk_2	O
E26	STxPrty_2	I
F1	LSigDet_1	I
F2	LTxClkIn–_2	I
F3	AVDD	—
F4	LRxPFN_1	I
F23	SRxStart[1]_2	O
F24	STxData[0]_2	I
F25	SRxStart[2]_2	O
F26	SRxClk_2	O
G1	LRxData–_1	I
G2	LRxClk+_1	I
G3	AVDD	—
G4	AVDD	—
G23	VDD	—
G24	STxStart_2	O
G25	SRxData[6]_2	O
G26	SRxHSClk_2	O
H1	LRxData+_1	I
H2	LRxClk–_1	I
H3	AVDD	—
H4	AVDD	—
H23	SRxData[7]_2	O
H24	SRxStart[3]_2	O
H25	SRxData[3]_2	O
H26	SRxData[4]_2	O
J1	LTxData+_2	O
J2	LTxClk+_2	O
J3	AVDD	—
J4	LRxPFN_2	I
J23	VSS	—
J24	SRxData[5]_2	O
J25	SRxData[0]_2	O
J26	SRxData[2]_2	O
K1	LTxData–_2	O
K2	LTxClk–_2	O
K3	AVDD	—
K4	LRxPFP_2	I
K10	VSS	—
K11	VSS	—
K12	VSS	—
K13	VSS	—
K14	VSS	—
K15	VSS	—
K16	VSS	—
K17	VSS	—
K23	SRxPrty_2	O
K24	SRxData[1]_2	O
K25	STxData[6]_3	I
K26	STxHSClk_3	O
L1	LSigDet_2	I
L2	LRxClk–_2	I
L3	AVDD	—
L4	LTxPFP	I
L10	AVSS	—
L11	VSS	—
L12	VSS	—
L13	VSS	—
L14	VSS	—
L15	VSS	—
L16	VSS	—
L17	VSS	—
L23	VDD	—
L24	STxData[7]_3	I
L25	STxData[2]_3	I
L26	STxData[4]_3	I
M1	LRxData–_2	I
M2	LRxClk+_2	I
M3	AVDD	—
M4	LTxPFN	I
M10	AVSS	—
M11	AVSS	—
M12	VSS	—
M13	VSS	—
M14	VSS	—
M15	VSS	—
M16	VSS	—
M17	VSS	—
M23	STxData[5]_3	I
M24	STxData[3]_3	I
M25	STxPrty_3	I
M26	STxData[1]_3	I
N1	LRxData+_2	I
N2	RxPLLClk	I
N3	AVSS	—
N4	ExtRes	I
N10	AVSS	—
N11	AVSS	—
N12	VSS	—
N13	VSS	—
N14	VSS	—
N15	VSS	—
N16	VSS	—
N17	VSS	—
N23	VSS	—
N24	STxData[0]_3	I
N25	SRxClk_3	O
N26	STxStart_3	O
P1	LTxData+_3	O
P2	LTxSynRef	I

Table 5-16. Listing of Pin Numbers and Labels (Numeric Order) (3 of 4)

Pin Number	Pin Label	I/O(1)
P3	AVSS	—
P4	AVSS	—
P10	AVSS	—
P11	AVSS	—
P12	VSS	—
P13	VSS	—
P14	VSS	—
P15	VSS	—
P16	VSS	—
P17	VSS	—
P23	VSS	—
P24	STxClk_3	O
P25	SRxHSClk_3	O
P26	SRxStart[2]_3	O
R1	LTxData–_3	O
R2	LTxClk+_3	O
R3	AVDD	—
R4	AVDD	—
R10	AVSS	—
R11	AVSS	—
R12	VSS	—
R13	VSS	—
R14	VSS	—
R15	VSS	—
R16	VSS	—
R17	VSS	—
R23	SRxStart[3]_3	O
R24	SRxStart[1]_3	O
R25	SRxData[5]_3	O
R26	SRxData[6]_3	O
T1	LSigDet_3	I
T2	LTxClk–_3	O
T3	AVDD	—
T4	LRxPFP_3	I
T10	AVSS	—
T11	VSS	—
T12	VSS	—
T13	VSS	—
T14	VSS	—
T15	VSS	—
T16	VSS	—
T17	VSS	—
T23	VDD	—
T24	SRxData[7]_3	O
T25	SRxData[2]_3	O
T26	SRxData[4]_3	O
U1	LRxData–_3	I
U2	LTxClkIn–_3	I
U3	AVDD	—
U4	LRxPFN_3	I
U10	VSS	—
U11	VSS	—
U12	VSS	—
U13	VSS	—
U14	VSS	—
U15	VSS	—
U16	VSS	—
U17	VSS	—
U23	SRxData[1]_3	O
U24	SRxData[3]_3	O
U25	STxHSClk_4	O
U26	SRxData[0]_3	O
V1	LRxData+_3	I
V2	LTxClkIn+_3	I
V3	AVDD	—
V4	AVDD	—
V23	VSS	—
V24	SRxPrty_3	O
V25	STxData[6]_4	I
V26	STxData[7]_4	I
W1	LTxData+_4	O
W2	LRxClk–_3	I
W3	AVDD	—
W4	AVSS	—
W23	STxData[3]_4	I
W24	STxData[5]_4	I
W25	STxData[2]_4	I
W26	STxData[4]_4	I
Y1	LTxData–_4	O
Y2	LRxClk+_3	I
Y3	AVDD	—
Y4	LRxPFP_4	I
Y23	VDD	—
Y24	STxData[1]_4	I
Y25	STxPrty_4	I
Y26	STxData[0]_4	I
AA1	LSigDet_4	I
AA2	LTxClk+_4	O
AA3	AVDD	—
AA4	LRxPFN_4	I
AA23	SRxClk_4	O
AA24	STxStart_4	O
AA25	SRxStart[1]_4	O
AA26	STxClk_4	O
AB1	LRxClk+_4	I
AB2	LTxClk–_4	O
AB3	AVDD	—
AB4	Reserved - NC	—
AB23	SRxHSClk_4	O
AB24	SRxStart[3]_4	O
AB25	SRxData[7]_4	O
AB26	SRxStart[2]_4	O
AC1	LRxClk–_4	I
AC2	LTxClkIn–_4	I
AC3	AVDD	—

Table 5-16. Listing of Pin Numbers and Labels (Numeric Order) (4 of 4)

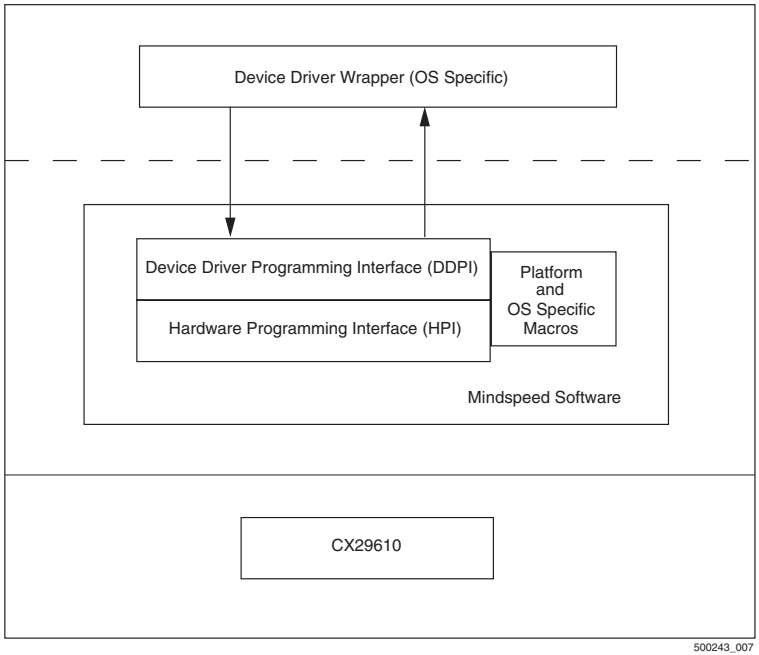
Pin Number	Pin Label	I/O(1)
AC4	AVSS	—
AC5	TxFrameOut_4	O
AC6	TxLDCC_Clk_4	O
AC7	VDD	—
AC8	RxLDCC_Clk_4	O
AC9	VSS	—
AC10	TxSDCC_Clk_3	O
AC11	VDD	—
AC12	RxLDCC_Dat_3	O
AC13	VSS	—
AC14	VSS	—
AC15	TxE1_2	I
AC16	VDD	—
AC17	RxSDCC_Clk_2	O
AC18	VSS	—
AC19	TxFrameOut_1	O
AC20	VDD	—
AC21	TxLDCC_Clk_1	O
AC22	RxLDCC_Clk_1	O
AC23	VSS	—
AC24	SRxData[5]_4	O
AC25	SRxData[4]_4	O
AC26	SRxData[6]_4	O
AD1	LRxData–_4	I
AD2	LTxClkIn+_4	I
AD3	AVSS	—
AD4	RxTstClk_4	O
AD5	TxSDCC_Dat_4	I
AD6	TxE1_4	I
AD7	RxSDCC_Dat_4	O
AD8	RxE2_4	O
AD9	TxFrameOut_3	O
AD10	TxLDCC_Clk_3	O
AD11	RxSDCC_Clk_3	O
AD12	RxE1_3	O
AD13	E1E2_Clk_3	O
AD14	TxFrameOut_2	O
AD15	TxLDCC_Dat_2	I
AD16	RxFrameOut_2	O
AD17	RxLDCC_Clk_2	O
AD18	E1E2_Clk_2	O
AD19	TxSDCC_Clk_1	O
AD20	TxE2_1	I
AD21	RxSDCC_Clk_1	O
AD22	RxE2_1	O
AD23	E1E2_Clk_1	O
AD24	VSS	—
AD25	SRxPrty_4	O
AD26	SRxData[3]_4	O
AE1	LRxData+_4	I
AE2	AVSS	—
AE3	Reserved - NC	—
AE4	Rx8kHz_3	O
AE5	TxFrameIn_4	I
AE6	TxLDCC_Dat_4	I
AE7	RxFrameOut_4	O
AE8	RxLDCC_Dat_4	O
AE9	E1E2_sync_4	O
AE10	TxFrameIn_3	I
AE11	TxLDCC_Dat_3	I
AE12	TxE2_3	I
AE13	RxSDCC_Dat_3	O
AE14	RxE2_3	O
AE15	TxFrameIn_2	I
AE16	TxSDCC_Clk_2	O
AE17	TxE2_2	I
AE18	RxLDCC_Dat_2	O
AE19	RxE2_2	O
AE20	TxFrameIn_1	I
AE21	TxLDCC_Dat_1	I
AE22	RxFrameOut_1	O
AE23	RxLDCC_Dat_1	O
AE24	SRxData[2]_4	O
AE25	VSS	—
AE26	SRxData[1]_4	O
AF1	AVSS	—
AF2	Reserved - NC	—
AF3	RxTstClk_3	O
AF4	Rx8kHz_4	O
AF5	TxSDCC_Clk_4	O
AF6	TxE2_4	I
AF7	RxSDCC_Clk_4	O
AF8	RxE1_4	O
AF9	E1E2_Clk_4	O
AF10	TxSDCC_Dat_3	I
AF11	TxE1_3	I
AF12	RxFrameOut_3	O
AF13	RxLDCC_Clk_3	O
AF14	E1E2_sync_3	O
AF15	TxSDCC_Dat_2	I
AF16	TxLDCC_Clk_2	O
AF17	RxSDCC_Dat_2	O
AF18	RxE1_2	O
AF19	E1E2_sync_2	O
AF20	TxSDCC_Dat_1	I
AF21	TxE1_1	I
AF22	RxSDCC_Dat_1	O
AF23	RxE1_1	O
AF24	E1E2_sync_1	O
AF25	SRxData[0]_4	O
AF26	VSS	—

NOTE(S):
(1)Key:
I = Input
O = Output
OD = Open Drain Output
The symbol (*) indicates Active Low

Appendix A : CX29610 Software Overview

The Mindspeed CX29610 software consists of two layers. The purpose of the lowest layer, the Hardware Programming Interface (HPI), is to abstract the hardware details from the interface user. The HPI provides a broad interface allowing access to all (software accessible) device features. The Device Driver Programming Interface (DDPI) utilizes the HPI to provide an interface closer to a device driver's requirements. The software is designed to be easily portable across operating systems and hardware system architectures. Figure A-1 illustrates, conceptually, the CX29610 software architecture.

Figure A-1. Conceptual Software Architecture



The CX29610 software features are:

- Device initialization, configuration, management, and shutdown capabilities.
- Full device feature support.
- Modular software architecture.
- Portable across Operating Systems.
- Embedded software friendly ANSI C implementation.
- Supports multiple CX29610 devices.
- Maintains applicable SONET/SDH MIB/RFC 2558 statistics.

A.1 HPI Overview

The HPI layer performs these key functions:

- Device initialization, configuration, and shutdown
- SONET/SDH Section, Line, and Path overhead management
- Error insertion
- Loopback configuration
- Status and Interrupt processing
- Counter retrieval

The HPI provides complete device functionality yet abstracts the HPI user from the register details and bit manipulation.

A.1.1 Device Initialization, Configuration, and Shutdown

The CX29610 device is highly flexible and configurable. The initialization component of the HPI provides a simple and efficient means of initializing the device to a default state.

The configuration component of the HPI allows the user to configure the device in any of the supported modes of operation.

It should be noted that certain configurable features of the device can be enabled or disabled during run time, while others should not be configured at any time other than during the initialization process.

A.1.2 SONET Overhead Management

The CX29610 device provides extensive SONET/SDH overhead processing capabilities. The CX29610 HPI allows the user to use these capabilities for Section, Line, and Path overhead processing, as well as error insertion and other capabilities.

A.1.3 Status and Interrupt Processing

The CX29610 HPI allows the user to configure interrupts and process received interrupts indicators. The HPI accommodates polling of status registers.

A.1.4 Error Insertion

The CX29610 allows the user to inject various types of errors into the following transmitted SONET overhead bytes: A1, B1, B2, B3, M1 and G1.

A.1.5 Loopback Configuration

The CX29610 HPI allows the user to enable and disable Source and Line loopbacks on the device.

A.1.6 Counter Retrieval

The CX29610 HPI provides primitives to retrieve section, line, and path counter values. The HPI performs all necessary register operations to retrieve the complete counter values, not just the high, medium, or low register byte value.

A.1.7 Register Mirrors

On some system architectures the operation of reading across buses can be slow. This can affect the performance of other devices on the system.

Therefore to minimize the impact of reading CX29610 registers on other devices, the CX29610 HPI can be compiled with a software mirror that is used to store the values of those CX29610 registers which do not change under normal conditions. Having a local copy of the register value reduces the expensive bus read operations. Those device registers that may change during normal operations (i.e., counters and status registers are not mirrored and therefore have to be read each time).

A.2 DDPI Overview

The CX29610 DDPI layer performs these key functions:

- Aggregates HPI primitives to provide device driver type primitives.
- Device initialization, configuration, and shutdown capability.
- SONET/SDH Overhead, Status, and Interrupt processing.
- Maintains applicable SONET/SDH RFC 2558 MIB statistics and counters.

The purpose of the DDPI is to simplify the initialization, configuration and utilization of the CX29610 device. The DDPI further abstracts the device use from the specific hardware details.

The DDPI layer incorporates the HPI primitives to create a smaller interface of primitives that is suited for use by a device driver wrapper layer. Internal to each DDPI primitive, the DDPI layer sequences the required HPI calls to perform the required operation.

A.2.1 Device Initialization, Configuration, and Shutdown Capability

The DDPI is responsible for initialization, configuration, management, event processing and shutdown of the CX29610 device.

The DDPI provides an initialization primitive to put the specified CX29610 device into a default state. The default state may be altered according to the specified parameters. It is possible to initialize the CX29610 device in a different sequence. However, by using the DDPI the initialization is performed in a known, consistent, and controlled fashion.

After initialization, the device may require additional configuration. Because some configuration may only occur during initialization, the DDPI ensures the device is not put in an invalid operational condition.

A.2.2 SONET Overhead, Status and Interrupt Processing

The CX29610 DDPI primitives can be found in the CX29610 Software Driver Package (CX29610DRV OptiPHY™).

A.2.3 Statistics and Counter Retrieval

The DDPI is responsible for managing the statistics gathering and counter processing for the support of the SONET/SDH Interface MIB (RFC 2558). This is achieved by collecting the appropriate counter values and status from the device each second. These are processed in-order to maintain the object identifiers defined in the MIB. Only those object identifiers supported by the device can be supported. VT related objects are therefore not supported. In addition to the MIB statistics, raw counter values are accessible through the DDPI.

A.3 General CX29610 Software Features

The following features are applicable across both the HPI and DDPI software.

A.3.1 Portability

The software is portable across operating systems and hardware. This is done using C macros to abstract the dependencies from the source code and defining these macros in specific porting header files. This makes porting simpler as the operating system or system specific calls are located in a single file.

A.3.2 Reentrancy

The HPI and DDPI support reentrancy. This is designed to prevent resource contention when two threads are using the HPI or DDPI.

A.3.3 Error codes

If either the HPI or DDPI determines incorrect parameters have been passed or an invalid situation has occurred in the software, the particular software layer will return an error code to the software layer above. The CX29610 software has a rich error logging library to aid the debugging and diagnoses of these problems.

A.3.4 Integration and Performance Friendly

The CX29610 software employs a compile-time option to validate received parameters.

Typically, software integration involves eliminating the passing of invalid parameters to functions. The CX29610 HPI and DDPI software provides stringent parameter checks to identify these problems. The return of an error code indicates that an error is detected. After integration and confidence has been obtained, these parameter check routines may be removed by excluding the compile time flag. This ensures run-time performance is not affected by this debug code.

A.3.5 Multiple Device Support

The HPI and DDPI software supports multiple CX29610 devices.

A.3.6 Common libraries

To improve code re-use and reliability, the HPI and DDPI software uses a series of C function libraries for lists, error log mechanisms, string handling, etc. These libraries are included in the software package.

Appendix B : Related Standards

The following is a list of standards relevant to the CX29610.

- *Bellcore Specification T1S1/92-185*
- *Bellcore Spec. GR-253-CORE: Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, Issue 1, Dec. 1994*
- *ITU Recommendation G.707, "Network node interface for the synchronous digital hierarchy (SDH)," 1996*
- *ITU Recommendation G.709, "Synchronous Multiplexing Structure," 1990*
- *ANSI T1.105: Synchronous Optical Network (SONET)—Basic Description Including Multiplex Structure, Rates and Formats, 1995*

All of these documents can be obtained from the following companies:

Bellcore
Customer Service
8 Corporate Place - Room 3C-183
Piscataway, NJ 08854-4156
1-800-521-CORE

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
1-800-433-5177
1-503-797-4207

For ITU documents:

Omnicom
Phillips Business Information
1201 Seven Locks Road,
Suite 300
Potomac, MD 20854
1-800 OMNICOM (666-4266)
New York, NY 10036
1-212-642-4900

MINDSPEED™

www.mindspeed.com

General Information:
(949) 579-3000
Headquarters - Newport Beach
4000 MacArthur Boulevard
Newport Beach, CA. 92660