ADC-44d

Multi-Function Analogue Input/Output Card

User Manual

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User Manual

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OUTLINE DESCRIPTION 1

SPECIFICATION 2
- Analogue Inputs 2
- Analogue Outputs 3
- Digital Input/Output 4
- Timers 5
- Board Connectors 5
- Electromagnetic Compatibility (EMC) 6
- EMC Specification 7

QUICK INSTALLATION 8
- Base Address 8
- Interrupts 8
- DMA Settings 9
- Analogue Input Range 9
- Fitting the Card 10

USING THE CARD 11
- External Input/Output Connections 11
- Analogue Connections 12
- Digital Connections 13
- Analogue Inputs 14
- Input Scaling 15
- Analogue Voltage Outputs 16
- Analogue Current Outputs 17
- Selecting the Load Resistor/Supply Voltage 17
- Typical Connections 19

OPERATION OF THE CARD 20
- Programmable Digital Input Output 20
- Control Code Table 21
- Timer 22
- Timer Modes 23
- ADC Section 24
- ADC Operating Modes 24
- DAC Section 27

MAPS AND REGISTERS 29
Card Address Map 29
DAC Control Register 30
ADC Control Register 31
ADC Gain Select Table 31
ADC Start Convert Mode Table 31
Status Register 32
Mask 0 Control Register 32

SAMPLE PROGRAM DESCRIPTIONS 33
QBASIC Examples 33
'C' Examples 34

DETAILED CARD INSTALLATION 35
Base Address 35
Interrupts 37
DMA Settings 38
Analogue Input Range 39
Fitting the Card 40

CARD LAYOUT 41

APPENDIX A - NUMBERING SYSTEMS 43
Binary and Hexadecimal Numbers 43
Base Address Selection 46

APPENDIX B - PC MAPS 47
PC/XT/AT I/O Address Map 47
PC/XT Interrupt Map 48
PC/AT Interrupt Map 49
DMA Channels 49

APPENDIX C - HOW TO USE DMA 50
The DMA Controller 50
The DMA Controller Registers 52
Mode Register 52
Mask Register 54
Status Register 54
Clear Byte Pointer Flip Flop 55
DMA Transfer Start Address 55
Transfer Length 55
Page Register 55
Addressing 56
DMA Limitations 57
Programming Example 57

OUTLINE DESCRIPTION

The ADC-44d is a PC-compatible short card which provides digital inputs and outputs, timers, analogue inputs and analogue outputs.

There are 24 TTL compatible programmable digital input/outputs available externally. There are also three programmable timers. Two of the timer outputs are available externally to the user and may be gated by external circuitry. The third timer acts as a prescaler to the other two.

Analogue inputs may be either sixteen single-ended or eight differential signals. The input ranges from ±50 mVolts to ±10 Volts for a full scale reading. Input resolution is 12 bits.

There are four analogue outputs available as ±10 Volts and 0 to +20 mA (corresponding to a voltage output range of 0 to +10 Volts) simultaneously. Output resolution is 12 bits.

Analogue conversions (input or output) may be made under programmed I/O control, interrupt control or DMA control. The timers may be used to control the rate of operation if required.

DMA data transfers for both the analogue inputs and outputs may operate simultaneously, thereby providing a constant stream of input and output data with little program intervention.

SPECIFICATION

Analogue Inputs

Analogue Input Channels	16 (Single Ended) 8 (Differential)
Full Scale Input Ranges	± 10.0V, ± 5.0V, ± 2.5V, ±500mV, ±100mv, ± 50mv
Input Common Mode Range	±15 Volts Maximum
Programmable Gains	x1, x2, x10, x100
Pre-Set Link Gain	x1, x½
ADC Conversion Time	3µS
Maximum Data Throughput	100 KHz
Resolution	12 Bit

Accuracy @ 25ºC, Gain x1, Single Ended Input:-

Unipolar 0 To +5 V Range	±0.2% FS + 4 Bits
Bipolar ±5 V Range	±0.2% FS + 4 Bits

Data Transfer Modes	I/O Port or DMA
Data Ready Flags	Interrupt, Status Register or DMA Request
DMA Channels Supported	1 and 3
Interrupt Channels Supported	2 to 7

Analogue Outputs

Analogue Outputs	4
Resolution	12 Bit Monotonic
Voltage Outputs	±10 Volts @ 10mA max. one O/P, or 5mA each from all O/Ps
Current Outputs	0 to +20mA (Corresponding to 0 to 10 Volt output).
Output Error:	
Volts	0.5% of Span
Current	2% of Full Scale
Output Settling Time	3µS to ±1 LSB
Data Transfer	I/O Port, Interrup, or DMA
DMA Channels Supported	1 and 3
Fastest DMA Transfer Rate	12µS per Transfer
Channel Selection	Any or all channels may be selected to be updated
DMA Transfer Initialisation	Programmable Timer, or I/O
Maximum Time Skew	
Channel 1 to Channel 4	48µS
Between Channels	12µS
DMA Timing Source	Fixed or On-board Programmable Timer

Digital Input/Output

Number of Channels	24

Digital Inputs

High Level Input	2.2 Volts minimum
Current	10µA sink
Low Level Input	0.8 Volts maximum
Current	10µA source

Digital Outputs

Logic High Voltage	3.5 Volt minimum
Current	400µA source
Logic Low Voltage	0.4 Volt
Current	2.5mA sink

Power Supply Requirements

5 Volt at 900mA. maximum

Timers

Number Of Timer Channels	3
Timer Usage	
Timer 0	Pre-Scales Timer 1 and 2
Timer 1	For Analogue Outputs
Timer 2	For Analogue Inputs
Timer 0	
Resolution	250ns
Minimum Time	500ns
Maximum Time	16ms
Timer 1	
Resolution	500ns
Minimum Time	1µS
Maximum Time	17.5 Minutes
Timer 2	
Resolution	500ns
Minimum Time	1µS
Maximum Time	17.5 Minutes

Board Connectors

PC ISA 8-bit card	
Analogue Signals	50 Way Male ‘D’ Type
Digital Signals	50 Way IDC Male Box Header

Electromagnetic Compatibility (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in a Blue Chip Technology Icon industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements for an industrial environment (Class A product) subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for the industrial environment.

- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.

- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.

- Most EMC problems are caused by the external cabling to boards. With analogue boards particular attention must be paid to this aspect. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple “pig-tail”. Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC.

- If difficulty with interference is experienced the cable should also be fitted with a ferrite clamp as close possible to the connector. The preferred type is the Chomerics clip-on style, type H8FE-1004-AS.

- It is recommended that cables are kept as short as possible, particularly when dealing with low level signals.

- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.

Failure to observe these recommendations may invalidate the EMC compliance.

> Warning
> This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

EMC Specification

A Blue Chip Technology Icon industrial PC fitted with this card meets the following specification:

Emissions:	EN 55022:1995	
	Radiated	Class A
	Conducted	Class A & B
Immunity:	EN 50082-1:1992 incorporating	
	Electrostatic Discharge	IEC 801-2:1984 Performance Criteria B
	Radio Frequency Susceptibility	IEC 801-3:1984 Performance Criteria A
	Fast Burst Transients	IEC 801-4:1988 Performance Criteria B

QUICK INSTALLATION

Before installing the card into your computer system, there are a number of links which must be set.

The settings of these links will depend upon the computer system into which the card is being fitted. The positions of these links are shown on the circuit board layout diagram towards the end of this manual. Users unfamiliar with the settings of links should refer to the section "Detailed Card Installation". For those unfamiliar with Binary and Hexadecimal numbers, a brief explanation is included in the Appendices.

Base Address

Select an unused I/O address range for the card. The card requires 16 contiguous addresses.

The base address is set on jumper block JP4. Fitting a link is equivalent to a logic "0". Leaving the link open is equivalent to a logic "1". The card is shipped with the default address setting of 300 $_{Hex.}$ This is suitable for most small installations.

Interrupts

The ADC and the DAC can both operate under interrupt control independently. Interrupts IRQ-2 to IRQ-7 are provided. The PIO and the Timer cannot generate interrupts.

The interrupt settings are selected by links on jumper block JP6. Only one link should be fitted for each of the ADC and the DAC. It is not possible to select the same interrupt for both. If interrupt operation is not required leave off the link for the appropriate function.

DMA Settings

The card can transfer data from memory to the analogue outputs, and from the analogue inputs using DMA independently.

The settings are controlled by links on jumper blocks JP7 and JP8. DMA channels 1 and 3 are provided. The ADC and DAC may not use the same channel.

JP7 controls the setting of the DMA Request channels for both ADC and DAC. JP8 controls the setting of the DMA Acknowledge channels. The settings must be the same on both JP7 and JP8. If DMA operation is not required for one or both ADC and DAC, the links are left open.

The appendix contains a section explaining the use of DMA

Analogue Input Range

The input range for the ADC is 50 mV, 100 mV, 500 mV, 1 V, 2.5 V, 5 V, 10 V bipolar (±V) or unipolar (0 to +V) for full scale reading on the ADC. The selection of bipolar or unipolar is controlled by the setting of a link on JP2.

The gain setting is a combination of software control and a jumper block (JP5) which provides a “divide-by-two” function. The following table shows the settings.

FULL SCALE RANGE	PROGRAMMED GAIN	JUMPER JP5 FITTED?
10 Volt	1	Yes
5 Volt	1	No
5 Volt	2	Yes
2.5 Volt	2	No
1 Volt	10	Yes
500 mV	10	No
100 mV	100	Yes
50 mV	100	No

Notice that a full scale input of 5 Volts can be obtained with two different settings.

Be aware also that the software is unaware of the setting of JP5. Therefore when JP5 is fitted the values returned by the ADC will reflect a value of 50% of the actual voltage applied to the inputs. The user must multiply the final value by 2 to obtain the correct reading if JP5 is fitted.

Fitting the Card

Once all the links have been set, the card can be installed into the host computer.

Observe all safety precautions and anti-static precautions. If possible try and locate the card away from 'noisy' cards such as hard disc controllers, network cards and processor cards.

USING THE CARD

External Input/Output Connections

The ADC-44d has two connectors for external circuitry.

The analogue input and output signals are available at a standard 50 pin D-type connector which protrudes through the end bracket of the printed circuit board.

The digital input output signals including those of the timers, are presented on a 50 way IDC header at the inner end of the printed circuit board. These signals may be brought to a suitable connector on the rear cover of the PC using a 50 way ribbon extension cable.

Analogue Connections

The following table shows the pin out of the D-type analogue connector CON2. The pins are arranged in three rows.

Pin	Signal Single	Signal Differl	Pin	Signal	Pin	Signal
1	+Vin0	-Vin0	18	Vin 0v	34	Vout 0v
2	+Vin1	-Vin1	19	Iout0	35	Vin 0v
3	+Vin2	-Vin2	20	Iout+	36	Vin 0v
4	+Vin3	-Vin3	21	Iout1	37	Vin 0v
5	+Vin4	-Vin4	22	Iout+	38	Vin 0v
6	+Vin5	-Vin5	23	Iout2	39	Vin 0v
7	+Vin6	-Vin6	24	Iout+	40	Vin 0v
8	+Vin7	-Vin7	25	Iout3	41	Vin 0v
9	+Vin8	+Vin0	26	Iout+	42	Vin 0v
10	+Vin9	+Vin1	27	Vout0	43	Vin 0v
11	+Vin10	+Vin2	28	Vout 0v	44	Vin 0v
12	+Vin11	+Vin3	29	Vout1	45	Vin 0v
13	+Vin12	+Vin4	30	Vout 0v	46	Vin 0v
14	+Vin13	+Vin5	31	Vout2	47	Vin 0v
15	+Vin14	+Vin6	32	Vout 0v	48	Vin 0v
16	+Vin15	+Vin7	33	Vout3	49	Ext. 0v
17	Vin 0v	Vin 0v			50	Ext. +v

Key:

Vin “n”	Analogue voltage input channel “n”
Vin 0v	Analogue voltage input 0 Volts
Vout “n”	Analogue voltage output channel “n”
Vout 0v	Analogue voltage output 0 Volts
Iout “n”	Analogue current output sink channel “n”
Iout+	Internal connection to pin 50, Ext. +v
Ext. +v	External supply positive for current outputs
Ext. 0v	External supply 0 Volts common.
Single	Single ended mode
Diffl.	Differential mode

See the section “Typical Connections” for examples.

Digital Connections

The following table shows the pin out of the IDC digital signal connector CON1. The pins are arranged in two rows.

PIN	SIGNAL	PIN	SIGNAL
1	DIO Port A, Bit 0	2	DIO Port A, Bit 1
3	DIO Port A, Bit 2	4	DIO Port A, Bit 3
5	DIO Port A, Bit 4	6	DIO Port A, Bit 5
7	DIO Port A, Bit 6	8	DIO Port A, Bit 7
9	DIO Port B, Bit 0	10	DIO Port B, Bit 1
11	DIO Port B, Bit 2	12	DIO Port B, Bit 3
13	DIO Port B, Bit 4	14	DIO Port B, Bit 5
15	DIO Port B, Bit 6	16	DIO Port B, Bit 7
17	DIO Port C, Bit 0	18	DIO Port C, Bit 1
19	DIO Port C, Bit 2	20	DIO Port C, Bit 3
21	DIO Port C, Bit 4	22	DIO Port C, Bit 5
23	DIO Port C, Bit 6	24	DIO Port C, Bit 7
25	Digital 0 Volt Return	26	Digital 0 Volt Return
27	ADC Timer (2) Trigger	28	DAC Timer (1) Trigger
29	Digital 0 Volt Return	30	Digital 0 Volt Return
31	ADC Timer (2) Output	32	DAC Timer (1) Output
33	Digital 0 Volt Return	34	Digital 0 Volt Return
35	Digital 0 Volt Return	36	Digital 0 Volt Return
37	Digital 0 Volt Return	38	Digital 0 Volt Return
39	Digital 0 Volt Return	40	Digital 0 Volt Return
41	Digital 0 Volt Return	42	Digital 0 Volt Return
43	Digital 0 Volt Return	44	Digital 0 Volt Return
45	Digital 0 Volt Return	46	Digital 0 Volt Return
47	Digital 0 Volt Return	48	Digital 0 Volt Return
49	Digital 0 Volt Return	50	Digital 0 Volt Return

Key:

DIO- “x” “n” Digital input/output, Port “x”, Bit “n” of I/O device.
ADC Trigger Control input for Timer 2 (ADC timer)
DAC Trigger Control input for Timer 1 (DAC timer)

See the section “Typical Connections” for examples.

Analogue Inputs

The ADC-44d analogue input circuitry can be software configured to operate with single ended or differential signals.

A single ended input measures the absolute voltage applied to the input channel (e.g. Vin3) with reference to the signal ground connection or 0 Volts (Vin 0v). This is the simplest connection type and suitable in all but the noisiest environments.

With this input configuration the maximum voltage range that the card can measure is ±10 Volts.

> **Note:** Voltages in excess of ± 15V on the input terminals may cause the input devices to become damaged. DO NOT apply voltages greater than this level.

A differential input measures the difference between two input terminals. This configuration provides good noise rejection if measurements are to be made in an electrically noisy environment. When the card is configured in this mode the maximum voltage range on each of the input pairs is ±10 Volts, subject to a maximum of ±10 Volts on any input pin. That is, no pin may exceed ±10 Volts with respect to the analogue 0 Volts.

Each channel in the range 0 to 7 has a corresponding channel in the range 8 to 15. Differential inputs are applied to the corresponding pairs,
e.g. between +Vin0 and -Vin0, or between +Vin1 and -Vin1, etc. Note that +Vin0 in differential mode is +Vin8 in single ended mode.

Input Scaling

The ADC-44d gain can be selected by software and by the use of a link. The link selects x1 or x½ ranges. The programmable gains may be set to x1, x2, x10, x100. In combination these provide the capability to measure the following full scale input voltages:-

±10 Volts, ±5 Volts, ±2.5 Volts,
±500 mV, ±100 mV and ±50 mV.

The selection of a particular gain will depend upon the application for which the card is being used. When using the 50mV full scale input, special care should be exercised in shielding input cables against spurious noise and the use of a differential input configuration is recommended.

Note that the computer is *not* aware of the setting of the link. If this is set to x½, the actual input to the ADC is half that applied to the card input. It is this voltage that the ADC indicates not the input voltage. The *user* must multiply the output value by 2 to get the true input voltage.

Analogue Voltage Outputs

The analogue output signals from the ADC-44d are available as voltages and current sinks simultaneously.

Each of the four output signals (Vout0 to Vout3) has a corresponding analogue ground or 0 Volt connection. The voltage outputs are referenced to these connections. Measuring output voltages with reference to other ground points (particularly the digital ground) will give electrically noisy results.

The voltage output has a span from +10 Volts to -10 Volts with an output drive of 10mA maximum for any single output and 5mA maximum each for all outputs simultaneously.

If large capacitive loads are to be connected to the voltage output, it is recommended that a series resistance of approximately 100 ohms is placed in series with the output voltage to avoid oscillations occurring at the output.

All outputs are disabled following a power on and will be set to 0 Volts and 0 mA. Writing 0 to the DAC control register bit 2 at address Base + 1, or issuing a master reset (a read from Base + 0) will also disable the outputs.

This is a safety feature and also allows the outputs to be pre-set to a specific value prior to enabling them. This is accomplished by writing a logic 1 to bit 2 of the DAC control register.

Analogue Current Outputs

Four current outputs are available corresponding to the four voltage outputs. The outputs sink current from an external power supply provided by the user. Additional pins are provided at the output connector to facilitate the external wiring.

The current sinks 0 to 20mA through an external load. The output current range of 0 to +20 mA corresponds to a voltage output of 0 to +10 Volts at the equivalent voltage output pin. The output current is 0mA for a voltage output of -10 Volts to 0 Volts.

The user must provide an external supply voltage for the current outputs. The voltage for this supply should be +4 Volts minimum to +24 Volts maximum.

> **NOTE:** Supplies greater than 24 Volts may cause serious damage to the card.

Selecting the Load Resistor/Supply Voltage

The output current drivers require an absolute minimum of 2 Volts at the output terminals to function correctly. The value of load resistor in ohms for a given supply voltage may be calculated from the following formula:

$$R_{load} = [V_{supply} - 2] \times 50$$

Load resistances less than the calculated value may be used.

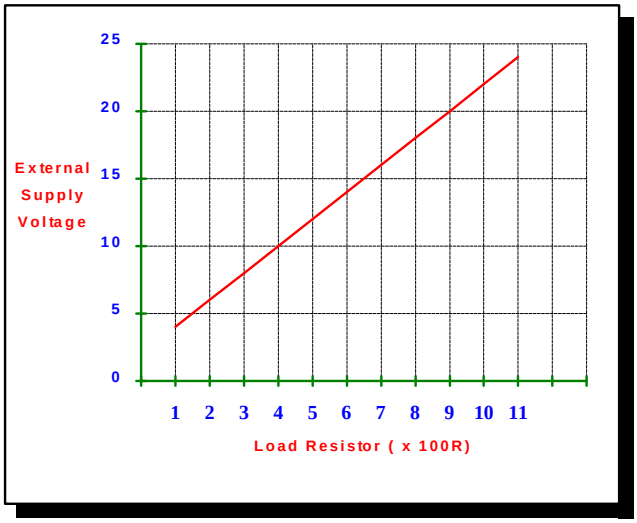
To calculate the minimum supply voltage required for a known value of load resistance, use the following equation:

$$V_{supply} = [0.02 \times R_{load}] + 2$$

Voltages in excess of the calculated minimum may be used up to the maximum of 24 volts.

External voltages of less than 4 Volts, and external loads of less than 100 ohms are not recommended.

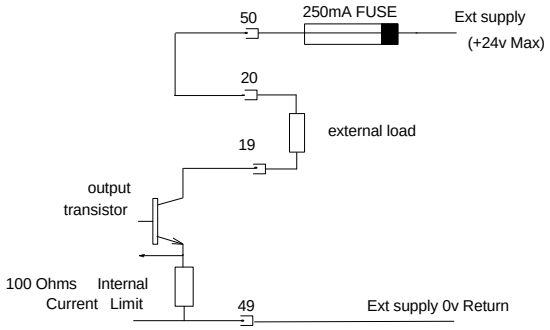
As a guide the graph below can be used to determine load resistor values and supply voltages



Typical Connections

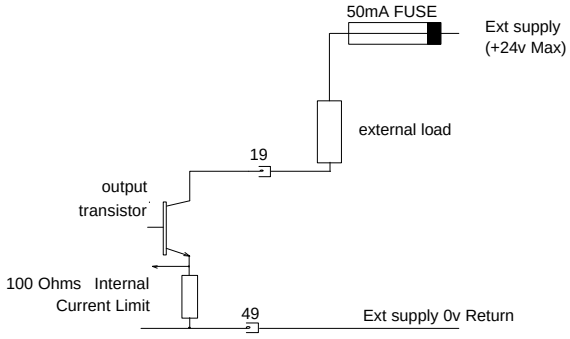
The following two diagrams illustrate the method of connection.

The first shows the use of the internal connections to wire the external loads directly to the output connector. Note that pin 50 is a single common supply pin internally linked to pins 20, 22, 24 and 26. Pin 49 is a single common supply return pin.



Note the use of a fuse to protect the circuitry.

The second diagram shows an individual load connected directly to the power supply. Again the use of a fuse is recommended.



OPERATION OF THE CARD

Programmable Digital Input Output

The ADC44d includes an NEC µPD71055 device which is equivalent to an Intel i8255 PIO.

This device provides 24 programmable digital I/O channels. It is suitable for sensing the presence of, or driving TTL connections only.

The digital I/O appears to the PC as four ports. The first three can be set as input or output by writing suitable codes to the fourth Control Port.

These four ports are mapped into the ADC44d port map as follows:

ADDRESS	PORT	READ/WRITE
Base + 8	Programmable Digital I/O Port A	R/W
Base + 9	Programmable Digital I/O Port B	R/W
Base + 10	Programmable Digital I/O Port C	R/W
Base + 11	Control Port	W

A typical sequence of events to use this feature would be :

- Decide on the input/output mix and write the appropriate code to BASE + 11.

- Read from the selected output port or write to the selected output port.

Control Code Table

The µPD71055 can operate in one of three modes.

The first mode (Mode 0) provides simple I/O for three, 8 bit ports. Data is written to or read from a specified port (A, B, or C) without the use of handshaking.

The following table gives a summary of the most commonly used 'Control Words' which must be written to the control port to configure the D71055 I/O ports in Mode 0.

Control Word (Hex)	**Control Word** (Decimal)	**Set all of Port A as**	**Set all of Port B as**	**Set high 4 bits of C as**	**Set low 4 bits of C as**
80	128	Output	Output	Output	Output
81	129	Output	Output	Output	Input
82	130	Output	Input	Output	Output
83	131	Output	Input	Output	Input
88	136	Output	Output	Input	Output
89	137	Output	Output	Input	Input
8A	138	Output	Input	Input	Output
8B	139	Output	Input	Input	Input
90	144	Input	Output	Output	Output
91	145	Input	Output	Output	Input
92	146	Input	Input	Output	Output
93	147	Input	Input	Output	Input
98	152	Input	Output	Input	Output
99	153	Input	Output	Input	Input
9A	154	Input	Input	Input	Output
9B	155	Input	Input	Input	Input

Mode 1 enables the transfer of data to or from a specified 8 bit port (A or B) in conjunction with strobes or handshaking signals on port C.

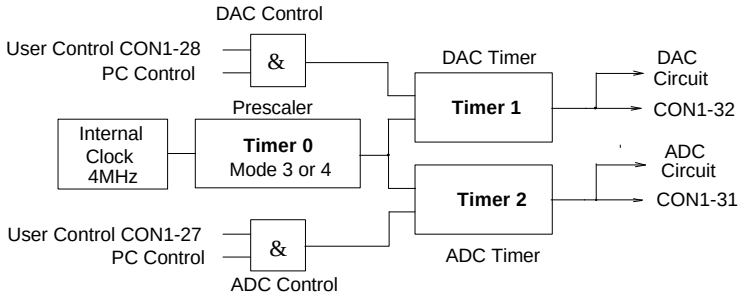
In Mode 2, data is transferred via one bi-directional 8 bit port (A) with handshaking (port C). Refer to the µPD71055 or i8755 data sheet for full details of the settings and use of Modes 1 and 2.

Timer

The ADC-44d includes an NEC µPD71054 timer chip which is equivalent to an Intel i8254.

The timer chip contains three independent 16 bit counters which may be operated in different modes. There are five basic modes of operation with each mode providing a different output signal from the three output pins of the device.

On the ADC-44d, Timer 0 is used as a prescaler and may only be used free running in mode 3 or 4. Timers 1 and 2 are connected to the output of the prescaler. This allows the DAC and the ADC to have up to a 17.5 minute interval between updates.



Block Diagram of timer connections

Timer 1 is used for transfers involving the DAC whilst Timer 2 is used for transfers involving the ADC.

The reference clock for the timer is 4MHz. The output rate of the prescaler is 4MHz divided by the pre-loaded Timer 0 counter value.

The output rate from Timer 1 and Timer 2 is the prescaler output divided by the pre-loaded timer counter value.

The timer circuit appears to the PC as four ports.

These four ports are mapped into the ADC44d port map as follows:

ADDRESS	PORT	READ/WRITE
Base + 12	Timer/Counter 0	R/W
Base + 13	Timer/Counter 1	R/W
Base + 14	Timer/Counter 2	R/W
Base + 15	Control port	W

Timer Modes

The timers have five modes of operation. Only Modes 3 and 4 are described for the prescaler. Refer to the data sheet of the µPD71054 or i8254 for a more detailed description.

Mode 3

When programmed in this mode the output pin will toggle each time the count register decrements to its base level from the value programmed into it. If the count value loaded is an odd number then the counter will reach zero before the output pin toggles. The programmed value is automatically reloaded.

This mode therefore acts as a frequency divider with an approximate 1:1 mark-space ratio.

Mode 4

In this mode the output pin pulses when the count reaches zero.

ADC Section

The Analogue to Digital converter is accessed as four ports.
The four ports are mapped into the PC at the following addresses:

ADDRESS	FUNCTION	READ/WRITE
Base + 3	Read ADC Data, low 8 bits on first read, high 4 bits on second read	R
Base + 4	Write ADC Control word	W
	Read resets the control logic to pre-defined state	R
Base + 5	ADC start conversion, write to this port starts conversion in I/O mode	W
Base + 6	Channel select, upper 4 bits set the input channel number	W
	ADC Status, bit 0 is high when ADC is performing a conversion	R

An interrupt may be generated at the end of every conversion if required.

ADC Operating Modes

The ADC section can operate in one of three modes:

by individual I/O read/write operations;
by automatic re-trigger, or;
by timer control.

The modes are set by writing to the upper 2 bits of the ADC CONTROL register at address Base + 4 (see MAP and REGISTER section for details).

> **Note** - When changing modes it is necessary to issue an ADC reset instruction (Read Base + 4) 10µS after the mode change. This allows the ADC device time to finish an internal cycle (if any) before clearing the busy bit. Reading port Base + 4 resets the ADC internal control logic only. It does not clear the ADC control register bits.

In its simplest mode an ADC cycle is triggered by writing to Base + 5 with bits 6 and 7 of the ADC CONTROL register set to zero (default condition).

A typical sequence of events to acquire data in this mode would be:

- Select the mode by writing the value 0 to bits 3 to 7 of Base + 4.
- Set the input gain and type by writing to bits 0 to 2 of Base + 4.
- Write the required input channel number to the upper 4 bits of Base + 6.
- Start the conversion with a write to Base + 5.
- Monitor bit 0 of Base + 6 (ADC BUSY) until it goes LOW indicating data is available following a conversion cycle.
- Read Base + 3 for the data low byte.
- Read Base + 3 again for the data high byte.

In the second mode set Base + 4 bit 6 high, and bit 7 low and initiate the first conversion by writing to Base + 5. The ADC is then automatically re-triggered when data from the previous sample is read

In the third mode the ADC is re-triggered when Timer 2 overflows. This mode is best used for DMA or INTERRUPT operation. It is selected by setting Base + 4 bit 6 high, and bit 7 high. The sequence would be:

- Select the mode by setting Base + 4 bit 6 high, and bit 7 high.
- Set the input gain and type by writing to bits 0 to 2 of Base + 4.
- Program Timers 0 and 2 to give the required output rate.
- If DMA operation is required program the DMA controller and set bit 4 of Base + 4.
- Enable the Timer output by setting bit 3 of Base + 4.

If DMA is enabled a DMA transfer will be requested on each timer ‘tick’. An interrupt is always generated at this point indicating that data is available. If DMA is not enabled the data must be read before the next timer ‘tick’ occurs.

> **Note**: The GATE input for timer 2 is available on pin 27 of the 50 way IDC connector and returned as data bit 1in the status register. If pin 27 is pulled LOW by an external signal the timer is inhibited. This may be used as a simple hardware trigger.

DAC Section

The Digital to Analogue Converter is accessed as 4 ports. These ports are mapped into the PC at the following addresses.

ADDRESS	FUNCTION	READ/WRITE
Base + 0	Write DAC Output Data, low 8 bits on first write, high 4 bits on second write	W
Base + 1	DAC Control register	W
	Read resets DAC internal control logic. Does not clear the DAC control register bits	R
Base + 2	Write starts a DAC transfer in DMA mode	W
Base + 6	Bits 0 to 3 enable or disable writes to DAC channel 0 to 3 respectively	W

An interrupt may be generated if required whenever a channel is updated. Note that reading port Base + 1 resets the DAC internal control logic only. It does not clear the DAC control register bits.

The DAC section operates in one of two modes, I/O or DMA.

To output data to the DAC in I/O mode use the following sequence:

- Write 0 to Base + 1 (DAC Control Register).
- Write 0 to Base + 6 to enable all the DAC outputs.
- Write the channel number required into bits 0 and 1 of Base + 1.
- Write the least significant byte of DAC data into Base + 0.
- Write the most significant byte of DAC data into Base + 0.

Switch on the DAC reference to enable the outputs by setting bit 2 of Base + 1.

To operate in DMA mode updating a single channel use the following sequence:

- Program Timers 0 and 1 for the required output rate.
- Program the DMA controller.
- Write $D4_{Hex}$ to Base +1 (Control Register).
- Set the channel number in bits 0 and 1 of Base + 1.
- Start the timer by setting bit 3 high in Base + 1.

Note: As with the ADC, the GATE input for Timer 1 is available on pin 28 of the 50 way IDC connector. If pin 28 is pulled LOW by an external signal the timer is inhibited. This may be used as a simple hardware trigger.

MAPS AND REGISTERS

Card Address Map

BASE + n	R/W	SECTION	FUNCTION
0	W	DAC	Output Data to DAC
	R	ALL	Master Clear - Resets the Card to Default Condition. (All Registers And Control Logic).
1	W	DAC	Output Data to DAC Control Register.
	R	DAC	Reset DAC Control Logic Only.
2	W	DAC	Starts DAC DMA Mode - No Timer
3	R	ADC	Input ADC Data
4	W	ADC	Output Data to ADC Control Register.
	R	ADC	Reset ADC Control Logic Only.
5	W	ADC	Start ADC in DMA or PC Mode
6	W	ADC & DAC	Control Register - ADC Mux & DAC Mask
	R	ADC & DAC	Input Status of ADC & DAC Busy Bits & Channel Addresses
8	R/W	PIO	Digital Input/Output Channels 1 to 8
9	R/W	PIO	Digital Input/Output Channels 9 to 16
10	R/W	PIO	Digital Input/Output Channels 17 to 24
11	W	PIO	Digital Input/Output Control Register
12	R/W	TIMER	Timer 0 Count Register. Prescaler in mode 3 or 4 only
13	R/W	TIMER	Timer 1 Count Register
14	R/W	TIMER	Timer 2 Count Register
15	W	TIMER	Timer Control Register

DAC Control Register

(Base + 1)

DATA BIT	FUNCTION
0	Binary DAC Channel Select 0 to 3
1	Default = Channel 0.
2	0 = DAC 10v reference off, all DAC outputs = 0v. (Default) 1 = Reference on. DAC outputs active.
3	0 = Disable DAC Timer(1) & user control. (Default) 1 = Enable DAC Timer(1) & user control.
4	0 = Select DAC I/O mode. (Default) 1 = Select DMA mode.
5	0 = Manual Channel selection. (Default) 1 = Auto Channel increment.
6	0 = DMA Transfer stops when DMA controller reaches Terminal Count. (Default) 1 = DMA Transfer continues after Terminal Count, (Only if DMA controller is set to auto restart).
7	0 = DAC updated by an I/O Write operation. (Default) 1 = Timer updates DAC

ADC Control Register

(Base + 4)

DATA BIT	FUNCTION
0	ADC Gain Selection Bits
1	See Gain Select Table Below
2	0 = Single 16 Channel I/P (Default) 1 = Differential 8 Channel I/P
3	0 = Disable ADC Timer 2 (Default) 1 = Enable ADC Timer 2
4	0 = ADC in I/O Mode (Default) 1 = DMA MODE
5	0 = Manual Channel Select (Default). 1 = Auto Channel Increment
6	ADC Mode Bits 0 and 1
7	See Table Below For Modes

ADC Gain Select Table

Bit 1	Bit 0	PROGRAMMED GAIN
0	0	x 1 (Default)
0	1	x 2
1	0	x 10
1	1	x 100

ADC Start Convert Mode Table

Bit 7	Bit 6	MODE	ACTION
0	0	I/O	I/O Start Convert begins each conversion (Default).
0	1	I/O Auto Start	I/O Start Convert begins the first conversion, each subsequent read of the two data bytes begins a new conversion automatically.
1	0	Illegal	
1	1	Timer	Timer output begins each new conversion.

Status Register

(Base + 6 Read)

DATA BIT	FUNCTION
0	ADC Busy Bit. 0 = Conversion complete. 1 = Conversion in progress (incomplete).
1	External ADC Timer Enable Status Bit 0 = Timer Disabled. 1 = Timer Enabled. (Default)
2	ADC Channel Selection Bits (Binary 0 to 15)
3	
4	
5	
6	DAC Channel Selection Bits (Binary 0 to 3)
7	

Mask 0 Control Register

(Base + 6 Write)

DATA BIT	FUNCTION
0	DAC Channel Mask Bits Controls which of the four DAC output channels are updated. 0 = DAC Output is updated (Default). 1 = DAC Output is not updated
1	
2	
3	
4	Manual ADC Channel Selection Bits (0 to 15 binary) Default = Channel 0
5	
6	
7	

NOTE: Although any or all channels can be disabled, if the channel scanning is enabled, all channels are presented with data from the DMA array as if they were active. The internal write signal is switched off for the particular channels that are inhibited. This allows a channel or channels to be set to a particular output value and then left in that state whilst continuing to update the remaining channels via DMA.

SAMPLE PROGRAM DESCRIPTIONS

The disk supplied with the card contains several example programs to demonstrate the various operating modes.

QBASIC Examples

EXAMPLE1.BAS

Demonstrates the simplest I/O mode to read all 16 ADC input channels.

EXAMPLE2.BAS

Demonstrates the AUTO START CONVERT mode and sets the channel scanner to read all 16 input channels.

EXAMPLE3.BAS

Demonstrates the simple I/O mode to output a sine wave to all 4 analogue output channels.

EXAMPLE4.BAS

Demonstrates reading and writing to the digital I/O.

'C' Examples

EXAMPLE6.C

Demonstrates reading the ADC on a single channel using DMA and the on board timer.

EXAMPLE7.C

Demonstrates writing to a single DAC channel using DMA and the on board timer.

EXAMPLE8.C

Demonstrates writing to multiple DAC channels using DMA the on board timer.

EXAMPLE9.C

Demonstrates reading multiple ADC channels using interrupts and the on board timer.

DETAILED CARD INSTALLATION

Before installing the card into your computer system, there are a number of links which must be set. The settings of these links will depend upon the computer system into which the card is being fitted.

The positions of these links are shown on the card layout diagram towards the end of this manual

Base Address

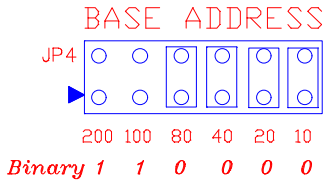
The card may be located in any 62 pin slot in the PC motherboard but must be set up to appear at a specified address in the I/O port map. Available positions are shown in the IBM-PC Technical Reference Guide. However, for those who do not possess a copy of this document, a good place is the location normally allocated to the prototyping card as supplied by IBM. This address is 300 $_{Hex}$ which is the factory default setting.

No two devices should be set to the same address since contention will occur and neither card will work. If your machine contains a card with a conflicting address then another reasonably safe address to use is 200 to 21F $_{Hex}$.

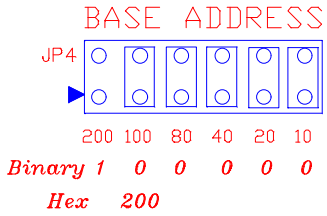
A set of links are provided on the card to set the base address within the IBM-PC I/O port map. The address is in binary with the presence of a link representing a 0 and the absence of a link representing a 1.

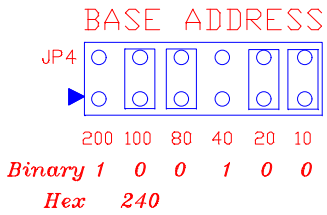
To set the base address to 300 $_{Hex}$, locate the jumper block JP4 labelled Base Address.

Set the following pattern on the links whilst viewing the card with Connector CON2 on right hand side and the gold fingers to the lower edge.:-



Other examples are:





Interrupts

An interrupt to the computer may be generated by the ADC and by the DAC.

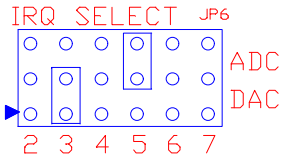
The ADC generates an interrupt signal at the end of a conversion when the data is available for the processor. This allows the program to do other tasks after starting a conversion without having to wait for data to become available.

The DAC generates an interrupt signal after the output has been updated.

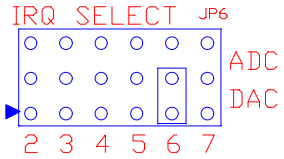
The interrupts are selected on jumper block JP6.

A link is added to the block in the ADC row if ADC interrupts are required, and similarly a link is added to the DAC row if DAC interrupt are required. If interrupts are not required, the links are not fitted.

The diagram below shows the ADC set to produce an interrupt request IRQ5, and a DAC interrupt request IRQ3.



The second example shows the block settings if the DAC generates interrupt request IRQ6, but an interrupt is not required from the ADC.



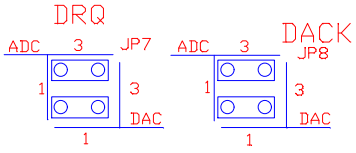
Notice that the ADC and the DAC cannot generate the same interrupt. Only one interrupt of each type (ADC or DAC) should be selected. It is not permissible for, say the ADC to generate IRQ2 and IRQ5.

DMA Settings

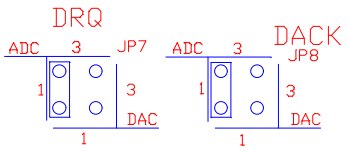
The DMA selection is set on two sets of jumper blocks, JP7 and JP8.

JP7 controls which channel the ADC and DAC use to request Direct Memory Access. Only channels 1 and 3 are available. Jumper JP8 sets the channel on which the DMA controller acknowledges the request. It is essential that the pattern of links on the two jumper blocks correspond.

The example below shows the link settings for the ADC to generate DMA request DRQ3 and receive acknowledgement on DACK3, and the DAC to generate DRQ1 and receive DACK1.



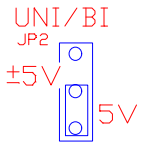
If DMA operation is not required the links are not fitted. The example below shows the ADC generating DRQ1 and receiving DACK1 in return, but no DMA operation from the DAC.



Analogue Input Range

The ADC inputs may be unipolar, meaning they may range from zero to some positive value (e.g. 0 to +5 Volts), or bipolar meaning that it ranges from a negative value to an equal and opposite positive value (e.g. -10 Volts to + 10 Volts, shown as ±10 Volts). This selection is set by a link on jumper block JP2.

The diagram below shows the jumper set for unipolar operation.



It is essential that a link is fitted to one or other of the positions on jumper block JP2.

The gain setting is a combination of software control and a jumper block (JP5) which provides a “divide-by-two” function. The following table shows the available ranges and settings.

FULL SCALE RANGE	PROGRAMMED GAIN	JUMPER JP5 FITTED ?
10 Volt	1	Yes
5 Volt	1	No
5 Volt	2	Yes
2.5 Volt	2	No
1 Volt	10	Yes
500 mV	10	No
100 mV	100	Yes
50 mV	100	No

Notice that a full scale input of 5 Volts can be obtained with two different settings. It is also important to note that the software cannot be aware of the setting of JP5. When JP5 is fitted the values returned by the ADC will reflect a value of only 50% of the actual voltage applied to the inputs. The user must multiply the final answer by 2 to obtain the correct reading if JP5 is fitted.

Fitting the Card

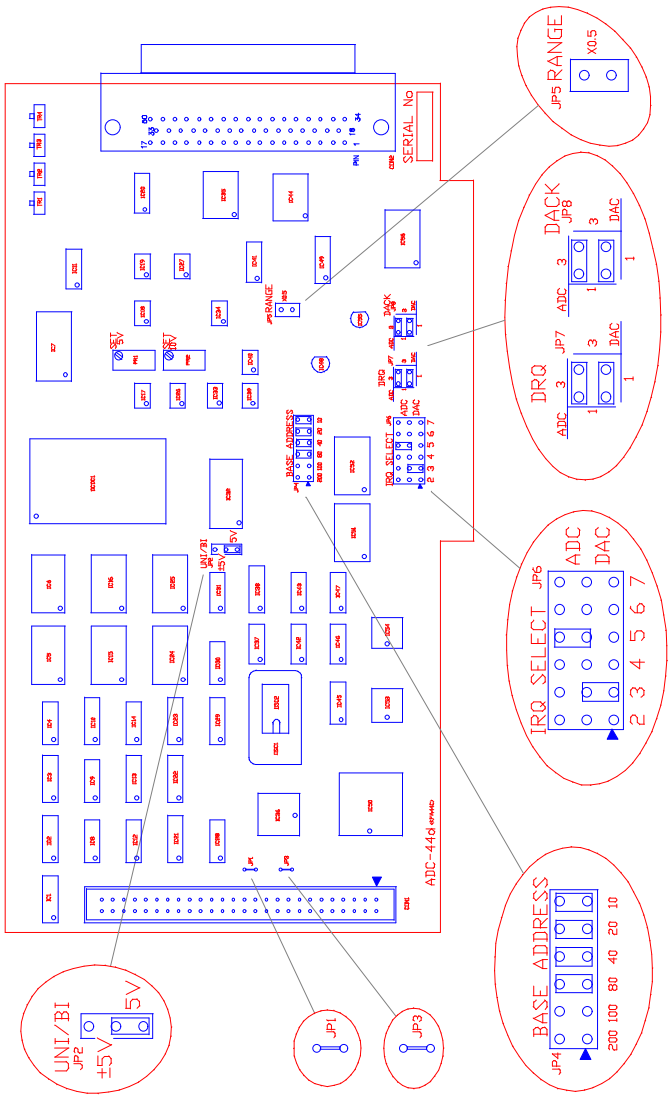
Once all the links have been set, the card can be installed into the host computer.

First and foremost ensure that the power is turned off at the supply. Carefully follow all of the manufacturer's instructions for opening the computer. Locate a free expansion slot in the machine, and remove the blanking plate for that slot. If possible try to locate the card away from “noisy” cards such as hard disk controllers, network cards and processor cards.

You should observe normal anti-static precautions. Remove the card from its anti-static bag, and holding the card only by the edges and the metal bracket, plug the card firmly into the slot. Screw the bracket in place and re-assemble the computer.

Run one of the test programs to verify the operation of the card.

CARD LAYOUT



APPENDIX A - NUMBERING SYSTEMS

Binary and Hexadecimal Numbers

The normal numbering system is termed DECIMAL because there are ten possible digits (0 to 9) in any single column of numbers. Decimal numbers are also referred to as numbers having a Base 10. When counting, the numbers increment in the units column from 0 up to 9. The next increment resets the units column to 0 and carries over 1 into the next column. This 1 indicates that there has been a full ten counts (the base number) in the units column. The second column is therefore termed the “tens” column.

It is more convenient when programming to use a number system that provides a clearer picture of the hardware at an operational or register level. The two most common number systems used are BINARY and HEXADECIMAL. These two systems provide an alternative representation to decimal numbers.

For a binary number there are only 2 possible values (0 or 1) and as a result binary numbering is often known as Base 2. When counting in binary numbers, the number increments the units column from 0 to 1. At the next increment the units column is reset to 0 and 1 is carried over to the next column. This column indicates that a full two counts have occurred in the units column. Now the second column is termed the “twos” column.

Hexadecimal numbers may have 16 values (0 to 9 followed by the letters A to F). It is also known as a system with the Base 16. With this counting system the units increment from 0 to 9 as with the decimal system, but at the next count the units column increments from 9 to A and then B, C and so on up to F. After F the units column resets to 0 and the next column increments from 0 to 1. This 1 indicates that sixteen counts have occurred in the units column. The second column is termed the “sixteens” column.

The following table shows how the three systems indicate successive numbers

Decimal Base 10		Binary Base 2					Hexadecimal Base 16	
0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	1
0	2	0	0	0	1	0	0	2
0	3	0	0	0	1	1	0	3
0	4	0	0	1	0	0	0	4
0	5	0	0	1	0	1	0	5
0	6	0	0	1	1	0	0	6
0	7	0	0	1	1	1	0	7
0	8	0	1	0	0	0	0	8
0	9	0	1	0	0	1	0	9
1	0	0	1	0	1	0	0	A
1	1	0	1	0	1	1	0	B
1	2	0	1	1	0	0	0	C
1	3	0	1	1	0	1	0	D
1	4	0	1	1	1	0	0	E
1	5	0	1	1	1	1	0	F
1	6	1	0	0	0	0	1	0
1	7	1	0	0	0	1	1	1
1	8	1	0	0	1	0	1	2
1	9	1	0	0	1	1	1	3
2	0	1	0	1	0	0	1	4

Notice how the next higher column does not increment until the lesser one to its right has overflowed.

Binary representation is ideally suited where a visual representation of a computer register or data is needed. Each column is termed a BIT (from **B**inary dig**IT**). Only five Bits are shown in the above table. With larger numbers, more Bits are required. Normally Bits are arranged in groups of eight termed BYTES. By definition there are 8 BITS per BYTE. Each Bit (or column) has a value. In the binary table above the rightmost or least significant column each digit has a value of 1. Each digit in the next column has a value of 2, the next 4, then 8 and so on.

The following diagram illustrates this.

BIT No	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1

To determine the decimal value of a binary pattern, add up the decimal number of each column containing a binary "1".

BIT No	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1
BINARY NUMBER	1	1	0	0	0	1	1	0

The above example shows the binary pattern that is equivalent to 198 $_{Decimal}$.

The binary string defining a Byte can be unwieldy. To make it less error prone, the 8 bits forming a byte are divided into two groups of 4 bits, known as NIBBLES. With four bits there are 16 possible numeric combinations (including zero). A convenient method of representing each nibble is to use the hexadecimal base 16 system.

When converting binary to hex, the byte is divided into nibbles each represented by a single hex digit. This technique is applied to the selection of the base address for the circuit board. The following diagram illustrates the construction of a hex number.

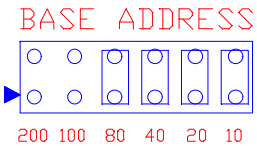
BIT No	7	6	5	4	3	2	1	0
NIBBLE VALUE	8	4	2	1	8	4	2	1
BINARY NUMBER	1	1	0	0	0	1	1	0
	ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÙ				ÀÄÄÄÄÄÄÄÄÄÄÄÄÄÙ			
HEXADECIMAL:	C				6			

Hexadecimal upper nibble = (1 x 8) + (1 x 4) + (0 x 2) + (0 x 1) = 12
lower nibble = (0 x 8) + (1 x 4) + (1 x 2) + (0 x 1) = 6

The resulting value is C6 $_{Hex}$, since 12 $_{Decimal}$ equals C $_{Hex}$.

Base Address Selection

Each column can be physically represented on the board by a pair of pins. In practice, the boards cover a range of addresses (usually $16_{Decimal}$). Therefore the low order four bits are not included, but two higher order bits are added. This gives an address range of 0 to $3F0_{Hex}$. The following diagram shows a typical set of pins.



Here a link is fitted to denote a binary or logic “0”, or left open to indicate a binary or logic “1”. The example shows a base address setting of 300_{Hex}.

APPENDIX B - PC MAPS

PC/XT/AT I/O Address Map

Address	Allocated to:
000-01F	DMA Controller 1 (8237A-5)
020-03F	Interrupt Controller 1 (8259A)
040-05F	Timer (8254)
060-06F	Keyboard Controller (8742) Control Port B
070-07F	RTC and CMOS RAM, NMI Mask (Write)
080-09F	DMA Page Register (Memory Mapper)
0A0-0BF	Interrupt Controller 2 (8259)
0F0	Clear NPX (80287) Busy
0F1	Reset NPX (80287)
0F8-0FF	Numeric Processor Extension (80287)
1F0-1F8	Hard Disk Drive Controller
200-207	Reserved
278-27F	Reserved for Parallel Printer Port 2
2F8-2FF	Reserved for Serial Port 2
300-31F	Reserved
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	Reserved for SDLC Communications, Bisync 2
3A0-3AF	Reserved for Bisync 1
3B0-3BF	Reserved
3C0-3CF	Reserved
3D0-3DF	Display Controller
3F0-3F7	Diskette Drive Controller
3F8-3FF	Serial Port 1

PC/XT Interrupt Map

Number	Allocated to:
NMI	Parity
0	Timer
1	Keyboard
2	Reserved
3	Asynchronous Communications (Secondary) SDLC Communications
4	Asynchronous Communications (Primary) SDLC Communications
5	Fixed Disk
6	Diskette
7	Parallel Printer

PC/AT Interrupt Map

Level	Allocated to:	
CPU NMI		Parity or I/O Channel Check
CTLR 1	CTLR 2	(Interrupt Controllers)
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Interrupt from CTLR 2
	IRQ 8	Real-time Clock Interrupt
	IRQ 9	S/w Redirected to INT 0AH (IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Co-processor
	IRQ 14	Fixed Disk Controller
	IRQ 15	Reserved
IRQ 3		Serial Port 2
IRQ 4		Serial Port 1
IRQ 5		Parallel Port 2
IRQ 6		Diskette Controller
IRQ 7		Parallel Port 1

DMA Channels

0	Memory Refresh
1	Spare
2	Floppy Disk Drive
3	Spare

APPENDIX C - HOW TO USE DMA

Direct Memory Access or DMA is a process by which data can be transferred directly from the memory of the PC into an I/O card or directly from the I/O card into the PC memory with no intervention from the processor. This can greatly increase the throughput of data and at the same time, reduce the overhead of processor time.

The DMA Controller

DMA is controlled by the PC using one of two DMA Controllers. The DMA Controllers are INTEL i8237 or compatible devices, each containing four channels. The first one is used for byte transfers in the bottom 1 MB of system memory, the second can transfer words into the bottom 16 MB.

Blue Chip Technology boards only allow DMA channels 1 or 3 on the first controller to be used. Normally channel 0 is reserved for memory refresh control and channel 2 is used by the floppy disk drives.

In order to begin a DMA transfer, first the I/O board must be configured to enable DMA operation - consult the relevant section of the manual on how to do this. Secondly, the DMA controller must be programmed to begin the transfer. The DMA controller is programmed by writing to I/O ports in much the same way as the card is programmed.

These port locations are fixed for all PCs as follows:-

I/O ADDRESS	READ/ WRITE	DESCRIPTION
0000H	R/W	DMA Channel 0 Current Address
0001H	R/W	DMA Channel 0 Current Word Count
0002H	R/W	DMA Channel 1 Current Address
0003H	R/W	DMA Channel 1 Current Word Count
0004H	R/W	DMA Channel 2 Current Address
0005H	R/W	DMA Channel 2 Current Word Count
0006H	R/W	DMA Channel 3 Current Address
0007H	R/W	DMA Channel 3 Current Word Count
0008H	R/W	Command/Status Register
0009H	R/W	DMA Request Register
000AH	R/W	DMA Single Bit Mask Register
000BH	R/W	DMA Mode Register
000CH	R/W	DMA Clear Byte Pointer
000DH	R/W	DMA Master Clear
000EH	R/W	Clear Mask Register
000FH	R/W	DMA Write All Mask Register Bit
000DH	R/W	DMA Master Clear
0081H	R/W	Page Register DMA Channel 2
0082H	R/W	Page Register DMA Channel 3
0083H	R/W	Page Register DMA Channel 1

The DMA Controller Registers

In order to begin a DMA transfer there are several registers within the DMA controller which need to be configured. The relevant registers are described below:-

Mode Register

Port 0BH

7	6	5	4	3	2	1	0
MODE Bit 1	MODE Bit 0	AUTO INC/ DEC	AUTO INIT.	TRANS MODE Bit 1	TRANS MODE Bit 0	CHAN SEL Bit 1	CHAN SEL Bit 0

Mode Bits

Bit1	Bit 0	FUNCTION
0	0	Demand Mode
0	1	Single Mode
1	0	Block Mode
1	1	Not Used

The mode bits set the particular mode for the channel, normally this will be set for SINGLE mode.

Auto INC/DEC

0	Increment Address
1	Decrement Address

When a DMA transfer takes place, the transfer address can either be incremented or decremented after each transfer selected by this bit.

Auto Initialise

0	Disabled
1	Enabled

If set to AUTO INITIALISE, when the DMA transfer reaches the end of a block, the DMA controller will reload all its initial values and repeat the transfer. This is useful on ANALOGUE OUT boards for outputting continuous wave forms.

Transfer Mode

Bit 1	Bit 0	FUNCTION
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Not Used

Use WRITE TRANSFER if the I/O board is generating a value to be written into memory (Analogue in), use read transfer when values are written from memory into the board (Analogue out).

Channel Select

Bit 1	Bit0	FUNCTION
0	0	DMA Channel 0 select
0	1	DMA Channel 1 select
1	0	DMA Channel 2 select
1	1	DMA Channel 3 select

Mask Register

Port 0AH

7	6	5	4	3	2	1	0
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	CLR/SET MASK	MASK Bit 1	MASK Bit 0

CLR/SET Mask

0	Clear Mask Bit
1	Set Mask Bit

Mask

Bit 1	Bit 0	FUNCTION
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Setting a mask bit for a particular channel disables the DMA operation on that channel.

Status Register

Port 0BH READ

7	6	5	4	3	2	1	0
CHAN 3 DMA RQ	CHAN 2 DMA RQ	CHAN 1 DMA RQ	CHAN 0 DMA RQ	CHAN 3 AT TC	CHAN 2 AT TC	CHAN 1 AT TC	CHAN 0 AT TC

DMA RQ 1 = DMA Request made on channel N

AT TC 1 = Channel N has reached the Terminal Count (TC)

The status register indicates which channels have made a DMA request and which channels have reached Terminal Count. Terminal count is set when the number of bytes specified by the TRANSFER LENGTH register have been transferred.

Clear Byte Pointer Flip Flop

Port 0CH

Any write to this port resets the byte pointer flip flop. This ensures that the first write to the Start Address or Transfer Length registers will go into the LSB of that register.

DMA Transfer Start Address

Port 00H, 02H, 04H, 06H

Sets the 16 bit start address for the DMA transfer, send LS Byte first.

Transfer Length

Port 01H, 03H, 05H, 07H

Sets the 16 bit length of the DMA transfer, send LS Byte first.

Page Register

Port 83H, 81H, 82H

Sets the upper four bits of the physical memory address of the DMA transfer.

Addressing

In order for DMA to operate correctly the page register and start address register should be set-up to inform the DMA controller where in memory the transfer is to take place.

The INTEL x86 family of microprocessors address memory using 2 address pointers called SEGMENT and OFFSET, this is called a LOGICAL address. The microprocessor combines the SEGMENT and OFFSET to produce a PHYSICAL address which it uses to access the memory.

If we consider a PC which has 1Mbyte of memory, each memory location will have a PHYSICAL address of 0 to 1048575 (or 0 to $FFFFF_{Hex}$).

It has a LOGICAL range of 0000:0000 to F000:FFFF. The colon is commonly used to separate the SEGMENT address from the OFFSET address (Segment:Offset)

To convert from LOGICAL address to PHYSICAL address use the following formula:

PHYSICAL ADDRESS = (SEGMENT * 16) + OFFSET

Most programming languages allow access to the SEGMENT and OFFSET addresses of variables in memory. For example, in QUICK BASIC the following commands can be used:

```
DIM dat%(1000)
seg = VARSEG(dat%)
offs = VARPTR(dat%)
```

In this example, the variables “seg” and “offs” would contain the SEGMENT and OFFSET addresses of the array “dat%”. In order to pass this address to the DMA controller the segment and offset values need to be converted into DMAPAGE and DMAOFFSET addresses in the following way:

```
PhyAdd = (seg * 16) + offs
DMAPAGE = (PhyAdd / 65536) AND 15
DMAOFFSET = PhyAdd AND 65535
```

DMA Limitations

The DMA controller is only capable of incrementing or decrementing the DMAOFFSET address, the DMAPAGE value is fixed throughout the transfer. This means that a maximum of 64K bytes can be transferred in one operation.

Programming Example

To set-up a DMA transfer the following program sequence is required:

- Define an area of memory for the transfer
- Set-up the I/O board for DMA operation
- Disable the DMA channel being used.
- Load the start address into PAGE register. This is the START address register for the DMA channel being used.
- Load the length count into the TRANSFER LENGTH register. Note that the DMA controller only transfers 8 bits at a time, each value written to an ANALOGUE OUT board or read from an ANALOGUE IN board is 2 bytes long so the transfer length will be twice the number of samples to be taken.
- Load the mode for the selected DMA channel.
- Enable the DMA channel.

The extract from a QUICK BASIC program on the following page demonstrates how to program the DMA controller for a WRITE transfer.

```
2000 REM PROGRAM THE DMA CONTROLLER
2005 REM FIRST EXTRACT THE SEGMENT AND OFFSET
      ADDRESS OF OUR DATA
2010 seg = VARSEG(DAT%(0))
2020 offs = VARPTR(DAT%(0))
2025 REM Transfer the Logical SEGMENT:OFFSET address
2027 REM into a physical PAGE:OFFSET address
2030 PAGE& = seg1% AND &HF000
2040 PAGE& = PAGE& / 4096
2050 PAGE& = PAGE& AND 15
2060 OFFSET& = seg
2070 OFFSET& = OFFSET& * 16
2080 OFFSET& = OFFSET& + offs
2090 OFFSET& = OFFSET& AND 65535
2100 REM Set-up the DMA registers.
2105 OUT (&HA),7: REM DISABLE DMA CHANNEL 3
2110 OUT (&HC), 0: REM RESET BYTE SELECT FF
2120 OUT (&HB), &H47: REM AUTO INC ON CH3,WRITE
      TRANSFER, SINGLE MODE
2130 OUT (&H82), PAGE&: REM SET PAGE FOR DMA CH3
2150 OUT (&H6), (OFFSET& AND 255): REM SET UP START
      FOR LS 8 BITS
2160 OUT (&H6), (OFFSET& AND &HFF00) / 256: REM SET
      UP START FOR MS 8 BITS
2170 OUT (&H7), length% AND 255: REM BYTE COUNT LS 8
      BITS
2180 OUT (&H7), length% / 256: REM BYTE COUNT MS
      BITS
2190 OUT (&HA), 3: REM ENABLE DMA TXFER
2200 RETURN
```