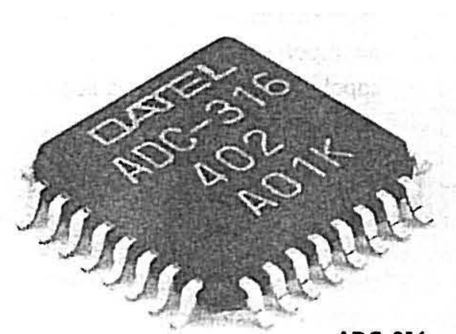
ADC-316

6-Bit, 140 MHz Flash A/D Converter

PRODUCT DATA SHEET



ADC-316

FEATURES

- Low Power Consumption: 225mW (typ.)
- Wide Analog Input Bandwidth: 200MHz
- Low Input Capacitance: 7pF (typ.)
- Differential Nonlinearity: ±0.25 LSB
- Low Error Rate
- ECL 100K/10KH/10K compatible

GENERAL DESCRIPTION

The ADC-316 is a 6-bit, high speed Flash Analog to Digital converter capable of digitizing analog signals at a rate of 140MHz. The ADC-316 is sparkle code error free up to Nyguist frequency. The digital I/O level of the ADC-316 is compatible with ECL 100K/10KH/10K.

The main features of the ADC-316 include ±0.25 LSB integral and differential nonlinearity error, a low 7pF input capacitance, min. 200MHz input bandwidth and a low 36dB signal to noise ratio with distortion.

The ADC-316 is packaged in a small 32-Pin plastic QFP and operates over the -20°C to +75°C temperature range.

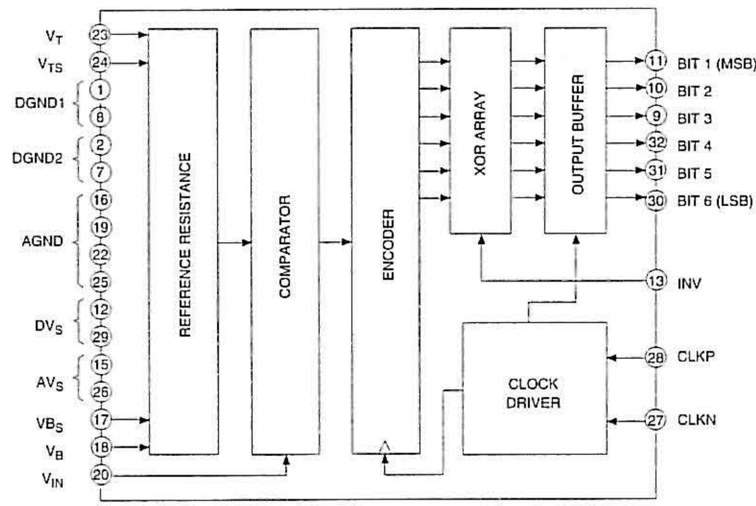
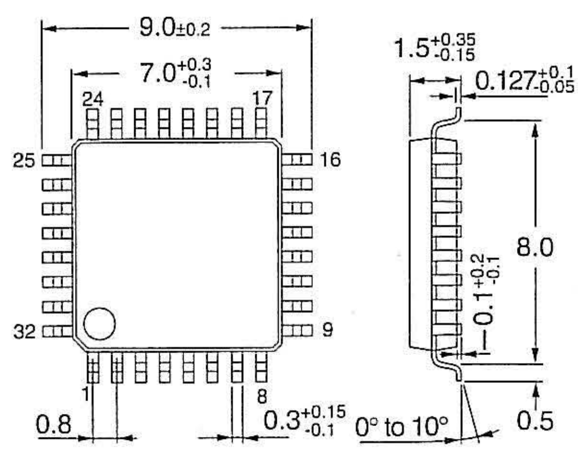


Figure 1. ADC-316 Simplified Block Diagram

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL GROUND 1	17	REF. BOTTOM SENSE (V_{BS})
2	DIGITAL GROUND 2	18	REF. BOTTOM (V_B)
3	NO CONNECTION	19	ANALOG GROUND
4	NO CONNECTION	20	ANALOG IN (V_{IN})
5	NO CONNECTION	21	NO CONNECTION
6	NO CONNECTION	22	ANALOG GROUND
7	DIGITAL GROUND 2	23	REF. TOP (V_T)
8	DIGITAL GROUND 1	24	REF. TOP SENSE (V_{TS})
9	BIT 3	25	ANALOG GROUND
10	BIT 2	26	AV_S (Analog)
11	BIT 1 (MSB)	27	CLOCK IN (CLKN)
12	DV_S (Digital)	28	CLOCK IN (CLKP)
13	INVERT (INV)	29	DV_S (Digital)
14	NO CONNECTION	30	BIT 6 (LSB)
15	AV_S (Analog)	31	BIT 5
16	ANALOG GROUND	32	BIT 4

Mechanical Dimensions
Units: mm



32-pin Plastic QFP

ABSOLUTE MAXIMUM RATINGS (Ta = +25°C)

PARAMETERS	SYMBOLS	LIMITS	UNITS
Supply Voltage	(AV_S, DV_S)	-7 to +0.5	V
Analog Input Voltage	(V_{IN})	-2.7 to +0.5	V
Reference Input Voltage	(V_T, V_B)	-1.5 to +0.5	V
	[V_T - V_R]	2.5	V
Digital Input Voltage	(CLKP, CLKN, INV)	-4 to +0.5	V
	[CLKP, CLKN]	2.7	V
Digital Output Current	Bit 1 to BIT 6	-30 to 0	mA

FUNCTIONAL SPECIFICATION

(Typical at Ta = +25°C, AV_S = DV_S = -5.2 V, V_T = 0V, V_R = -2V) -1V

ANALOG INPUTS

PARAMETERS	SYMBOLS	MIN.	TYP.	MAX.	UNITS
Input Voltage	(V_{IN})	V_B	-	V_T	V
Input Capacitance					
	V_{IN} = -1V+0.07V	-	7	18	pF
Input Resistance		300	-	-	kΩ
Input Bandwidth	(-3.0dB)	200	-	-	MHz
Bias Current	V_{IN} = -1V	-	-	400	µA
Reference Input	(V_T)	-0.1	0	+0.1	V
	(V_B)	-2.2	-2.0	← 0.8	V
Reference Resistance	(R_R)	-	-	200	Ω
Offset Voltage	(E_{OT}, E_{OB})	-	-	20	mV

DIGITAL INPUTS

PARAMETERS	SYMBOLS	MIN.	TYP.	MAX.	UNITS
Input Voltage	(V_{IH})	-1.13	-	0.65	V
	(V_{IL})	2.1	-	-1.15	V
Input Current	(I_{IH})				
	V_{IH} = -0.8V	0	-	50	µA
	(I_{IL})				
	V_{IL} = -1.6V	-50	-	50	µA
Input Capacitance	-	7	-	pF	
Clock Pulse Width	(t_{PW1}, t_{PW0})	3.0	-	-	ns

PERFORMANCE

PARAMETERS	SYMBOLS	MIN.	TYP.	MAX.	UNITS
Conversion Rate	(F_C)	140	-	-	MHz
Resolution		6	-	-	Bits
Integr./Diff. Linearity Error					
	F_C = 140MHz	-0.25	-	+0.25	LSB
Error rate	Clock = 140MHz	-	-	1E-09	TPS*1
Signal-to-Noise Ratio with Distortion					
	V_{IN} = FS, Fin = 1MHz	-	36	-	dB
	Fin = 70MHz	-	34	-	dB
Aperture Uncertainty	(T_U)	-	10	-	ps
Aperture Delay	(T_A)	-	1.5	-	ns

DIGITAL OUTPUTS

PARAMETERS	SYMBOLS	MIN.	TYP.	MAX.	UNITS
Output Voltage	(V_{OH})*2	-1.10	-	-0.65	V
	(V_{OL})*2	-2.1	-	-1.6	V
Output Delay	(T_D)*2	3.0	3.6	4.2	ns
Output Rise Time	(T_R)*3	-	0.8	-	ns
Output Fall Time	(T_F)*3	-	1.0	-	ns

$0.8V \leq |V_{RT} - V_{RB}| \leq 2.2V$

Technical Notes

1. Even with the input capacitance down to 18pF or less, the converter still requires an input amplifier with good drive capability to take full advantage of the converter's input bandwidth.

2. The input impedance of the ADC-316 is capacitive which may result in the input amplifier becoming unstable and causing oscillations. Stop oscillations by placing a resistor between the amplifier and the converter's input. See Figure 2 (Typical Connections).

3. CLKP and CLKN (ECL) are usually differentially supplied.
The ADC-316 is operable without CLKN input but using complementary input is recommended to obtain stable high-speed performance. If CLKN is left open the voltage goes to ECL threshold potential (-1.3V).

4. The polarity of the output data is controlled by input INV as shown in Table 1. Leave the input open for a logic level '0'.

5. Digital output bits 1 through 6 require 100Ω pull down resistors connected to the -2V supply rail. Refer to Figure 2 (Typical Connections).

6. The reference voltage range (-2.0V to 0V typical) determines the dynamic range of the input voltage. Adjustments to this range can be made within the range of V_B = -2V ±0.2V and V_T = 0V ±0.1V. The reference input V_B should be decoupled to GND using 1µF and 10nF capacitors. When connecting a voltage to V_T other then analog ground, decouple to a AGND using 1µF and 10nF capacitors.

7. Substantial analog and digital ground planes must be provided.
It is recommended that these ground planes are taken to a common point, the power ground plane, which should be located as close to the ADC as possible.

PARAMETERS	SYMBOLS	MIN.	TYP.	MAX.	UNITS
POWER REQUIREMENTS					
Power Supply Voltage	(AV_S, DV_S)	-5.5	-5.2	-4.95	V
	$(AV_S - DV_S)$	-0.05	-	0.05	V
	(AGND - DGND)	-0.05	-	0.05	V
Power Supply Current	(I_S)				
AVS = DVS = -5.2V		-60	-40	-25	mA
Power Consumption	(Pd)	-	225	-	mW

ENVIRONMENTAL/PHYSICAL

	MIN.	TYP.	MAX.	UNITS
Operating Temperature Range	-20	-	+75	°C
Storage Temperature Range	-65	-	+150	°C
Package		32-pin Plastic QFP		
Weight		0.2		g

*1 TPS: Times Per Sample
*2 RL = 100Ω to -2V
*3 RL = 100Ω to -2V, 20% to 80%

Table 1.Digital Output Coding

INV		1		0	
OUTPUT		BIT 1 (MSB)	BIT 6 (LSB)	BIT1 (MSB)	BIT 6 (LSB)
V_{IN}*)	STEP				
0V	0	000000		111111	
	1	000001		111110	
		.		.	
-1V	31	011111		100000	
	32	100000		011111	
		.		.	
	62	111110		000001	
-2V	63	111111		000000	

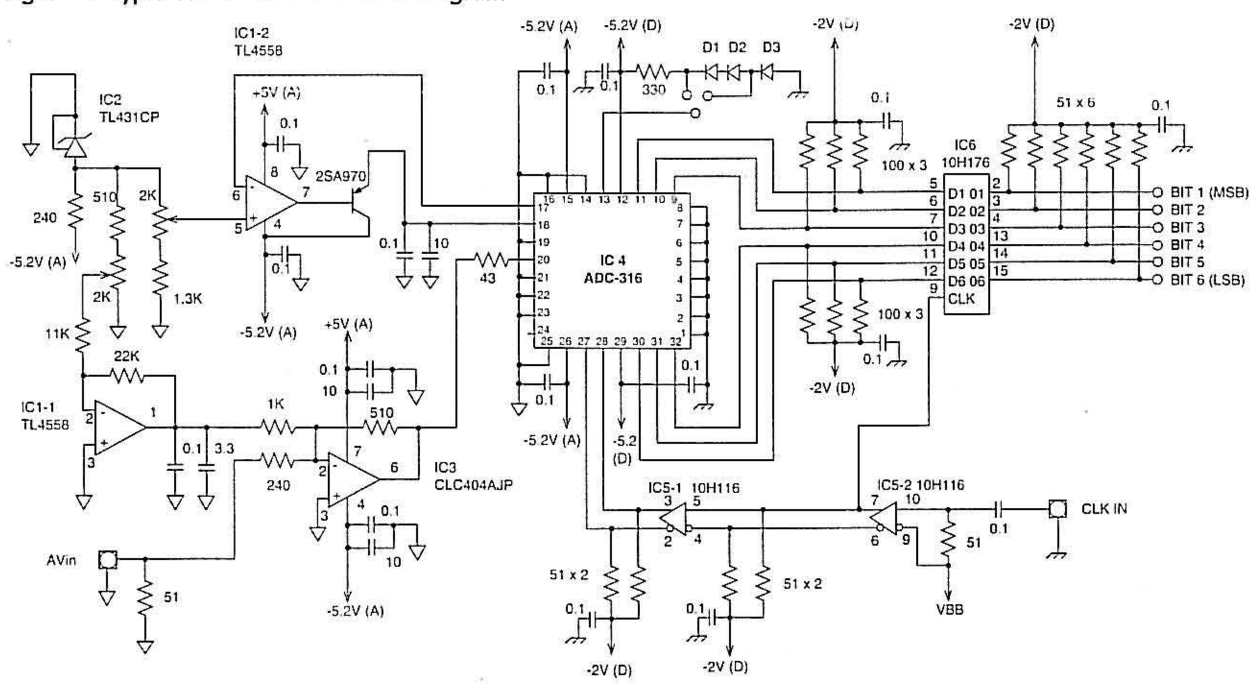
*)V_T = 0V, V_B = -2V

8. DGND1 is the ground for the internal logic circuits. DGND2 is the ground for the output transistors. AGND is the ground for the input buffers and comparator latches. Keep separated until connected at the power ground plane.

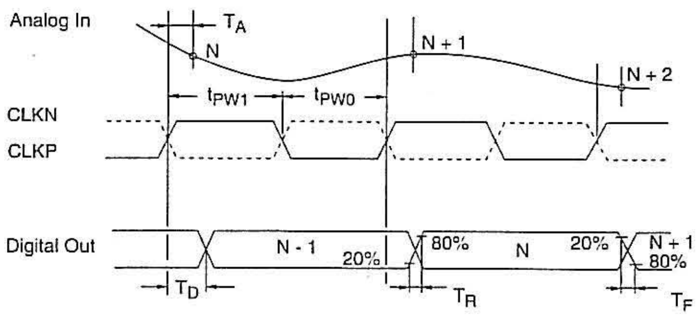
9. Although not internally connected, tie all NC (No Connection) pins to either AGND or DGND on the printed circuit board.

10. The analog and digital power supply inputs (-5.2V) are internally connected through a resistance of 4Ω to 6Ω and it is possible to use one power source for both inputs. For best performance, the power supplied to the analog and digital inputs (-5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second, the device may be destroyed. Both -5.2V lines should be decoupled using 1μF and 10nF capacitors located as close to the pins as possible.

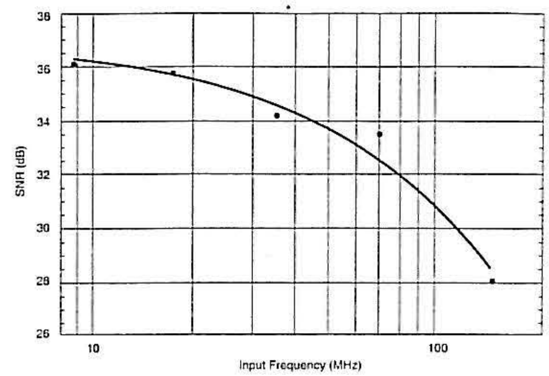
Figure 2. Typical ADC-316 Connection Diagram



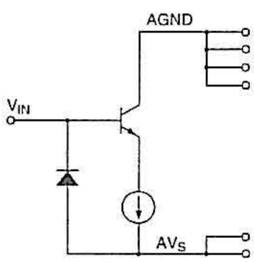
Timing Diagram



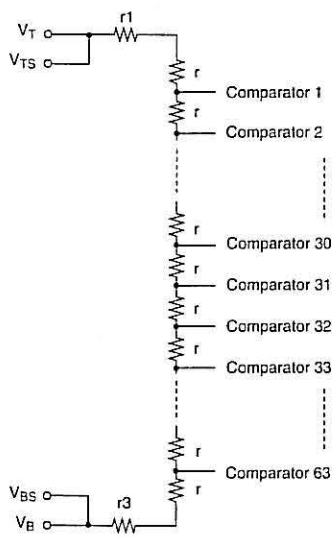
Typical Performance Curve



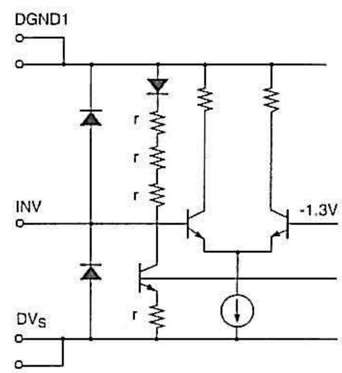
Equivalent Circuits



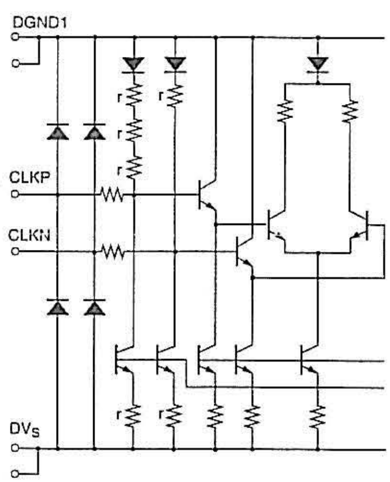
Analog Signal Input



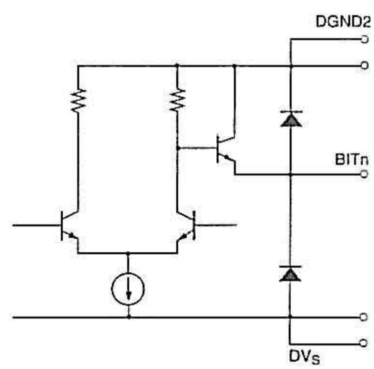
Reference Input
(For decoupling see Tech. Notes Item 6)



Digital Data In
(Refer to Table 1 Output Coding)



Clock Input
(See Tech. Notes Item 3)



Digital Data Out
(For pull down resistors see Tech. Notes Item 5)