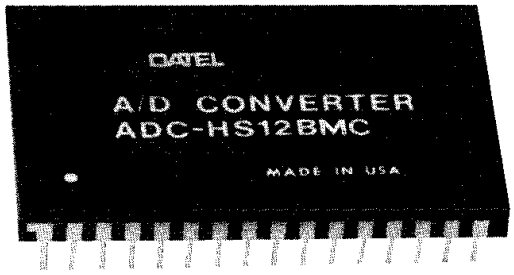
DATEL®
INNOVATION and EXCELLENCE

ADC-HS12B
12-Bit A/D Converter With Sample-Hold

FEATURES

- **12-Bit resolution**
- **Internal sample and hold**
- **6 Microseconds acquisition time**
- **9 Microseconds conversion time**
- **Programmable input ranges**
- **Parallel output**

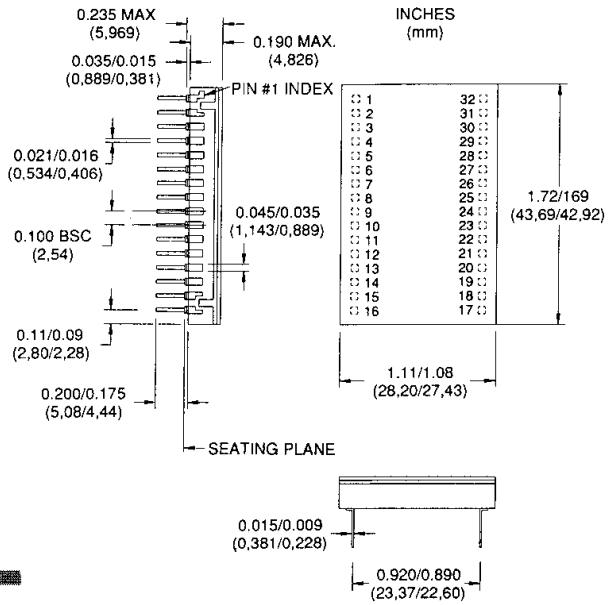


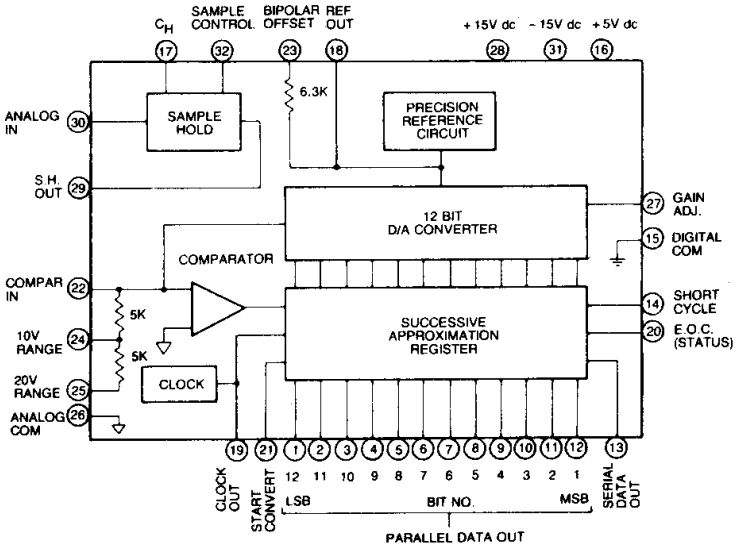
GENERAL DESCRIPTION

The ADC-HS12B is a high performance 12-bit hybrid A/D converter with a self-contained sample-hold. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. The internal sample-hold has a 6 microseconds acquisition time for a full 10V dc input change; the A/D converter has a fast 9 microseconds conversion time. Five input voltage ranges are programmable by external pin connection; 0 to +5V, 0 to+10V, ±2.5V, ±5V, and ±10V. Input impedance to the sample-hold is 100 megohms. Output coding is complementary binary for unipolar operation and complimentary offset binary for bipolar operation.

The ADC-HS12B uses a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic 12-bit successive approximation register, a clock and a monolithic sample-hold.

MECHANICAL DIMENSIONS INCHES (mm)





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	C_H
2	BIT 11 OUT	18	REF OUT
3	BIT 10 OUT	19	DO NOT CONNECT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V RANGE
9	BIT 4 OUT	25	20V RANGE
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJ.
12	BIT 1 OUT (MSB)	28	+15V POWER
13	DO NOT CONNECT	29	S.H. OUTPUT
14	SHORT CYCLE	30	ANALOG IN
15	DIGITAL COM	31	-15V POWER
16	+5V POWER	32	SAMPLE CONTROL

ABSOLUTE MAXIMUM RATINGS	
Positive Supply, pin 28	+18V
Negative Supply, pin 31	−18V
Logic Supply Voltage, pin 16	+5.5V
Digital Input Voltage, pins 14, 21, 32	+5.5V
Analog Input Voltage, pin 30	±15V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance[1]	100 megohms
Input Bias Current[1]	50 nA typical, 200 nA max.
Start Conversion	2V min. to +5.5V max. positive pulse with 100 nsec. duration min. Rise and fall times <30 nsec. Logic high to low transition resets converter and initiates next conversion. Loading: 2 TTL loads
Sample Control Input	Logic high = hold Logic low = sample Loading: 1 TTL load

OUTPUTS[2]	
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary
End of Conversion (status)	Conversion status signal. Output is logic high during reset and conversion and low when conversion is complete.

SAMPLE-HOLD PERFORMANCE[3]	
Input Offset Drift	25 µV/°C
Acquisition Time, 10V to 0.01%	6 µsec.
Bandwidth	1 MHz
Aperture Delay Time	100 nsec.
Aperture Uncertainty Time	10 nsec.
Sample to Hold Error	2.5 mV max.
Hold Mode Droop	200 nV/µsec. max.
Hold Mode Feedthrough	0.01% max.

CONVERTER PERFORMANCE	
Resolution	12 bits (1 part in 4096)
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±¾ LSB max.
Temp. Coefficient of Gain	±20 ppm/°C max.
Temp. Coefficient of Zero, unipolar	±5 ppm/°C of FSR max.
Temp. Coefficient of Offset, bipolar	±10 ppm/°C of FSR max.
Differential Nonlinearity Tempco	±2 ppm/°C of FSR
Missing Codes	None over oper. temp. range
Conversion Time	9 µsec. max.
Power Supply Rejection	0.004%/% max.

POWER REQUIREMENTS	
Power Suppy Voltage	+15V dc ±0.5V at 20 mA −15V dc ±0.5V at 25 mA +5V dc ±0.25V at 85 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, Case	0°C to 70°C (BMC) -55°C to +125°C (BMM, BMM-QL)
Storage Temperature Range	-65°C to +150°C
Package Type	32 pin ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounces (14 grams)

FOOTNOTES:

1. For sample-hold input
2. All digital outputs can drive 2 TTL loads
3. For 1000 pF external hold capacitor

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01 µF ceramic capacitor in parallel with a 1 µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 1 µF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01 µF ceramic capacitor. These precautions will assure noise free operation of the converter.

2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V dc ground should be run to pin 15.

3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100 ppm/ °C, cermet types. The adjustment range is ±0.5% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. Calibration of the ADC-HS12B is performed with the sample-hold connected and operating dynamically. This results in adjusting out the sample-hold errors along with the A/D converter. For slow throughput applications it is recommended that a 0.01 µF hold capacitor be used for best accuracy. With this value the acquisition time becomes 25 microseconds and the external timing must be adjusted accordingly.

4. The recommended timing shown in the Timing Diagram allows 6 microseconds for the sample-hold acquisition and then 1 microsecond after the sample-hold goes into the hold mode to allow for output settling before the A/D begins its conversion cycle.

5. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions in the Table.

6. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary. In cases where bipolar coding of offset binary is required, this can be achieved by inverting the analog input to the converter (using an operational amplifier connected for gain of -1.0000). The

converter is then calibrated so that –FS analog input gives an output code of 0000 0000 0000, and +FS – 1 LSB gives 1111 1111 1111.

7. These converters dissipate 1.81 watts maximum of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
8. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock. The pulse width of the external clock should be between 100 nanoseconds and 300 nanoseconds. Each N bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

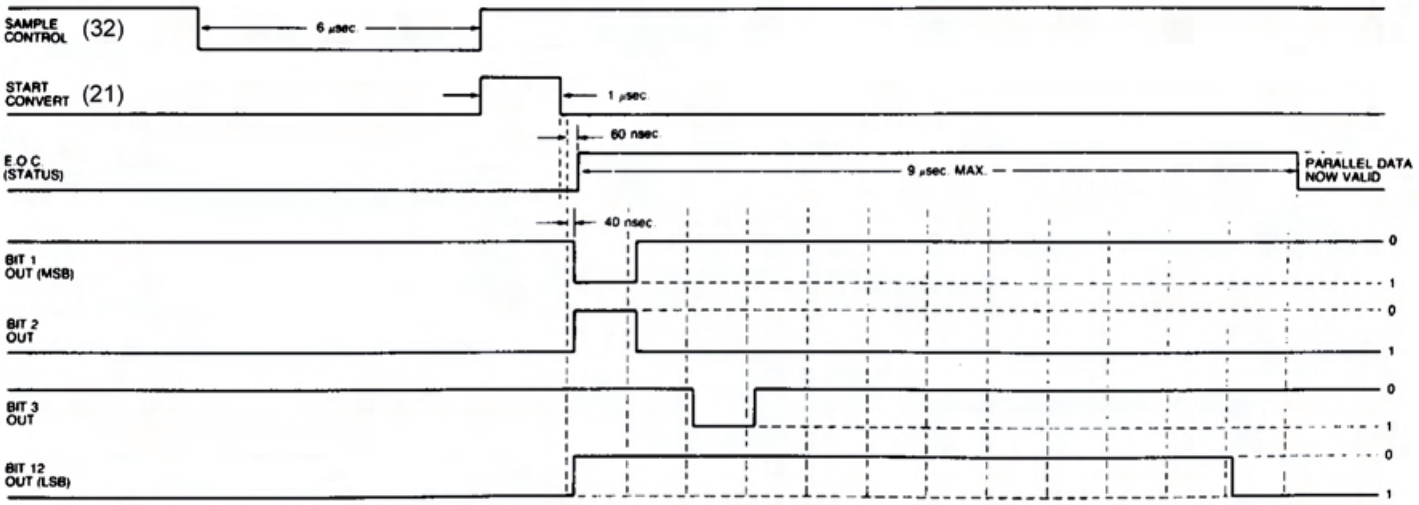
Sample-Hold Operation

The ADC-HS12B incorporates the LF398 monolithic sample-hold. A logic level LO applied to the Sample Control pin (32) places the sample-hold into acquisition (sample) mode; a logic level HI places the sample-hold in hold mode.

For a full scale 10V input voltage change an acquisition (sample) time of 6us and a 1us hold-mode settling time is required. The Sample Control pin (32) is held LO for 6us. A delay of 1us is allowed for hold-mode settling time before the falling edge of the logic signal is applied to the Start Convert (pin 21) to initiate a conversion.

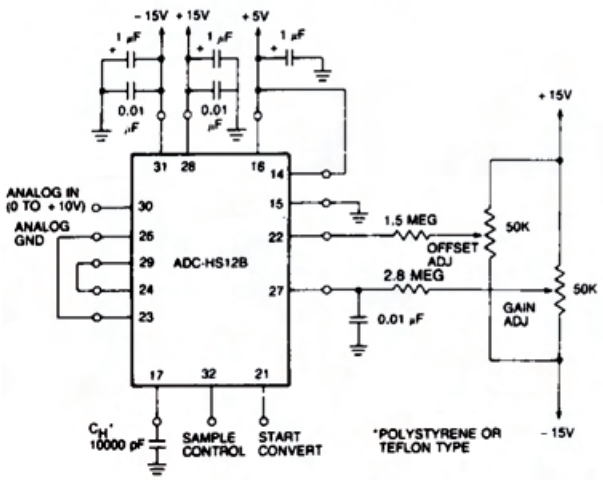
In this application a 1000pf Polystyrene or Teflon type quality capacitor, connected from the CH (Hold Capacitor- Pin 17) of the ADC-HS12B to Analog Ground, is recommended.

TIMING DIAGRAM FOR ADC-HS12B

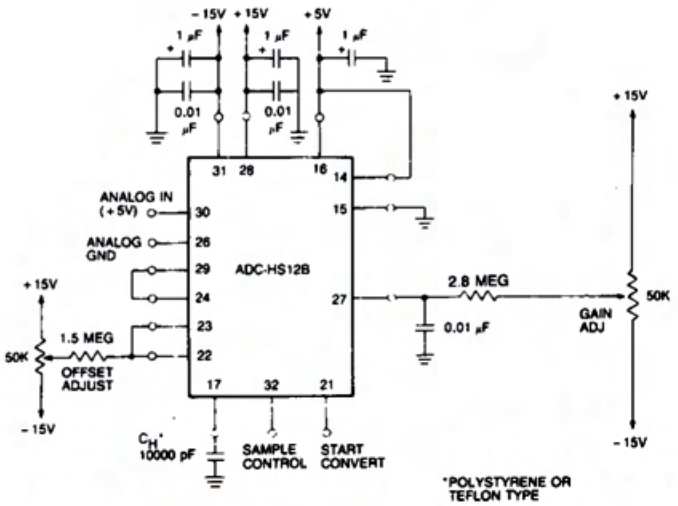


NOTE: TRIGGER, SAMPLE CONTROL, AND START CONVERT PULSES MUST BE EXTERNALLY GENERATED

UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, ±5V



CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +5V	MSB		LSB
+9.9976V	+4.9988V	0000	0000	0000
+8.7500	+4.3750	0001	1111	1111
+7.5000	+3.7500	0011	1111	1111
+5.0000	+2.5000	0111	1111	1111
+2.5000	+1.2500	1011	1111	1111
+1.2500	+0.6250	1101	1111	1111
+0.0024	+0.0012	1111	1111	1110
0.0000	0.0000	1111	1111	1111

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY		
±10V	±5V	±2.5V	MSB		LSB
+9.9951V	+4.9976V	+2.4988V	0000	0000	0000
+7.5000	+3.7500	+1.8750	0001	1111	1111
+5.0000	+2.5000	+1.2500	0011	1111	1111
0.0000	0.0000	0.0000	0111	1111	1111
−5.0000	−2.5000	−1.2500	1011	1111	1111
−7.5000	−3.7500	−1.8750	1101	1111	1111
−9.9951	−4.9976	−2.4988	1111	1111	1110
−10.0000	−5.0000	−2.5000	1111	1111	1111

CALIBRATION PROCEDURE

1. Connect the ADC-HS12B as shown in one of the connection diagrams. The sample-hold and A/D converter should be timed as shown in the timing diagram. The trigger pulse should be applied at a rate of 70 kHz or less and should be 100 nanoseconds minimum width.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (−FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS−1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

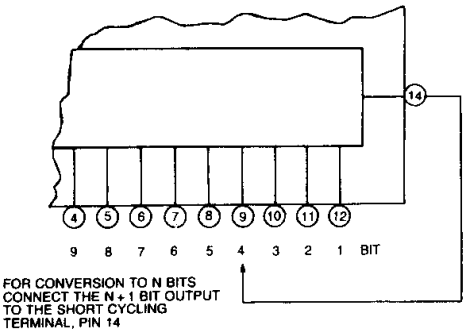
CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 to +5V	ZERO GAIN	+0.6 mV +4.9982V
0 to +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	−2.4994V +2.4982V
±5V	OFFSET GAIN	−4.9988V +4.9963V
±10V	OFFSET GAIN	−9.9976V +9.9927V

PIN 14 CONNECTION FOR SHORT CYCLE OPERATION

RES. (BITS)	PIN 14 TO	CONV. TIME
1	PIN 11	0.7 µsec
2	PIN 10	1.3
3	PIN 9	2.0
4	PIN 8	2.6
5	PIN 7	3.3
6	PIN 6	4.0
7	PIN 5	4.6
8	PIN 4	5.3
9	PIN 3	6.0
10	PIN 2	6.6
11	PIN 1	7.3
12	PIN 16	9.0

SHORT CYCLE OPERATION



INPUT CONNECTIONS

INPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER		
0 to +5V	29 & 24	22 & 25	23 & 26
0 to +10V	29 & 24	—	23 & 26
±2.5V	29 & 24	22 & 25	23 & 22
±5V	29 & 24	—	23 & 22
±10V	29 & 25	—	23 & 22

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-HS12BMC	0 to +70 °C
ADC-HS12BMM	-55 to +125 °C
ADC-HS12BMM-QL	-55 to +125 °C

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