Complementary 30-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
P-Channel	−30	0.051 @ V_{GS} = −10 V	−6.4
		0.075 @ V_{GS} = −6 V	−5.3
N-Channel	30	0.035 @ V_{GS} = 10 V	7.7
		0.050 @ V_{GS} = 4.5 V	6.5

FEATURES

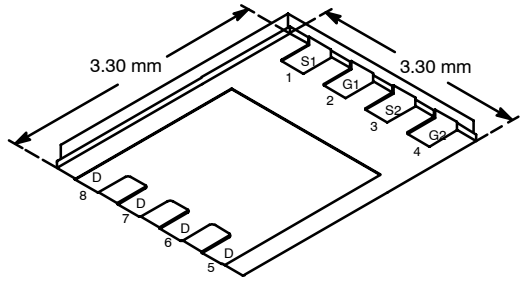
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

Pb-free
RoHS COMPLIANT

APPLICATIONS

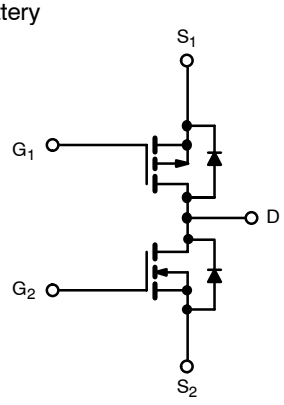
- Backlight Inverter
- DC/DC Converter
  - 4-Cell Battery

PowerPAK 1212-8



Bottom View

Ordering Information: Si7501DN-T1—E3 (Lead (Pb)-Free)



P-Channel

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter		Symbol	P-Channel		N-Channel		Unit
			10 secs	Steady State	10 secs	Steady State	
Drain-Source Voltage		V_{DS}	−30		30		V
Gate-Source Voltage		V_{GS}	±25		±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	−6.4	−4.5	7.7	5.4	A
	T_A = 70°C		−5.1	−3.6	4.7	4.3	
Pulsed Drain Current		I_{DM}	−25		25		
Continuous Source Current (Diode Conduction)[a]		I_S	−2.6	−1.3	2.6	1.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.1	1.6	3.1	1.6	W
	T_A = 70°C		3	1.0	2	1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150				°C
Soldering Recommendations (Peak Temperature)[b,c]			260				

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	32	40	°C/W
	Steady State		65	81	
Maximum Junction-to-Foot (Case)	Steady State	R_{thJC}	5	6.3	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (http://www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

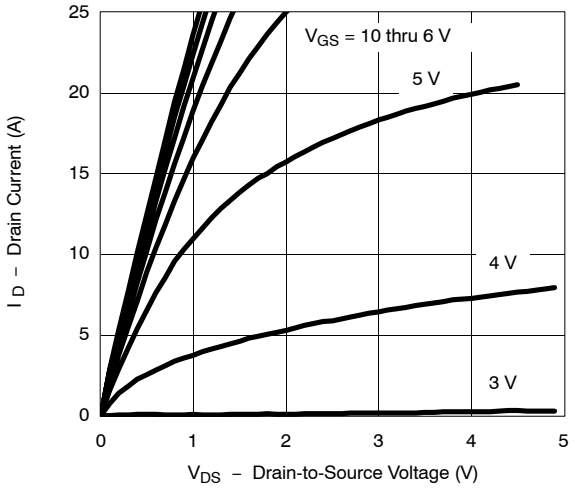
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	P-Ch	−1.0		−3	V
		V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	1.0		3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25 V	P-Ch			±200	nA
		V_{DS} = 0 V, V_{GS} = ±20 V	N-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V	P-Ch			−1	μA
		V_{DS} = 30 V, V_{GS} = 0 V	N-Ch			1	
		V_{DS} = −30 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−5	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ −5 V, V_{GS} = −10 V	P-Ch	−25			A
		V_{DS} ≤ 5 V, V_{GS} = 10 V	N-Ch	25			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −6.4 A	P-Ch		0.041	0.051	Ω
		V_{GS} = 10 V, I_D = 7.7 A	N-Ch		0.028	0.035	
		V_{GS} = −6 V, I_D = −5.3 A	P-Ch		0.055	0.075	
		V_{GS} = 4.5 V, I_D = 6.5 A	N-Ch		0.040	0.050	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −6.4 A	P-Ch		13		S
		V_{DS} = 15 V, I_D = 7.7 A	N-Ch		15		
Diode Forward Voltage[a]	V_{SD}	I_S = −1.7 A, V_{GS} = 0 V	P-Ch		−0.80	−1.2	V
		I_S = 1.7 A, V_{GS} = 0 V	N-Ch		0.80	1.2	
Dynamic[b]							
Total Gate Charge	Q_g	P-Channel V_{DS} = −15 V, V_{GS} = −10 V, I_D = −6.4 A N-Channel V_{DS} = 15 V, V_{GS} = 10 V, I_D = 7.7 A	P-Ch		12.5	19	nC
			N-Ch		9	14	
Gate-Source Charge	Q_{gs}		P-Ch		2.5		
			N-Ch		2		
Gate-Drain Charge	Q_{gd}		P-Ch		3.6		
			N-Ch		1.3		
Gate Resistance	R_g		P-Ch		9		Ω
			N-Ch		3		
Turn-On Delay Time	$t_{d(on)}$	P-Channel V_{DD} = −15 V, R_L = 5 Ω I_D ≅ −3 A, V_{GEN} = −10 V, R_G = 1 Ω N-Channel V_{DD} = 15 V, R_L = 5 Ω I_D ≅ 3 A, V_{GEN} = 10 V, R_G = 1 Ω	P-Ch		10	15	ns
			N-Ch		10	15	
Rise Time	t_r		P-Ch		20	30	
			N-Ch		15	25	
Turn-Off Delay Time	$t_{d(off)}$		P-Ch		25	40	
			N-Ch		20	30	
Fall Time	t_f		P-Ch		30	45	
			N-Ch		10	15	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.7 A, di/dt = 100 A/μs	P-Ch		25	50	
		I_F = 1.7 A, di/dt = 100 A/μs	N-Ch		20	40	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

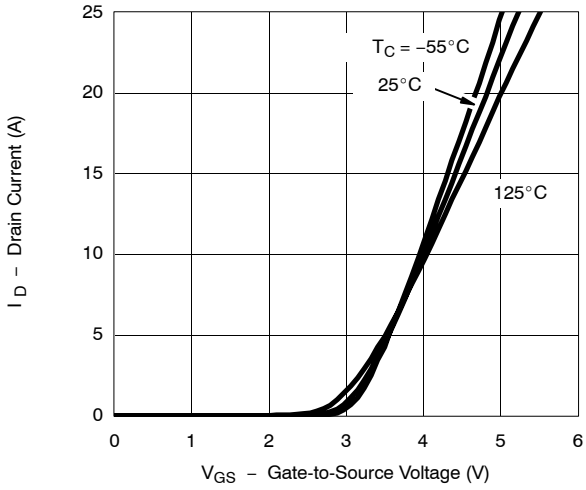
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

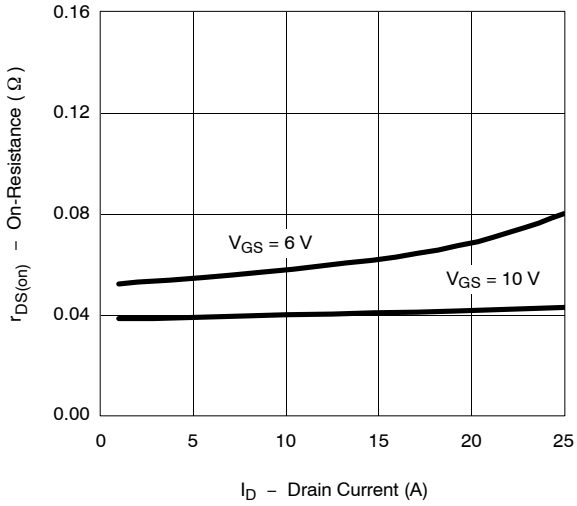
Output Characteristics



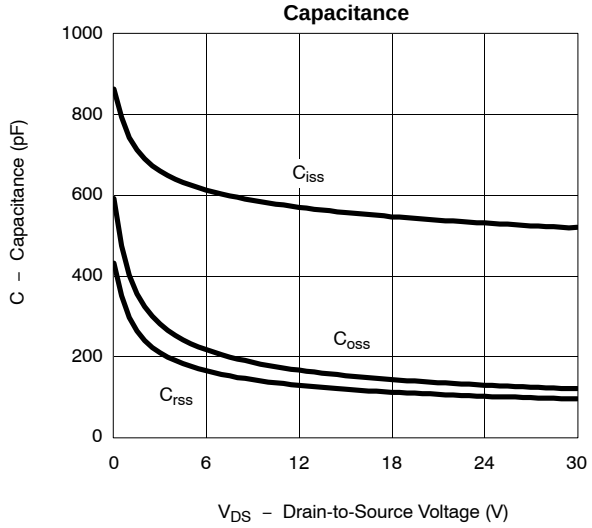
Transfer Characteristics



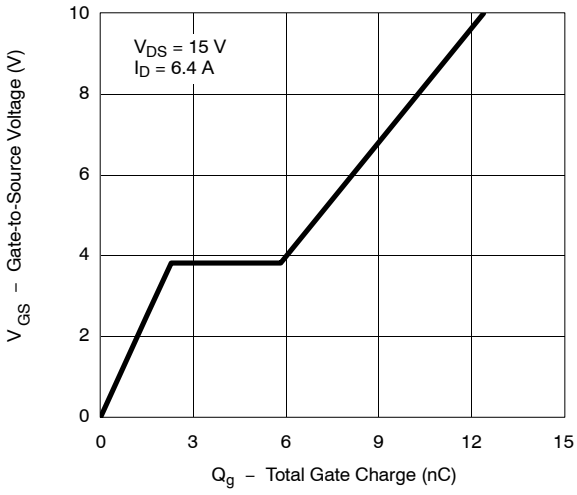
On-Resistance vs. Drain Current



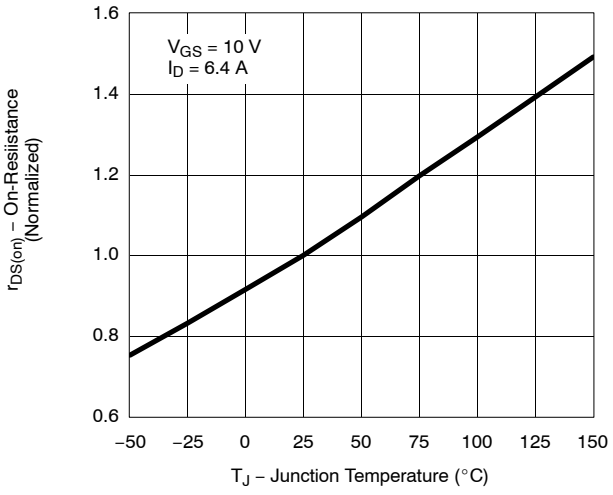
Capacitance



Gate Charge

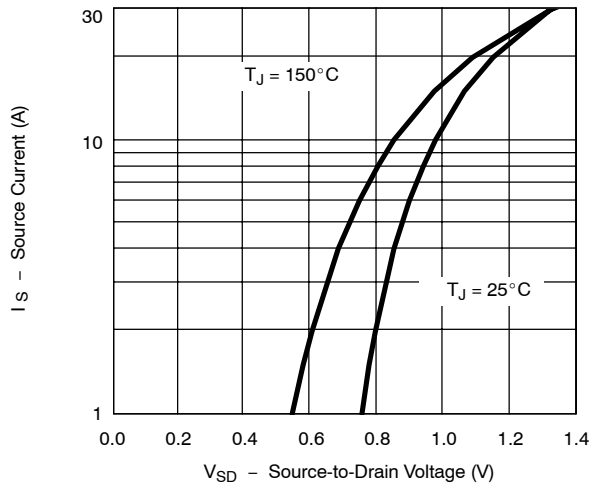


On-Resistance vs. Junction Temperature

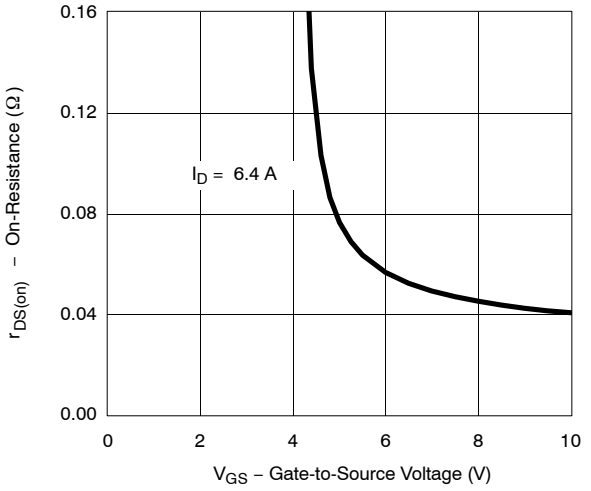


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

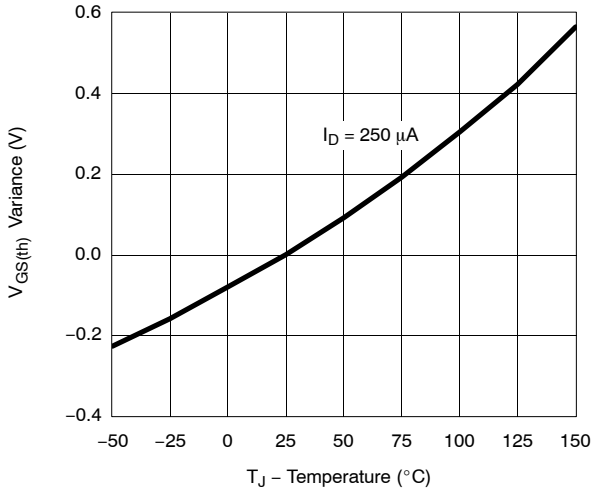
Source-Drain Diode Forward Voltage



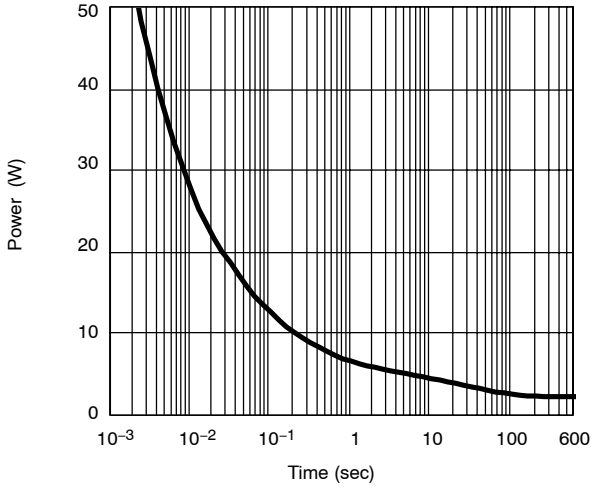
On-Resistance vs. Gate-to-Source Voltage



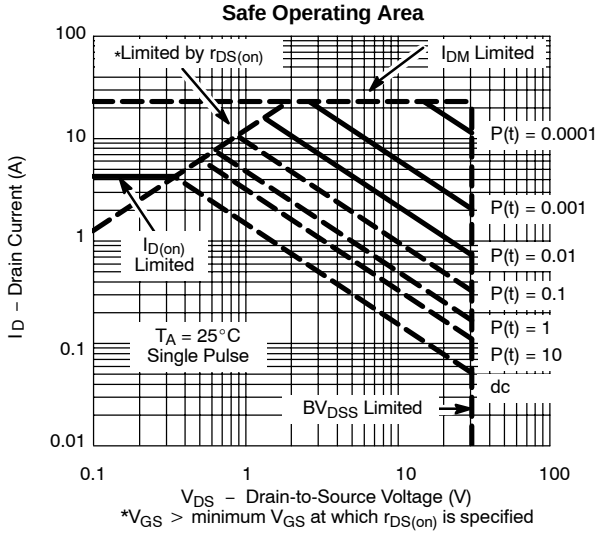
Threshold Voltage



Single Pulse Power

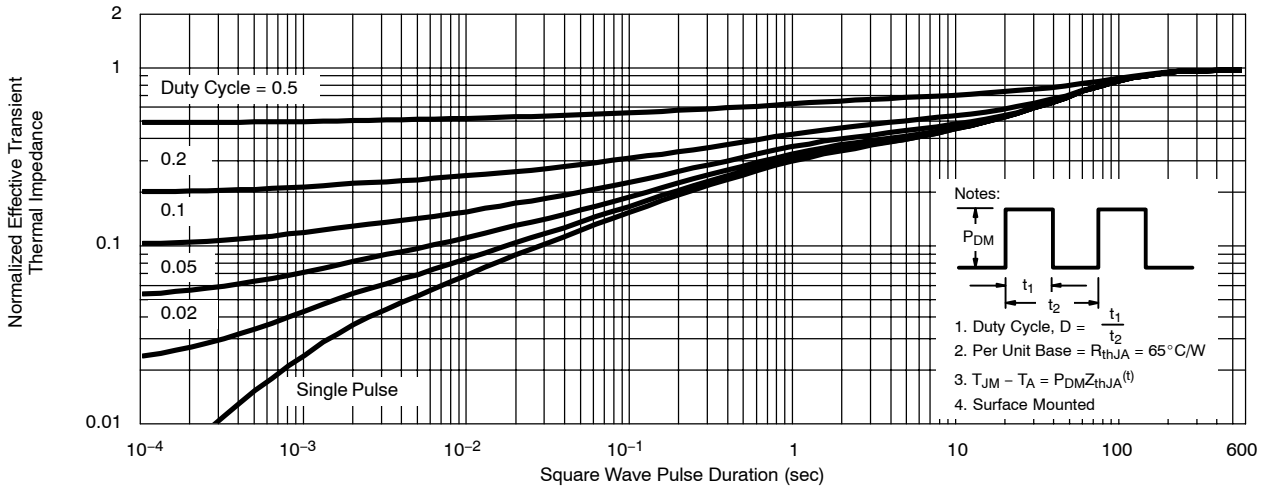


Safe Operating Area

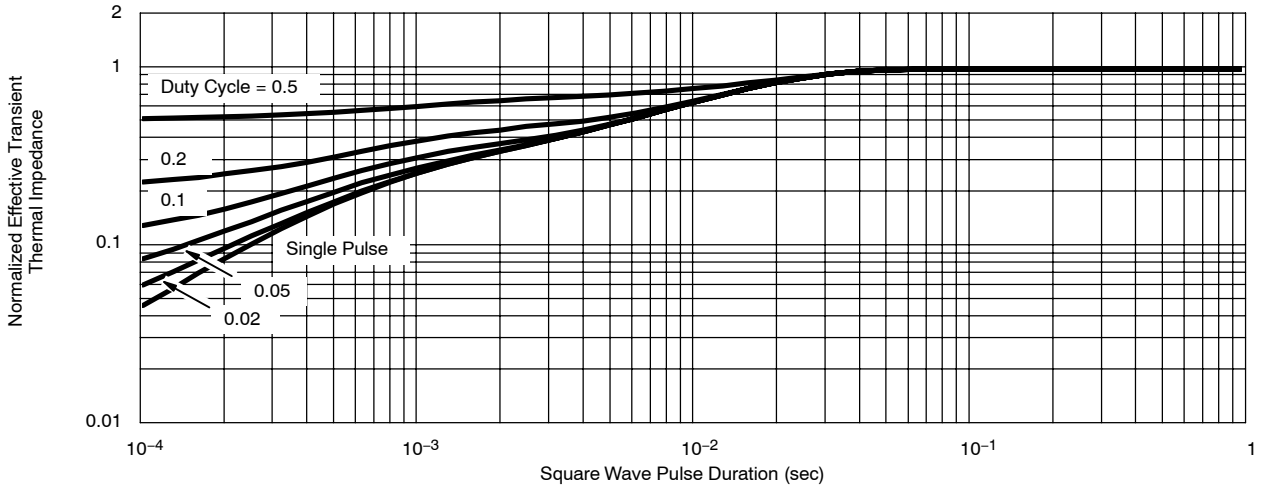


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

Normalized Thermal Transient Impedance, Junction-to-Ambient

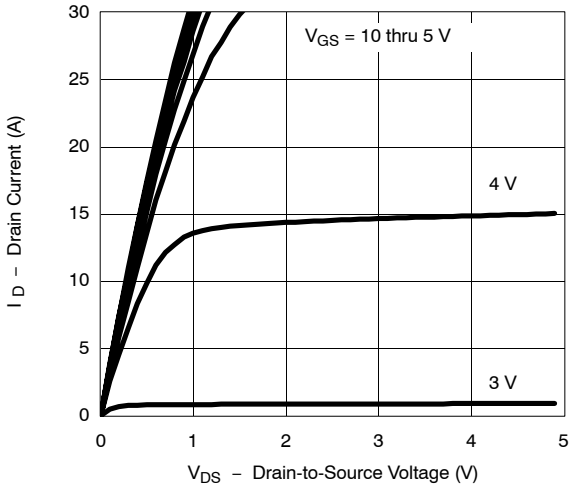


Normalized Thermal Transient Impedance, Junction-to-Case

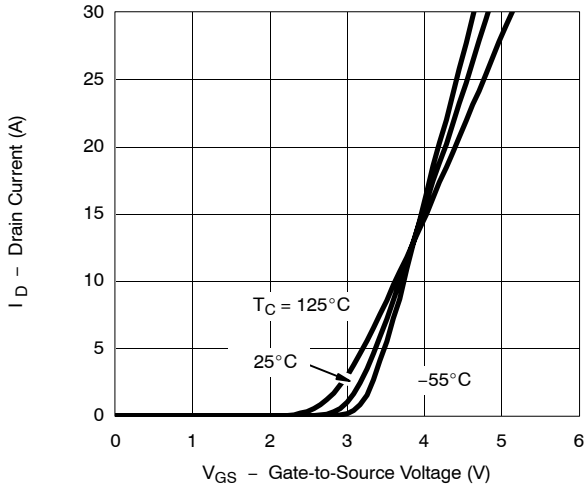


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

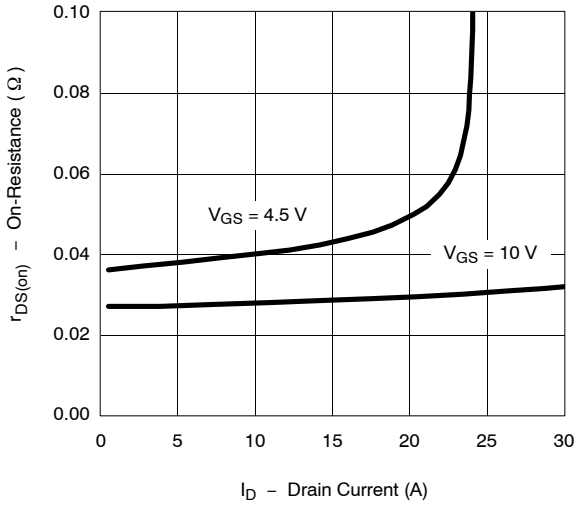
Output Characteristics



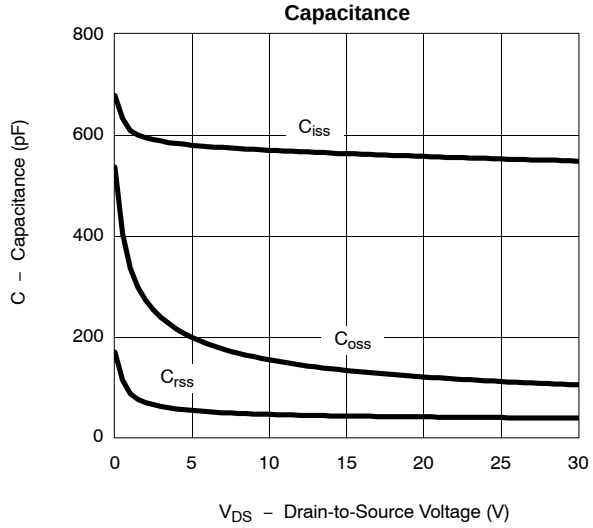
Transfer Characteristics



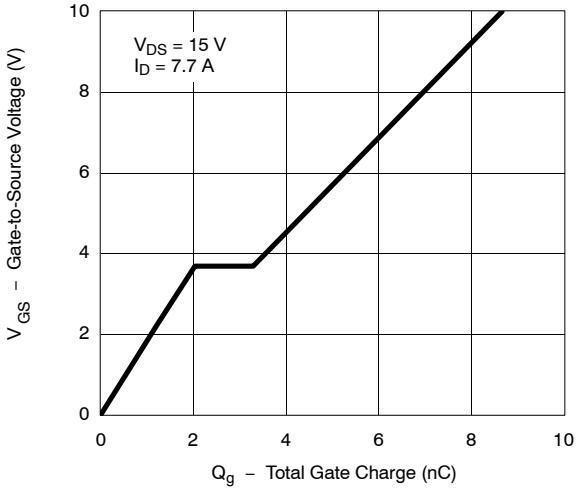
On-Resistance vs. Drain Current



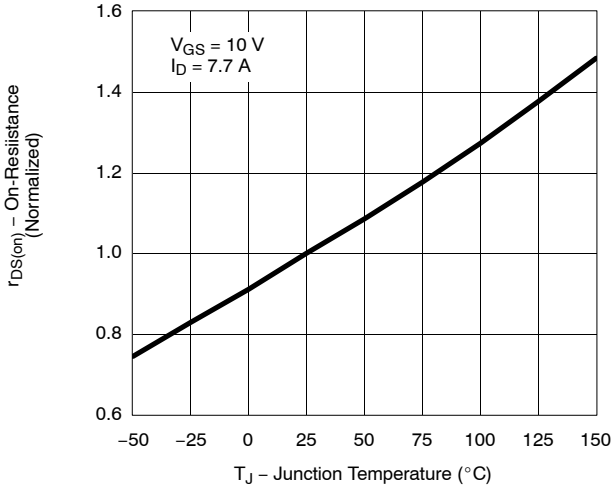
Capacitance



Gate Charge

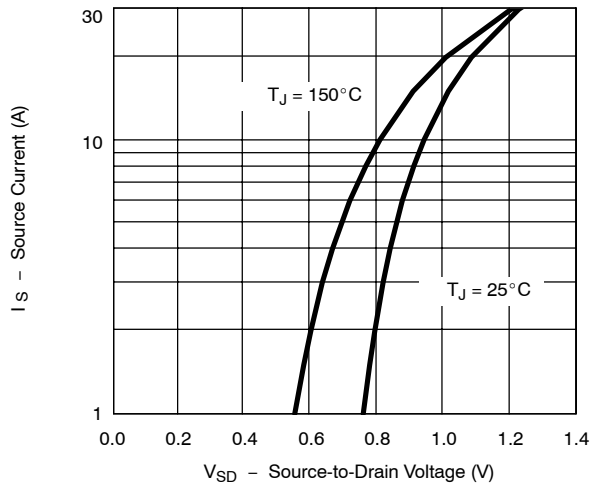


On-Resistance vs. Junction Temperature

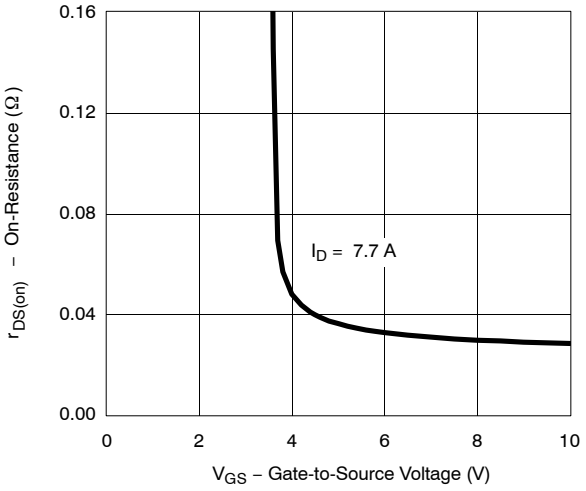


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

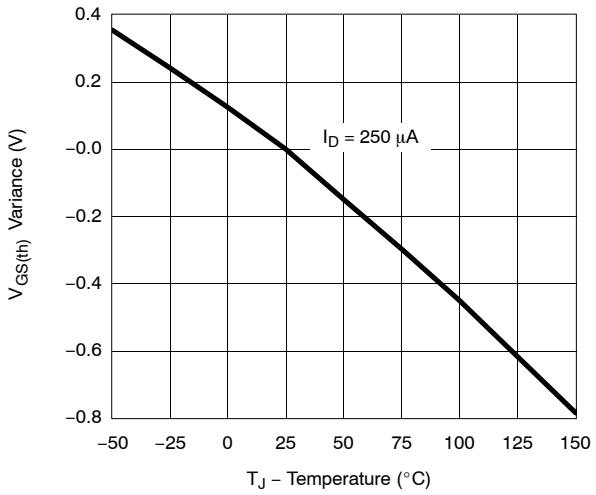
Source-Drain Diode Forward Voltage



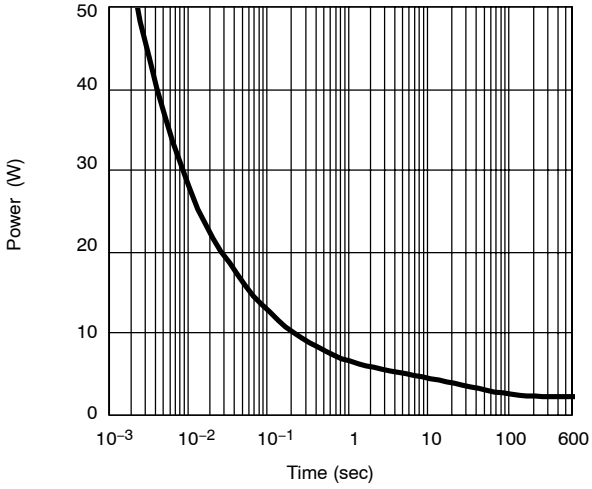
On-Resistance vs. Gate-to-Source Voltage



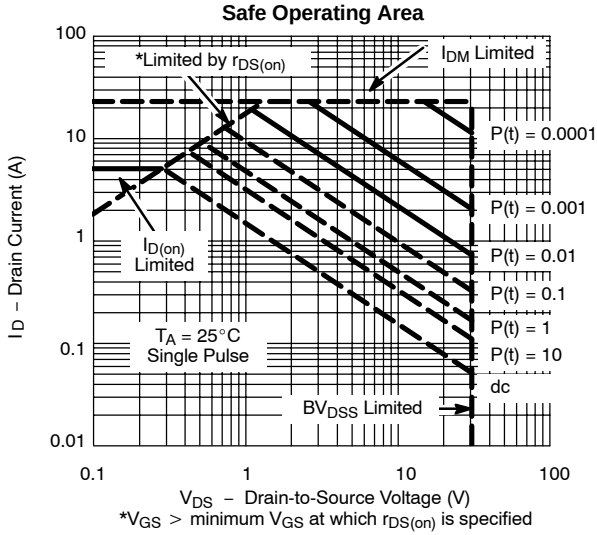
Threshold Voltage



Single Pulse Power

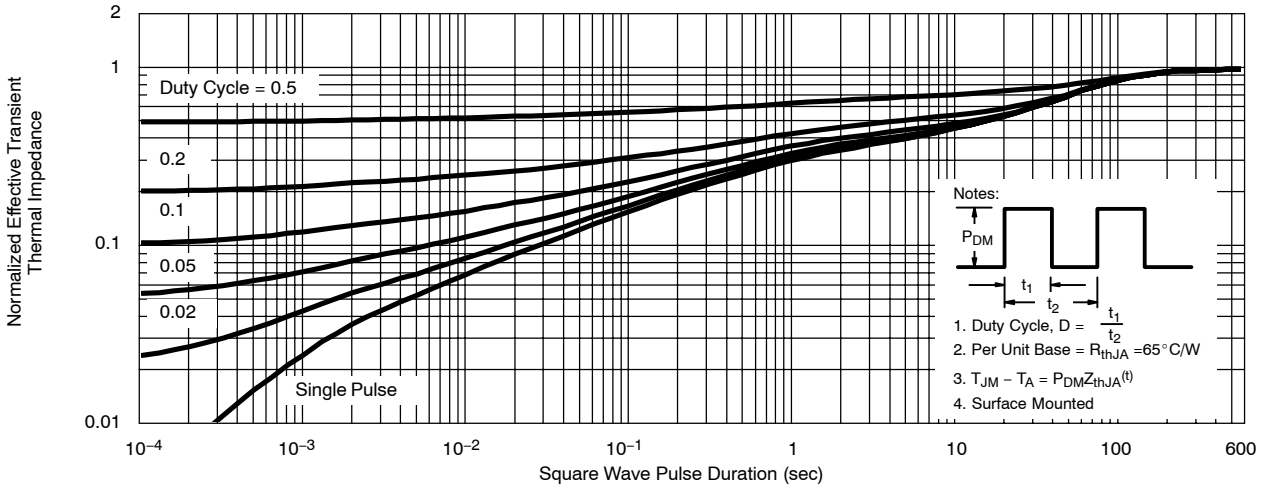


Safe Operating Area

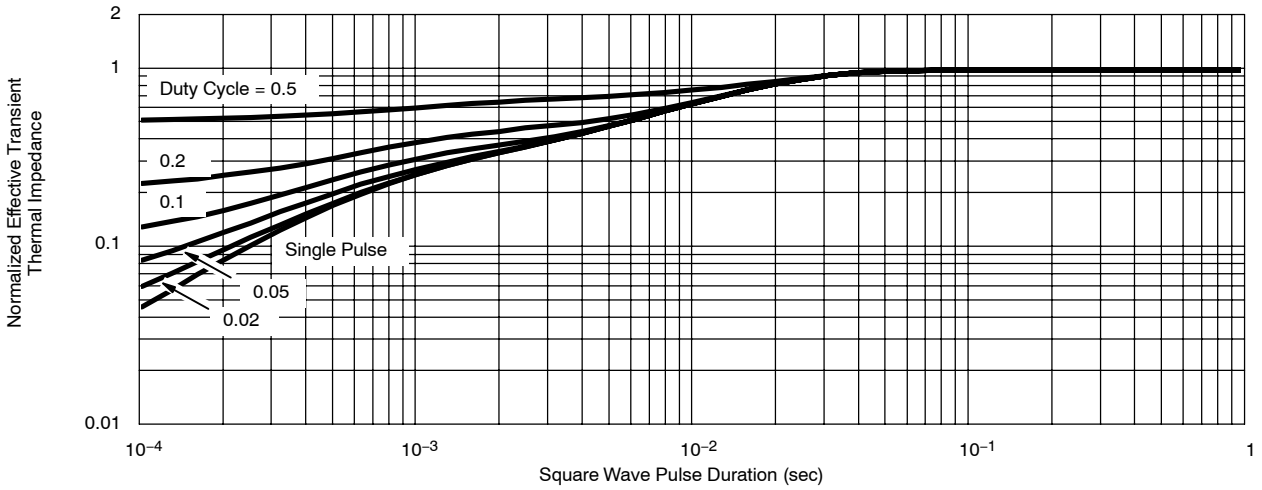


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



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