FEATURES

Easy software migration from industry leading AMCC NIAGARA FEC device

- Significant reuse of the Niagara register map in Rubicon.
- Superb migration path to lower power Rubicon-48 device.

Backwards compatible with AMCC's industry leading S3062 FEC device

- FEC and Framing compatible between Rubicon-48 and S3062.
- Superb migration path to better integration Rubicon-48 device.

G.709 ODU - 1 Synchronous and Asynchronous mapping

- 1 x OC – 48/STM-16 synchronous and asynchronous mapping (239,238).

G.709 Overhead processing

- Bi-directional add-drop ODU – 1.
- Bi-direction G.709 Overhead Processing for bi-directional OTU1 regeneration.
- Dedicated GCC ports.

Ingress and Egress SONET/SDH Performance Monitoring/ Injection

- 1 x OC-/48/12/3 TOH add-drop and processing.
- 8B/10B Monitoring.
- SONET/SDH section and line termination including full B2 recalculation.
- TOH add-drop port.
- LOS, OOF, LOF detection.
- B1, B2 monitoring with programmable Signal Degrade and Signal Fail thresholds.
- J0 Monitoring, SDH and SONET modes.
- Support for Protection Switching.
- K1, K2 monitoring for APS changes, line AIS and line RDI.
- Automatic, interrupt-driven, or manual AIS insertion.
- Frame boundary output.

Industry Standard RS(255,239) Forward Error Correction with 6.2 dB Coding Gain (at 10^{-15} CER)

- G.709 Compliant Frame Structure.
- Compatible with AMCC's S19203 (HUDSON) and S19208 (NIAGARA).
- Limited backwards compatibility with AMCC's S3062.

Enhanced Gain Forward Error Correction with G.709 ODU

- 2.7 Gbps enhanced FEC with > 8.6 dB coding gain.
- G.709 overhead processing and nominal rate expansion.
- Comprehensive channel statistics gathering including.
  - Corrected bits, bytes.
  - Corrected zeros, ones (with outputs).
  - Uncorrectable sub-frame count.

Broad Interface Compatibility

- 16-bit 155Mbps LVDS interface
- 4-bit 622Mbps LVDS interface
- Compatible with AMCC's DANUBE, MISSOURI, OHIO, RHINE, VOLTA, S3465, S3457, S3455, S3086 and S3485.
- Provides port swapping and output dual feed features for 1 + 1 line protection scheme.

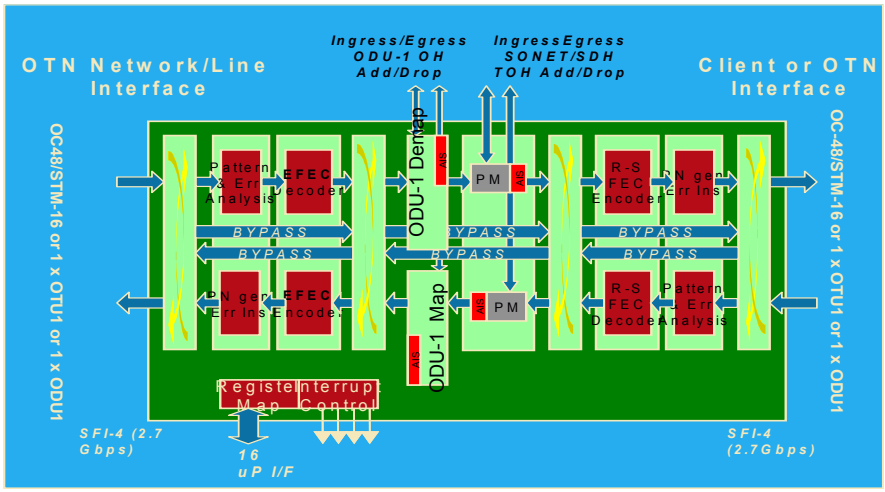
Support For System Test and Diagnostics

- Can synthesize SONET frames.
- Error injection capability for verification of remote error reporting.
- Test-set compliant pseudo-random sequence generation/analysis.
- Client and Line side loopback.

General Purpose Processor Interface

- Glueless 16-bit interface to MPC860, 25 MHz to 66 MHz. Dual mode interface also supports Intel processors.
- Interrupt driven or Polled mode operation.

Figure 1: Block Diagram



FINAL Information - The information contained in this document is about a product that has been fully tested, characterized, and is production release. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

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Additional Protocol Support

- FEC Frame Synchronous scrambling.
- Programmable sequence detection.

Pin Compatibility to Niagara device
Low Power.13 u CMOS Technology

- 1.2 Volt core operation.
- 2.5 Volt I/O.

APPLICATIONS

- SONET/SDH OC-48/STM-16 DWDM transport systems and DWDM metro networks.
- Transparent Add-Drop Multiplexing Transponder applications.
- Protocol Transparent Transport.
- IaDI to IrDI FEC transponder chip (6.2 dB gain network to > 8.6 dB gain network).

GENERAL DESCRIPTION

The AMCC Rubicon-48 device is a wide-area and metropolitan transport device aimed at next generation applications, required transparent mapping, and enhanced error correction capability. The device utilizes the ITU G.709 frame and overhead structures to enable deployment of full OTN compliant network elements. Rubicon-48 will support two gain rates, the standard G.975 based rate of 6.2 dB (raw optical coding gain), and AMCC's proprietary EFEC code, rated at greater than 8.6 dB (raw optical coding gain). The Rubicon-48 device is capable of running both these gains simultaneously, providing a superb single chip transponder solution for standard gain to enhanced gain networks. Note that the Rubicon-48 will employ the same industry leading EFEC code that was used in the AMCC Niagara device, making these devices totally compatible. The Rubicon-48 is targeted at 2.5G transport and will also support the framing and FEC code previously deployed in AMCC's industry leading S3062 FEC device, allowing for in-circuit upgrades of older systems.

DATA INTERFACES

Both the client and network interfaces support two interface modes, a 16-bit LVDS interface and a 4-bit LVDS interface. Data is transferred as either 16-bit LVDS parallel data or 4-bit LVDS parallel data with a synchronous clock. The defined low end of the parallel client/network interface is 31.25 Mbps (across 4 bits of the interface) for an aggregate bandwidth of 125 Mbps.

CLIENT PERFORMANCE MONITORING

A SONET/SDH performance monitor supporting OC-48/12/3 and SDH-16/4/1 rates is provided to perform optional-section and limited-line termination functions. TOH for the SONET signal is dropped and added. On chip processing of the critical TOH functions, such as B1, B2, J0, is provided to enable functioning as a SONET/SDH network element. The performance monitor may also be configured to provide non-intrusive monitoring while transparently passing through the received signal with no overwrite. The 2.5 Gbps client signal may be synchronously or asynchronously mapped into the ODU-1 payload. FEC parity check bytes are then optionally added to form the OTU-1. The device can also output the ODU-1 with no parity check bytes. In the receive direction, data is de-mapped from the OTU-1 and control signals are provided to enable timing regeneration of the client 2.5 Gbps signal.

When operating in the ITU G.709 OTU-1 or ODU-1 mode, the SONET monitors are bypassed. On-chip processing of the G.709 overhead is provided to enable single chip G.709 section termination. G.709 Overhead can be added or dropped as required. Remapping required for synchronization of asynchronous ODU-1 signals is not supported.

Client-signal monitoring for 8B/10B encoded data is also provided.

AIS SUPPORT

For applications in which the client signal is SONET or SDH, the Rubicon-48 can generate a SONET/SDH AIS on both the client ingress and the egress.

For applications in which the client signal is G.709 compliant or for OTN regenerator applications, Line Fail and un-equipped OTN AIS is supported. For OTN edge applications, the device can be provisioned to provide either a SONET/SDH AIS or a OTN Generic AIS to the client. This facilitates convergence of the SONET/SDH and OTN functions into a single network element.

ODU MAPPING

ITU compliant client mapping of SONET OC-48 or SDH STM-16 into the ODU-1 signal is supported whereby a G.709 overhead byte is added to every G.709 sub-frame resulting in an ODU rate expansion of (239/238). The chip can be configured to insert the G.709 compliant overhead byte value or to insert user data into this location. The values assigned to the stuff bytes can be defined either from a register set on chip or from an external add-drop port.

Start-of-frame signals are provided at the input and output ports to enable synchronization to the ODU.

LOOPBACK FUNCTIONS

Near-end and far-end loopback is supported for each of the client interfaces and for the line interface. This enables line and device testing and fault isolation. Each functional block may be bypassed as required to support the application. When all blocks are bypassed, the device allows transparent pass-through of client data (assuming synchronous inputs).

Key status and alarm signals are provided to outside pins to enable rapid response to failure conditions. These include but are not limited to: LOS, OOF, LOF, B1 Errors, and FEC errors. Three interrupt pins, each with a mask register are provided to enable prioritization of interrupts and timely interaction with firmware.

In addition to the loopback capabilities of the device, the Rubicon-48 also employs a unique port swapping capability allowing the physical ports on the device to be interfaced to either side of the FEC encoders. This capability increases the flexibility of a single board design used in a variety of modes.

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FORWARD ERROR CORRECTION CAPABILITY

Two FEC options are supported on the line side. The Rubicon-48 can support standard RS(255,239) FEC compliant with G.709, G.975, and compatible with the AMCC Hudson device. The device can also support an enhanced FEC algorithm that is applied using the same G.709 frame structure and rate as the Hudson but providing more than 2 dB of additional coding gain (*measured at a BER of 10^{-15}). The Rubicon-48 device will operate in a mode where both encoders and decoders are working simultaneously, allowing for a single chip transponder to operate between two networks with different gain characteristics.

LEGACY COMPATIBILITY

As indicated above, the Rubicon-48 also supports operation in the G.975 mode. In this mode, the G.709 overhead processing can be inhibited and direct access to the non-framing bytes in the overhead column is provided through the pins on the device. The device operates in the 255,238 mapping mode with no stuff columns inserted in the FEC payload.

There is also some limited backwards compatibility with the S3062 device, AMCC's first generation 2.5G FEC device. The details of this backwards compatibility are outlined in the full Rubicon-48 datasheet.

CONTROL INTERFACE

A general purpose 16-bit microprocessor interface is provided for control and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either interrupt driven or polled-mode configurations.

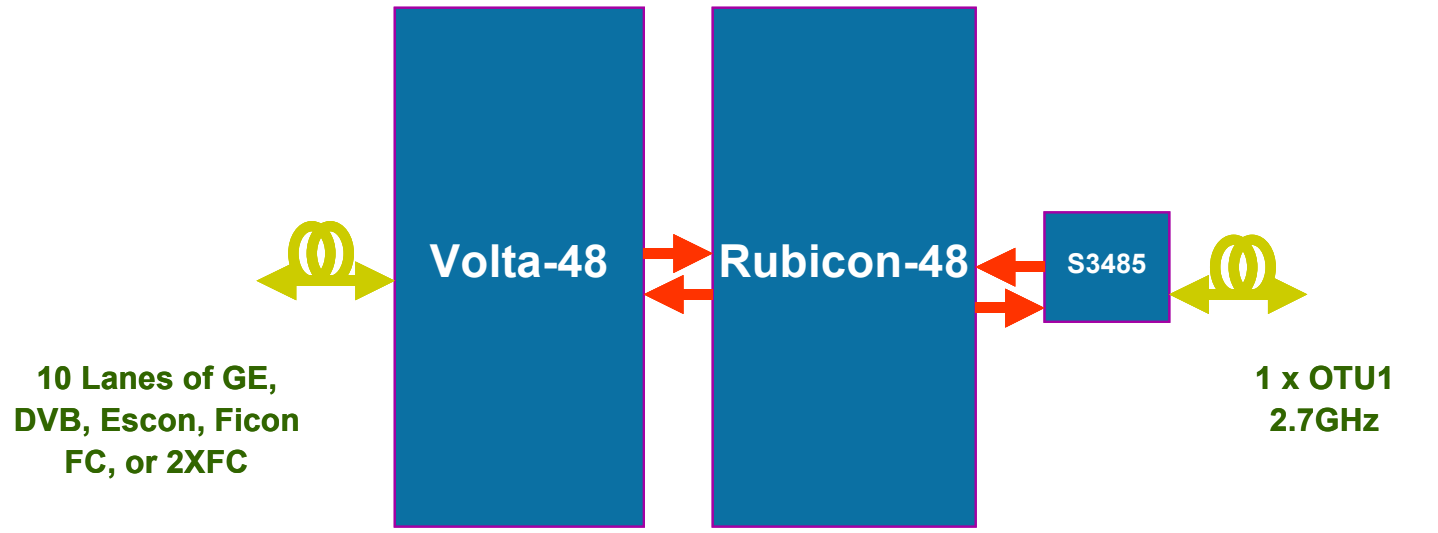
APPLICATION DIAGRAMS

Figure 2: Multi-Protocol LAN Transport

Figure 2 shows the Rubicon-48 in an edge transponder application. The client side signals are first mapped into virtually concatenated SONET streams. The Volta-48 supports a variety of client side signals including GE, FC, 2XFC, DVB, Ficon and Escon. In addition to the flexible client interface on the Volta-48, the chip also supports fractional GE interfaces, allowing a less than full rate GE client to be transported. The Volta-48 also includes an independent wide range CDR on each client input, allowing the chip to interface directly to the client optics module. Once the client payloads have been mapped into VC SONET streams, an STS48 signal is presented on the high speed or line side of the Volta-48.

The Rubicon-48 then monitors and wraps it's client signal into an ODU-1 payload and appends the GFEC or EFEC code necessary for transport. The PHY interface is achieved with the S3485 CMOS transciever.

Figure 2: Multi-Protocol LAN Transport



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