Hittite MICROWAVE CORPORATION v01.0507

HMC543

22.5° MMIC 4-BIT DIGITAL PHASE SHIFTER, 8 - 12 GHz

Typical Applications

The HMC543 is ideal for:

- EW Receivers
- Weather & Military Radar
- Satellite Communications
- Beamforming Modules

Features

Low RMS Phase Error: 5°

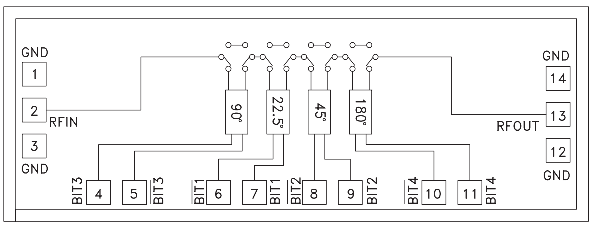
Low Insertion Loss: 6.5 dB

Excellent Flatness

360° Coverage, LSB = 22.5°

Die Size: 0.99 x 2.46 x 0.1 mm

Functional Diagram



General Description

The HMC543 is a 4-bit digital phase shifter die which is rated from 8 to 12 GHz, providing 0 to 360 degrees of phase coverage, with a LSB of 22.5 degrees. The HMC543 features very low RMS phase error of 5 degrees and extremely low insertion loss variation of ±0.8 dB across all phase states. This high accuracy phase shifter is controlled with complementary logic of 0/-3V, and requires no fixed bias voltage and is internally matched to 50 Ohms with no external components. Simple external level shifting circuitry can be used to convert a positive CMOS control voltage into complementary negative control signals.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Control Voltage = 0/-3V

Parameter	Min.	Typ.	Max.	Units
Frequency Range	8		12	GHz
Insertion Loss*		5	7	dB
Input Return Loss*		10		dB
Output Return Loss*		10		dB
Phase Error*		±10	±15	deg
RMS Phase Error		5		deg
Gain Variation*		±0.8		dB
Input Power for 1 dB Compression	21	24.5		dBm
Input Third Order Intercept		40		dBm
Control Voltage Current		<2		mA

*Note: All States Shown

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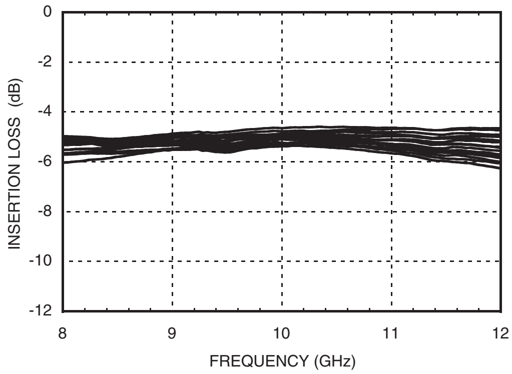
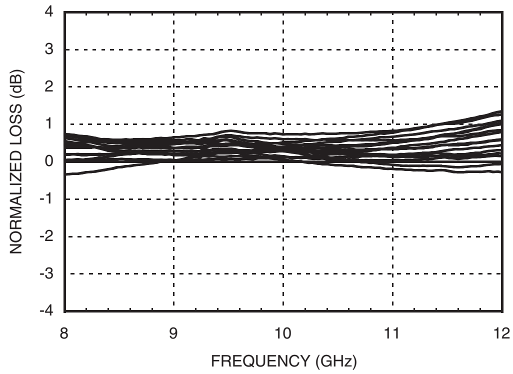
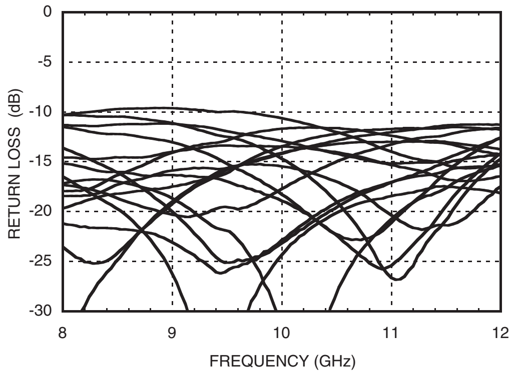
Insertion Loss, All States



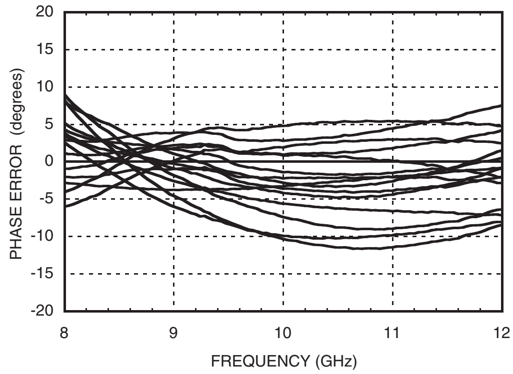
Normalized Loss, All States



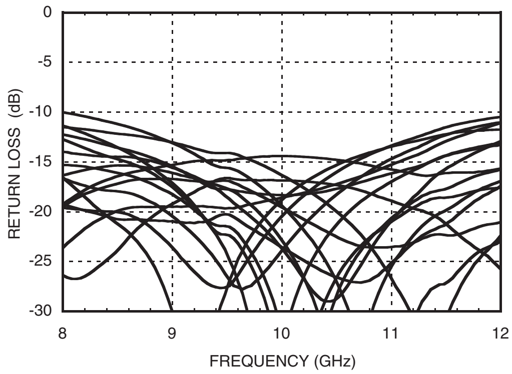
Input Return Loss, All States



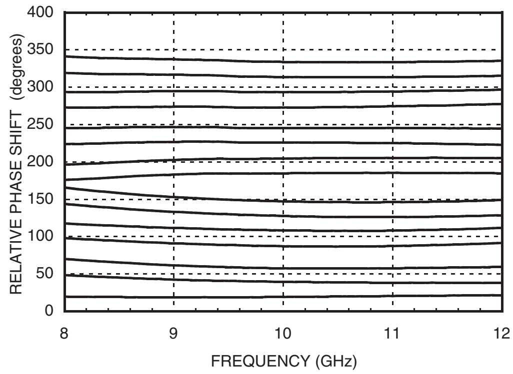
Phase Error, All States



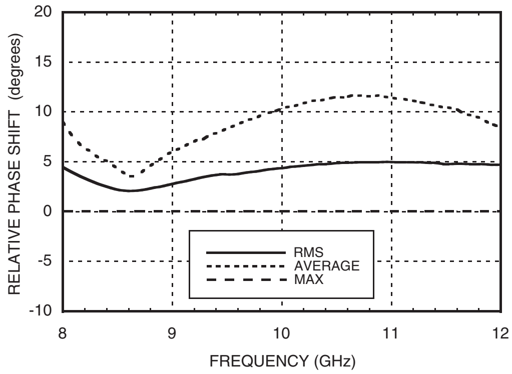
Output Return Loss, All States



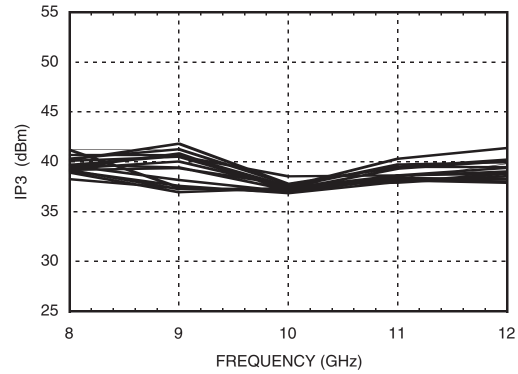
Relative Phase Shift, All States



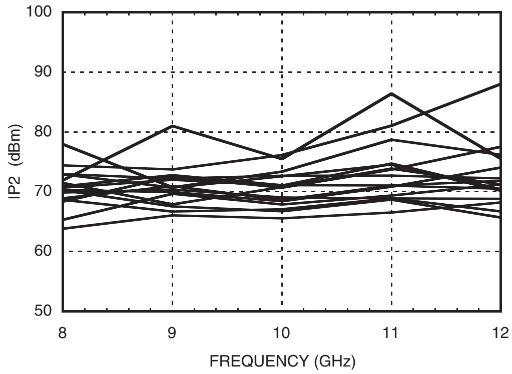
Relative Phase Shift, RMS, Average, Max, All States



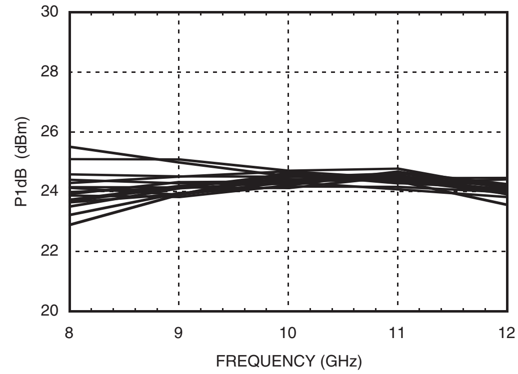
Input IP3, All States



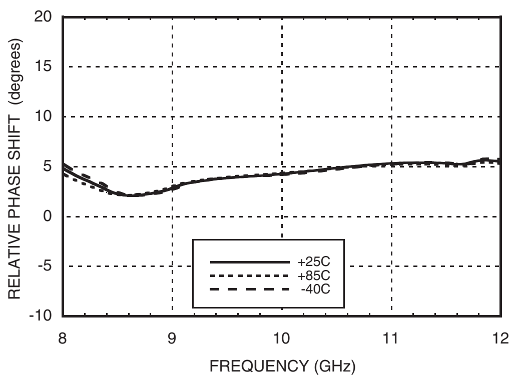
Input IP2, All States



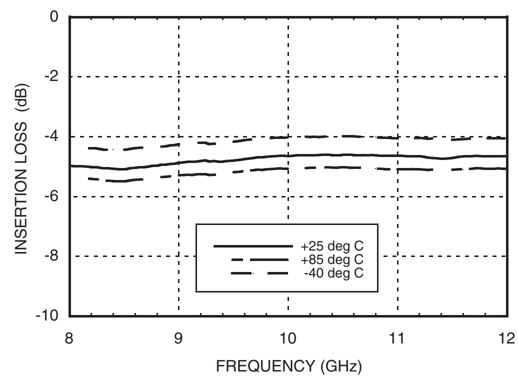
Input P1dB, All States



RMS Phase Error vs. Temperature

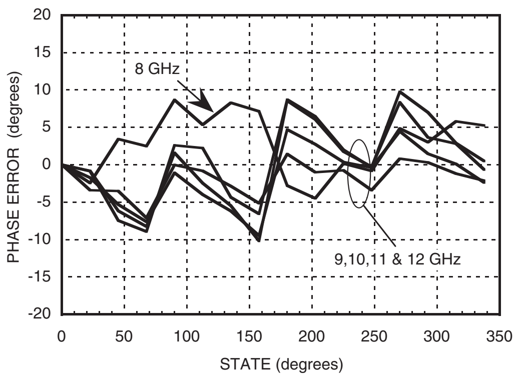


Maximum Insertion Loss vs. Temperature



22.5° MMIC 4-BIT DIGITAL PHASE SHIFTER, 8 - 12 GHz

Phase Error vs. State



Absolute Maximum Ratings

Input Power (RFin) (8-12 GHz)	+27 dBm (T= +85 °C)
Channel Temperature (Tc)	150 °C
Thermal Resistance (channel to die bottom)	130 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Control Voltage

State	Bias Condition
Low (0)	-2.5 to -3.5V @ 0.4 µA Typ.
High (1)	0 to +0.3V @ 0.4 µA Typ.

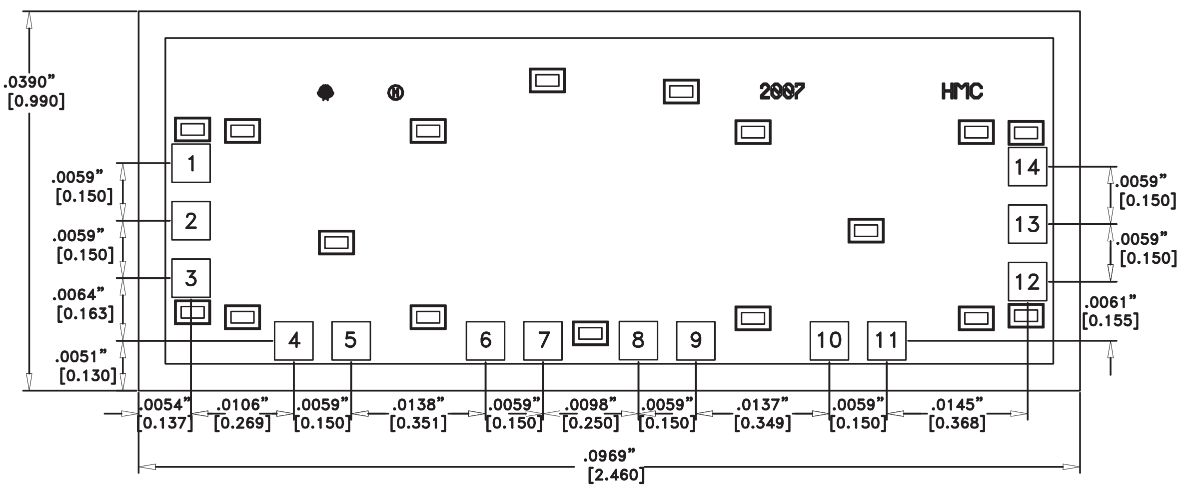
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Truth Table

Control Voltage Input								Phase Shift (Degree) RFIN - RFOUT
Bit 1	$\overline{\text{Bit 1}}$	Bit 2	$\overline{\text{Bit 2}}$	Bit 3	$\overline{\text{Bit 3}}$	Bit 4	$\overline{\text{Bit 4}}$	
0	1	0	1	0	1	0	1	Reference
1	0	0	1	0	1	0	1	22.5
0	1	1	0	0	1	0	1	45.0
0	1	0	1	1	0	0	1	90.0
0	1	0	1	0	1	1	0	180.0
1	0	1	0	1	0	1	0	337.5

Any combination of the above states will provide a phase shift approximately equal to the sum of the bits selected.

Outline Drawing



Die Packaging Information [1]

Standard	Alternate
GP-2	[2]

[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. DIE THICKNESS IS 0.007
3. TYPICAL BOND PAD IS 0.004 SQUARE
4. BACKSIDE METALLIZATION: GOLD
5. BACKSIDE METAL IS GROUND
6. BOND PADS METALLIZATION: GOLD
7. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
8. OVERALL DIE SIZE ±0.002

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

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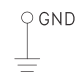
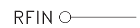
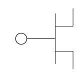
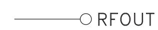
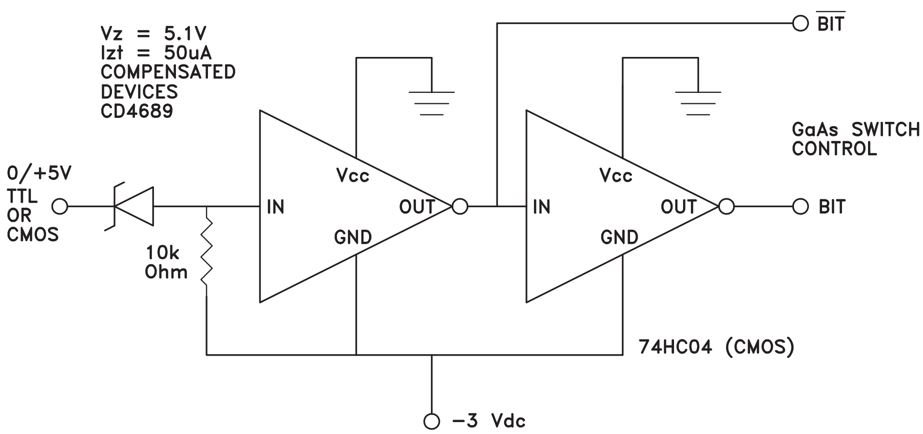
Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1, 3, 12, 14	GND	These pins and die bottom must be connected to RF/DC ground.	
2	RFIN	This port is matched to 50 Ohms.	
4, 7, 9, 11	BIT3, BIT1, BIT2, BIT4	Non-Inverted Control Input. See truth table and control voltage tables.	
5, 6, 8, 10	$\overline{BIT3}$, $\overline{BIT1}$ $\overline{BIT2}$, $\overline{BIT4}$	Inverted Control Input. See truth table and control voltage tables.	
13	RFOUT	This port is matched to 50 Ohms.	

Application Circuit



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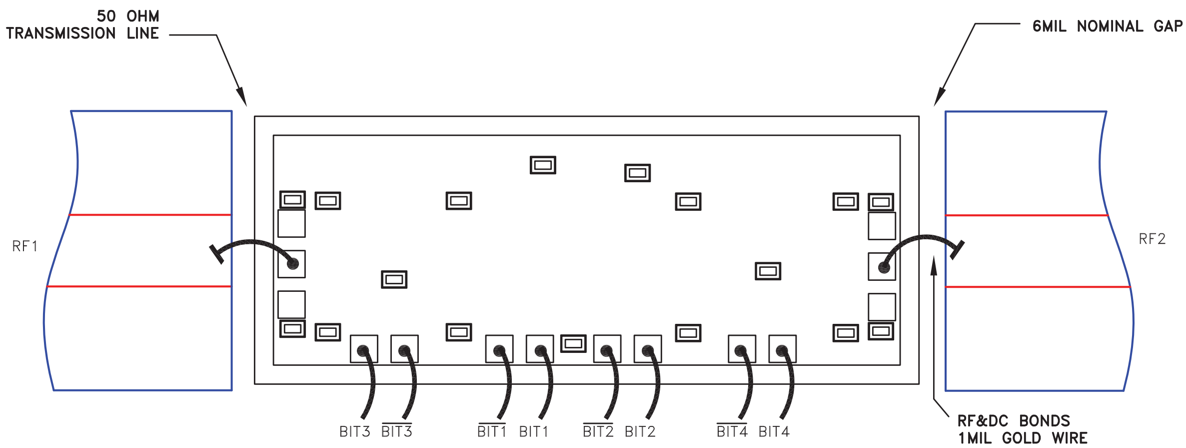
Assembly Diagram



Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against > ± 250V ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).

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Notes