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MindController™ OC-12 ATM Shaper

M27651

OC-12 ATM Traffic Shaper

The M27651 provides ATM layer traffic shaping, Operations, Administration, and Maintenance (OAM) processing, header translation, and statistics at OC-12 rates. Up to 64K connections are supported.The M27651 is a part of the MindController™ family of Application Specific Network Processors (ASNPs) that provide flexible, easy to upgrade network solutions at competitive prices.

KEY FEATURES

- OC-12 throughput
- ATM Forum TM 4.0-compliant traffic shaping supports CBR, VBR and UBR QoS classes
- Shaping rates configurable from 22 cells per second to line rate, with accuracy to within one percent
- I.610-compliant OAM (F4/F5 alarms, loopback, continuity check, activation)
- Per-connection queuing with EPD and PPD
- Per-buffer class and per-connection thresholds
- VP (or tunnel) shaping of channel-switched VCs
- Weighted round robin (WRR) access on unshaped connections
- ATM cell header translation
- Per-PHY and per-connection statistics
- Supports 64K connections
- Supports UTOPIA Level I/II ATM cell interfaces
- Cell insertion and extraction via host

Traffic Shaping

The traffic-shaping function provides two generic cell rate algorithms (GCRAs) per connection,and conforms with CBR.1, VBR.1, UBR.1 and UBR.2 as defined in the ATM Forum TM 4.0 specification. Shaping is enabled on a per-connection basis. Connection rates from 22 cells per second to line rate are shaped to within one percent ofthe desired value.

In addition to shaping VCs individually, arbitrary groups of VCs can also be shaped as a whole. This feature is useful at VP end-points to shape a collection of VCs using the traffic parameters ofthe associated VP.

Cells on unshaped connections are sent when nothing else is scheduled, allowing full use ofthe available line rate. Weighted round robin (WRR) access is provided on these connections to ensure fairness.

OAM Processing

The M27651 supports the fault management (alarm indication signal (AIS), and remote defect indication (RDI)), continuity check, activation/deactivation, and loopback OAM functions for both path (F4) and channel (F5) levels.

Congestion Management

Cells beginning the traffic shaping process are stored in per-VC queues. The queues are constructed using buffers from up to 16 buffer classes. The size of each buffer class is configurable at initialization,with a maximum buffer memory size for all classes of 512 Mbytes. Cells are mapped to a buffer class on a per-connection basis, with each class typically representing an ATM quality of service (QoS) (e.g., CBR, rtVBR, nrtVBR or UBR).

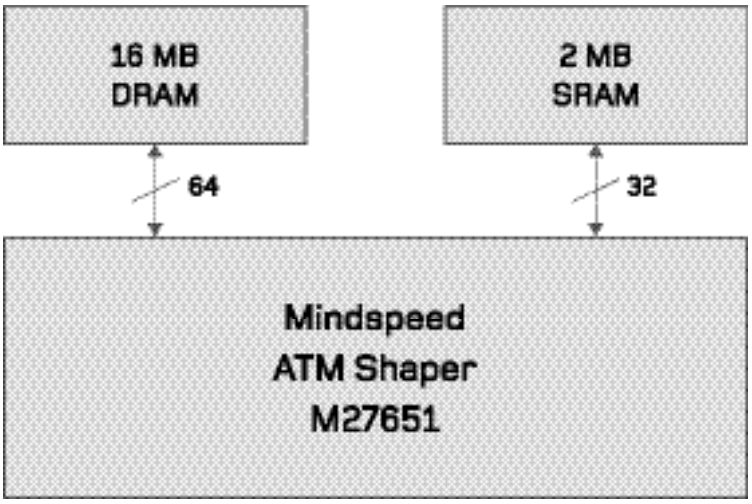
Two configurable per-buffer class thresholds (CLP1 and CLP01) and a per-connection threshold (CLP01) are provided. Cell discard occurs (based on the CLP bit) when any of these thresholds are exceeded, or when the buffer limit is reached. EPD is optionally applied on AAL5 connections when a CLP01 threshold is exceeded. PPD is optionally applied on AAL5 connections when the buffer limit is reached.

Header Translation

The M27651 supports the standard 53-byte UNI and NNI cell formats. For channel-switched connections (VCs and VP endpoints), the VPI and VCI fields in the ATM cell header are replaced with new values. For path-switched connections (VP midpoints), only the VPI is replaced.The PTI and CLP fields from input cells are copied and modified as appropriate.

Statistics

The M27651 provides the following statistics: aggregate cell count, total discards, AAL5 packets and OAM cells. All counters are available on a per-PHY and per-channel basis.



Memory Configuration

Memory Configuration

The M27651 requires external memory for channel context, cell buffer storage, and program and variable storage. A typical application using 64K connections would consist of 16 Mbytes ofDRAM for context and cell buffer storage, and 2 Mbytes ofSRAM for program and variable storage.

Applications

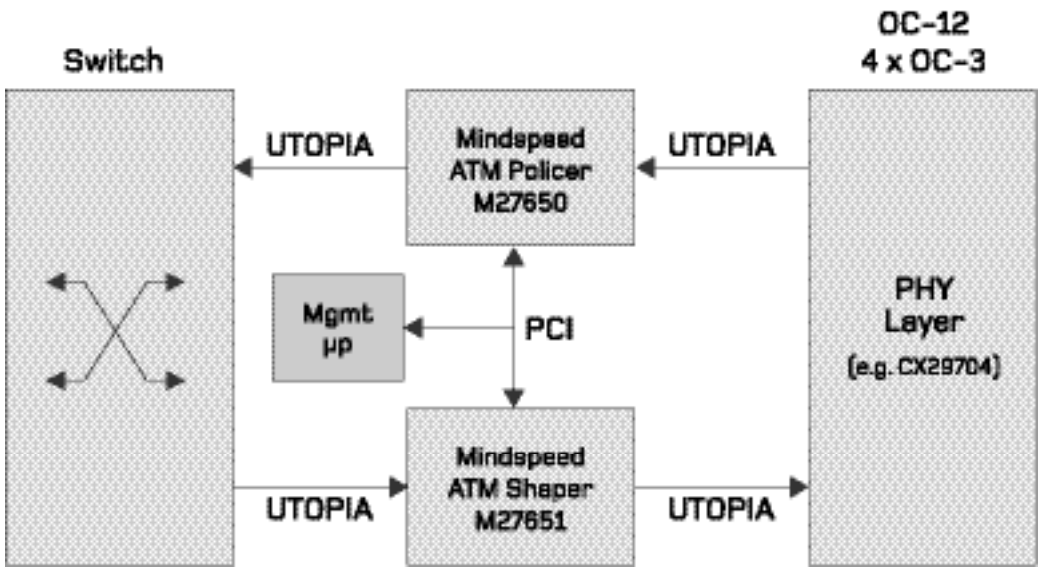
The M27651, when used in conjunction with the M27650 ATM Policer, forms a complete OC-12 ATM-layer solution. It can also be used as a stand-alone device, when only shaping functions are required. Typical applications include ATM switches, routers, multiservice edge concentrators, DSLAMs and wireless base stations.

Management Functions Via Host

A host processor controls the M27651. The host issues commands via the PCI bus, and receives results back through indications. Commands are available to open, close or modify the following: PHY ports, channels and tunnels. Additional commands get per-PHY or per-channel statistics, get or set the OAM state, and get or set buffer class thresholds. The host can also send or receive cells to or from any channel.

Support

Hardware simulation models (SWIFTand Verilog), test benches, bus functional models, IBIS models and a reference design are available. Reference code is provided to facilitate host application integration. A comprehensive set ofdiagnostics is provided to assist with testing.



System Block Diagram

Product Highlights

Functions

- ATM Forum TM 4.0–compliant traffic shaping
- OC–12 throughput
- Supports 64K connections
- Dual GCRAs per connection
- Supports the following conformance definitions:
  - CBR.1
  - VBR.1
  - UBR.1
  - UBR.2
- Shaping rates configurable from 22 cells per second to line rate, with accuracy to within one percent
- Per–connection queuing with EPD and PPD
- Per–buffer class and per–VC buffer thresholds
- Supports both VP and VC switching
- VP (or tunnel) shaping ofchannel–switched VCs
- WRR access on unshaped connections
- ATM header translation
- I.610 OAM processing
  - F4/F5 alarms (with escalation)
  - Loopback
  - Continuity check
  - Activation/deactivation
- Cell insertion and extraction
- Per–connection and per–port statistics
  - Aggregate cell count
  - –Total discards
  - AAL5 packets
  - OAM cells

Physical Interfaces

UTOPIA

- Level II–compliant,1–31 ports
- Master or slave mode
- Configurable as 8/16/32–bit bus Tx/Rx
- Registered mode for high speeds
- Independently clocked to 100 MHz
- 2.5 Gbps bandwidth

PCI

- Revision 2.2/2.1–compliant
- 32–bit bus
- Independently clocked to 66 MHz
- 266 Mbps peak bandwidth
- PCI master and slave (target)

External Memory

SDRAM

- 16–256 MB
- 64 bits wide
- Independently clocked up to 100 MHz

SRAM

- 2 MB
- 32 bits wide
- Core frequency operation up to 132 MHz
- Eight–word write buffer

Device Information

- Power supply: 3.3 V, 2.5 V
- I/O voltage levels: 3.3 V
- Typical power dissipation: 3.9 W
- Package: 474 CBGA
- Body size: 32.5 x 25 mm
- Ball pitch: 1.27 mm
- Θja(°C/W): 12.6 still air; 9.9 at 200 FPM
- Operating temperature: –40°C to +85°C
- Maximum device junction temperature: 110°C

Ordering Information

M27651: M27651–13

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U.S.and Canada: (800) 854-8099
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