

June 1992 Revised November 1999

100201

Low Power 2-Input OR/NOR Gate/Inverter

General Description

The 100201 is a 2-input OR/NOR Gate and a single Inverter Gate in an eight pin SOIC package. All inputs have 50 $k\Omega$ pull-down resistors and all outputs are buffered. The 100201 is ideal for single gate needs or for use as the feedback loop of a crystal oscillator circuit.

Features

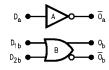
- Small 8 lead 150 mil SOIC package
- 2000V ESD protection
- 300 MHz minimum F toggle
- Temperature compensated
- Voltage compensated operating range = -4.2V to -5.7V V_{FF}

Ordering Code:

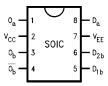
Order Number	Package Number	Package Description
100201SC	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.50" Narrow

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description					
D _a , D _{1b} , D _{2b}	Data Inputs					
O _b	Data Outputs					
\overline{O}_a , \overline{O}_b	Complementary Data Outputs					

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

 $\begin{array}{ll} \mbox{Operating Temperature ($T_{\rm C}$)} & \mbox{0°C to +85°C} \\ \mbox{Supply Voltage ($V_{\rm EE}$)} & -5.7\mbox{V to -4.2V} \end{array}$

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 3)

 $V_{EE} = -4.2 V$ to $-5.7 V,~V_{CC} = GND,~T_{C} = 0 ^{\circ} C$ to $+85 ^{\circ} C$

Symbol	Parameter	Min	Тур	Max	Units	Conditions		
V _{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with	
V _{OL}	Output LOW Voltage	-1830	-1705	-1620	mV	VIN - VIH(Max) Of VIL(Min)	50Ω to −2.0V	
V _{OHC}	Output HIGH Voltage	-1035			mV	V V or V	Loading with	
V _{OLC}	Output LOW Voltage			-1610	mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	50Ω to -2.0V	
V _{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs		
V _{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs		
I _{IL}	Input LOW Current	0.50			μΑ	$V_{IN} = V_{IL(Min)}$		
I _{IH}	Input HIGH Current			240	μΑ	$V_{IN} = V_{IH(Max)}$		
I _{EE}	Power Supply Current	-29	-17	-15	mA	Inputs OPEN		

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

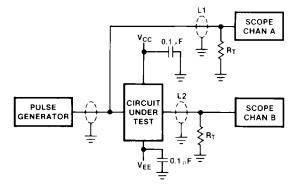
SOIC AC Electrical Characteristics

 $V_{\text{EE}} = -4.2 \text{V to } -5.7 \text{V}, \, V_{\text{CC}} = \text{GND}$

Symbol	Parameter	T _C = 0°C		$T_C = +25^{\circ}C$		T _C = +85°C		Units	Conditions
Oymboi		Min	Max	Min	Max	Min	Max	Onito	Conditions
t _{PLH}	Propagation Delay	0.4	1.10	0.4	1.15	0.4	1.20	ns	Figure 1Figure 2
t_{PHL}	Data to Output	0.4							(Note 4)
t _{TLH}	Transition Time	0.40	0.40 1.20	0.40 1.20	1.20	0.40	1.20	ns	Figure 1Figure 2
t_{THL}	20% to 80%, 80% to 20%	0.40			1.20	0.40			rigule irigule 2

Note 4: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Test Circuitry



Notes:

 V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

 $R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

 C_L = Fixture and stray capacitance \leq 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

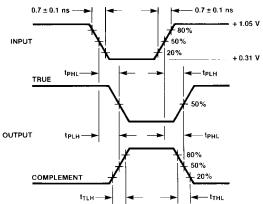
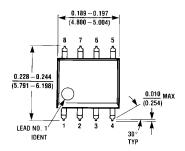
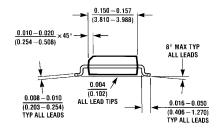
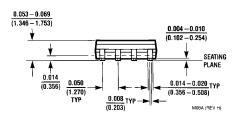


FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted







8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M08A

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