

M56770SP/FP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

DESCRIPTION

The M56770SP/FP is a semiconductor integrated circuit, with an oxide-film separated ECL/PL PLL frequency synthesizer. The prescaler and PLL, with a maximum operating frequency of 1.0 GHz, are housed on a single chip.

FEATURES

- Built-in prescaler with input amplifier ($f_{max}=1.0\text{GHz}$)
- Low power dissipation ($I_{cc}=30\text{mA}$ at $V_{cc}=5\text{V}$)
- Fine tuning capability (31.25kHz/step)
- PLL lock/unlock status display output
- Serial data input (2 or 3 data transfer lines)

APPLICATION

TV and VCR tuners

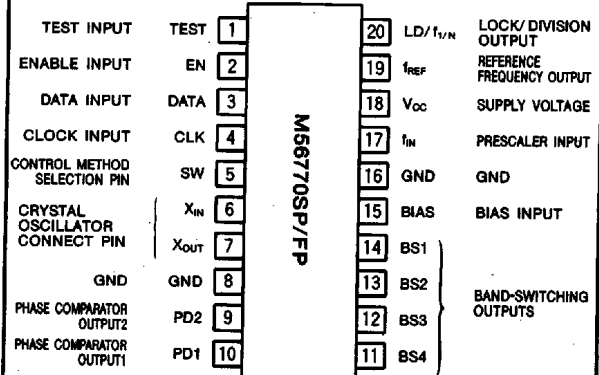
RECOMMENDED OPERATING CONDITION

Supply voltage range.....4.5~5.5V
 Operating frequency(1).....4MHz(Typ)
 (Crystal oscillator circuit)
 Operating frequency(2).....80~1000MHz(f_{in} input)
 Output low-level current.....2mA(Max)(Pin ①②)
 Band output low-level current 1mA(Max)(Pin ⑪⑫⑬⑭)

FUNCTION

The M56770SP/FP is a PLL frequency synthesizer IC for TVS and VCRs. The prescaler is realized in emitter-coupled logic,

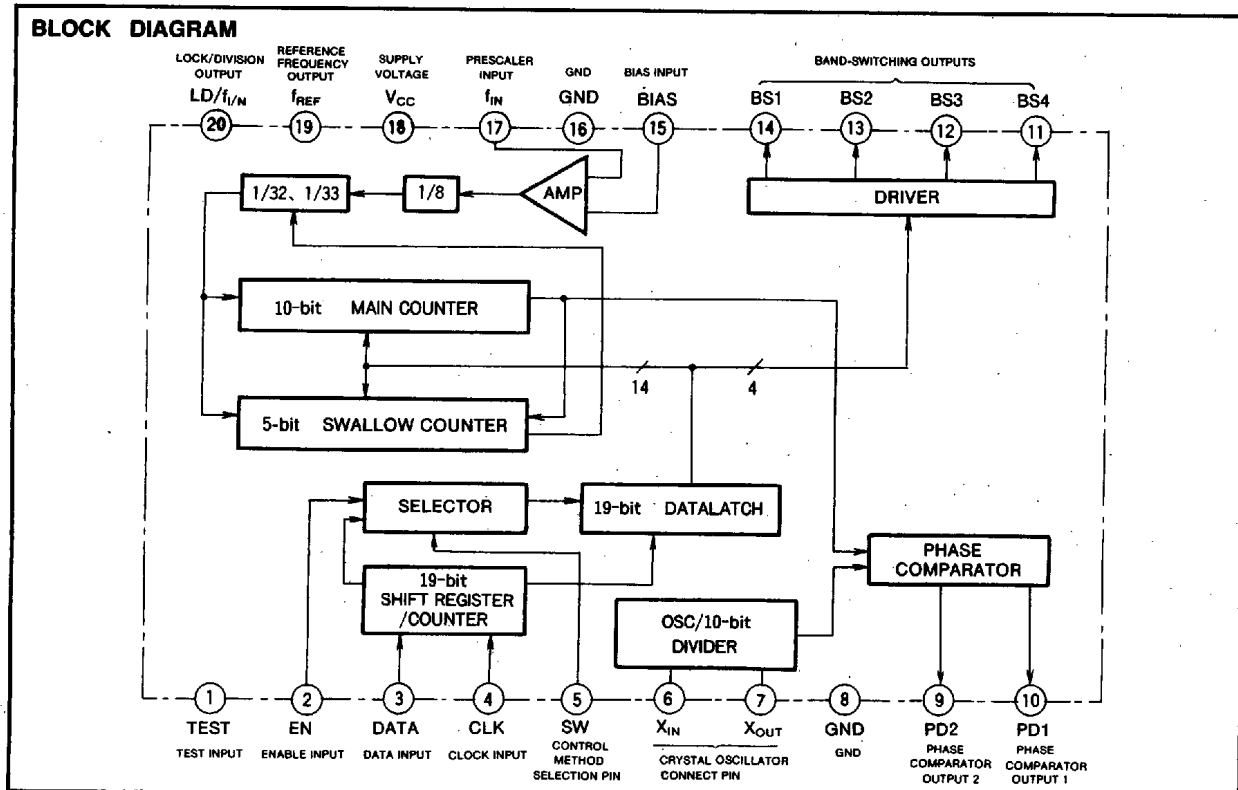
PIN CONFIGURATION (TOP VIEW)



Outline 20P4B(SP)
20P2N-A(FP)

and the PLL in integrated injection logic. The maximum operating frequency of the prescaler is 1.0 GHz. The first stage is a fixed 1/8 prescaler and the second stage is a 1/32 1/33 dual-modulus prescaler. The PLL consists of a 4MHz crystal oscillator, a 10-bit reference frequency divider, a programmable divider (a 10-bit M counter and a 5-bit S counter), a phase comparator, and a lock detector. Four band-switching circuits are also provided.

BLOCK DIAGRAM



SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings		Unit
		Min.	Max.	
V _{CC}	supply voltage	-0.5	6.5	V
V _I	input voltage	-0.5	6.5	V
V _{O1}	Output voltage (1) PD output	-0.5	5.5	V
V _{O2}	Output voltage (2) Other than above	-0.5	6.5	V
V _{BD}	Output withstanding voltage		13	V
P _d	Power dissipation		550	mW
T _{opr}	Operating temperature	-20	75	°C
T _{stg}	Storage temperature	-40	125	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test pin	Test Conditions	Limits			Unit
				Min.	Typ.	Max.	
V _{IH}	High-level input voltage	1, 2, 3, 4, 5		2.0		V _{CC} +0.3	V
V _{IL}	Low-level input voltage	1, 2, 3, 4, 5				0.7	V
I _{IH1}	High-level input current 1	1, 3, 4, 5, 2	V _{CC} =5.5V, V _I =2.7V			50	μA
I _{IL1}	Low-level input current 1	1, 3, 4, 5, 2	V _{CC} =5.5V, V _I =0.4V		-100	-200	μA
V _{IC}	Input clamp voltage	1, 2, 3, 4,	V _{CC} =4.5V, I _{IC} =-1.0mA		-1.3	-1.8	V
V _{OL}	Low-level output voltage	19, 20	V _{CC} =4.5V, I _{OL} =2mA		0.3	0.5	V
I _{OLK1}	Output leak current	PD output	10	V _{CC} =5.5V, V _O =0.5~4.8V	-1.0	+1.0	μA
I _{OLK2}		BS output	11~14	V _{CC} =4.5V, V _O =12V		+10	μA
I _{OLK3}		Other than above	19, 20	V _{CC} =5.5V, V _O =5.5V		+10	μA
I _{CC}	Supply current	18	V _{CC} =5.5V		30	55	mA

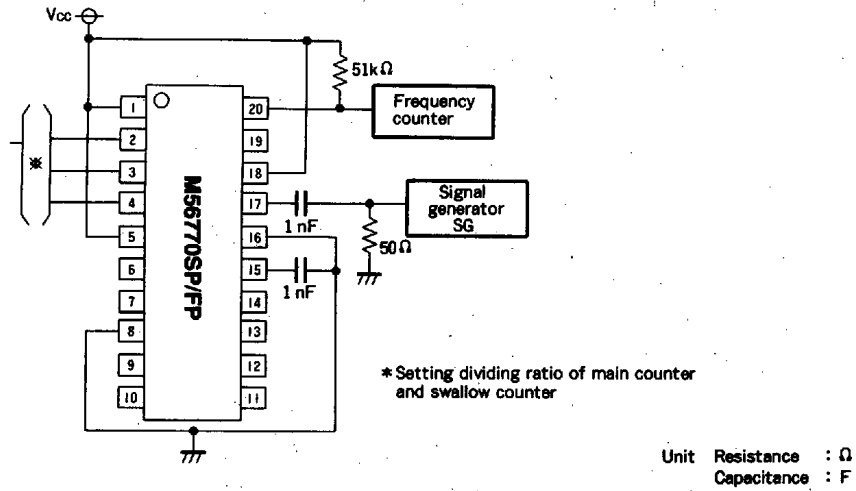
Typical values are at V_{CC}=5.0V, T_a=25°C.

SWITCHING CHARACTERISTICS (T_a=-20~75°C, unless otherwise noted)

Symbol	Parameter	Test pin	Test Conditions	Limits			Unit
				Min.	Typ.	Max.	
f _{opr}	Prescaler Operating frequency	17	V _{CC} =4.5~5.5V V _{IN} =V _{INmin} ~V _{INmax}	80		1000	MHz
V _{IN}	Operating input voltage	17	V _{CC} =4.5~5.5V 80~100MHz 100~1000MHz	-24 -27		4 4	dBm
t _{PWC}	Clock pulse width	4	V _{CC} =4.5~5.5V	1			μs
t _{SU (D)}	Data setup time	3		2			μs
t _{H (D)}	Data hold time	3		1			μs
t _{SU (E)}	Enable setup time	2		3			μs
t _{H (E)}	Enable hold time	2		3			μs
t _{INT}	Enable data interval time	2, 3		1			μs
t _r	Rising time	2, 3, 4				1	μs
t _f	Falling time	2, 3, 4				1	μs

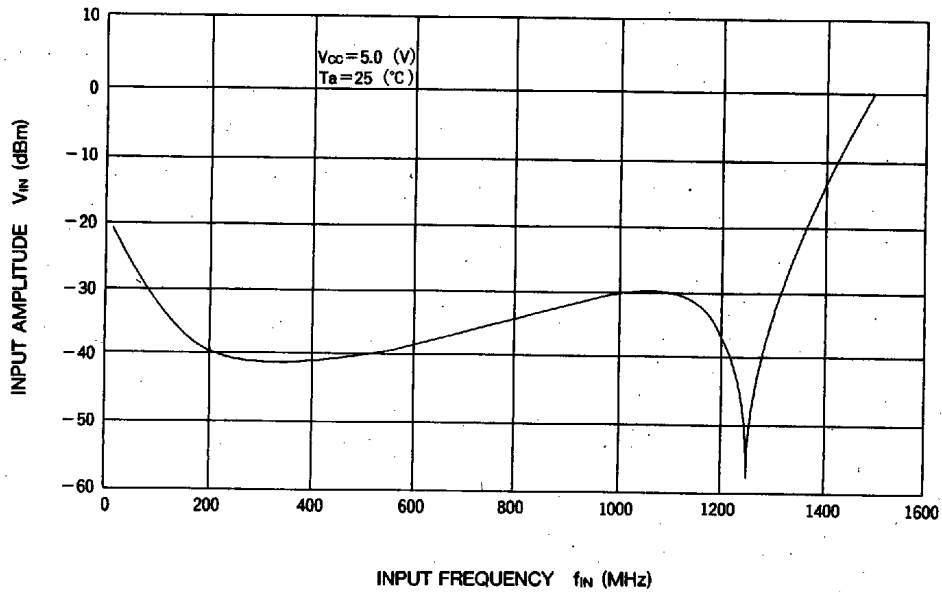
SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

TEST CIRCUIT



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY

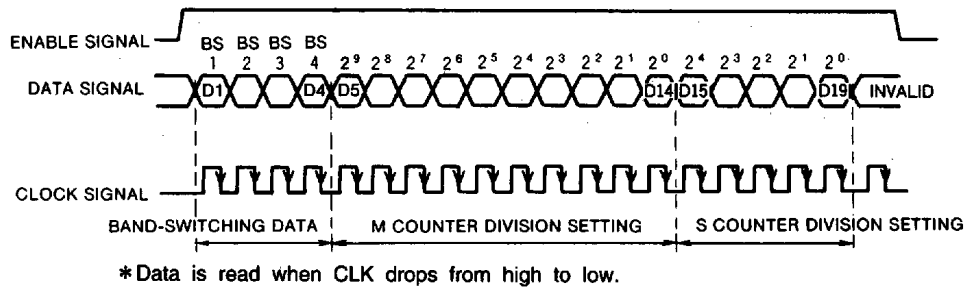


SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

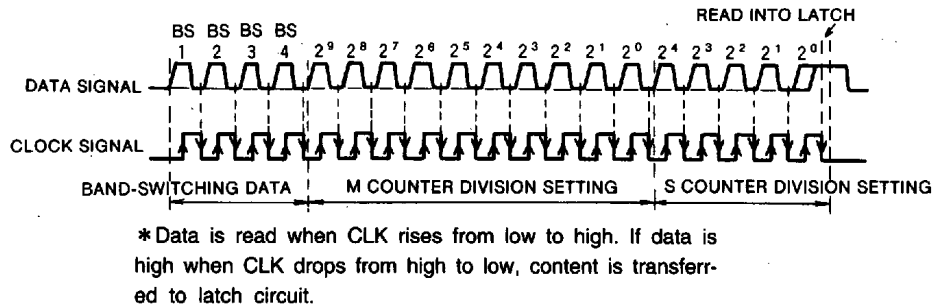
HOW TO SET THE DIVIDING RATIO OF THE PROGRAMMABLE DIVIDER AND BAND-SWITCHING OUTPUT

(1) When control method selection pin SW is set to Vcc or OPEN, the division ratio of the programmable divider and band-switching output are set as shown below.

When set high, the data and clock signals are read, and the data is read into the latch at the falling edge of the 19th clock signal pulse. The clock signal then becomes invalid.



(2) When the control method selection pin SW is set to GND, the division ratio of the programmable divider and band-switching output is as shown below.



Total division N is given by the following formulas, in addition to the prescaler used in the previous stage.

$$N=8(32M+S) \quad M: 10\text{-bit Main Counter Division}$$

$$S: 5\text{-bit Swallow Counter Division}$$

The M and S counters are binary and the possible division ranges are as follows.

$$32 \leq M \leq 1023$$

$$0 \leq S \leq 31$$

Therefore, division N range is 8,192~262,136.

The tuning frequency $f_{v.c.o.}$ is given by the following expressions.

$$f_{v.c.o.} = f_{REF} \times N$$

$$= 3.90625 \times 8 \cdot (32M+S)$$

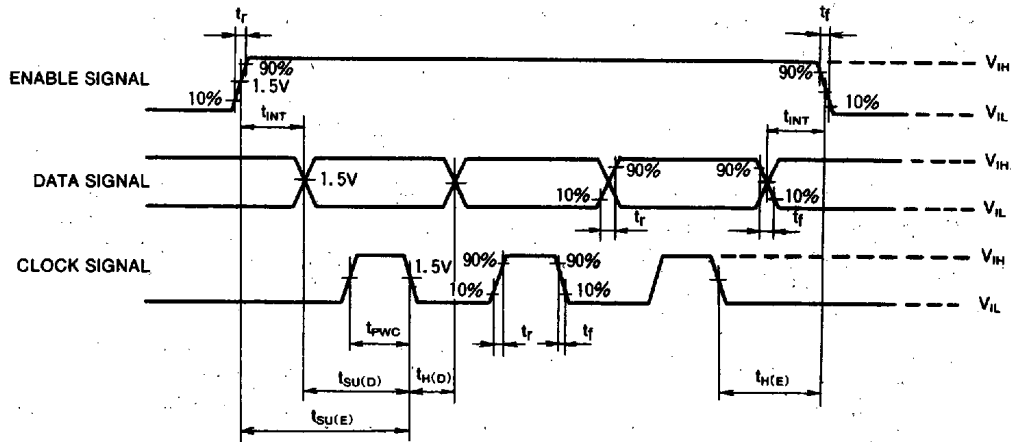
$$= 31.25(32M+S) [\text{kHz}]$$

Therefore, the tuning frequency range is 32MHz~1,023.96875MHz.

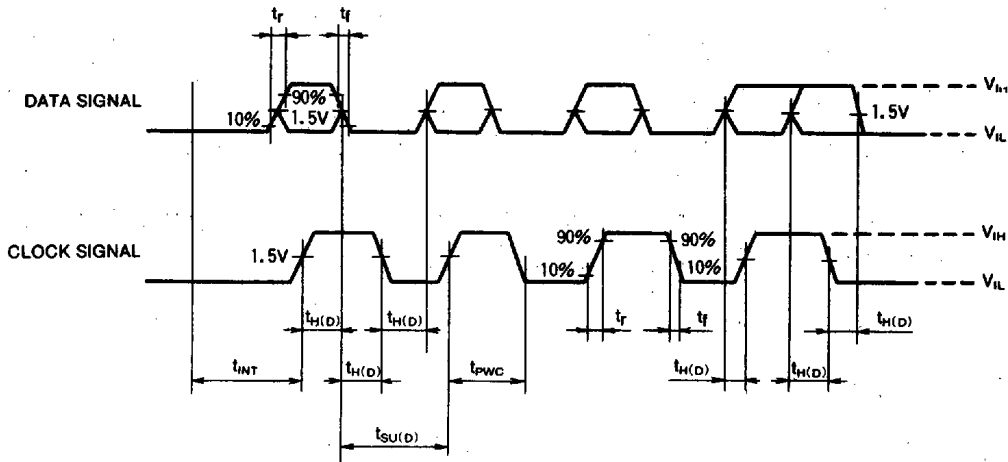
SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

TIMING DIAGRAM

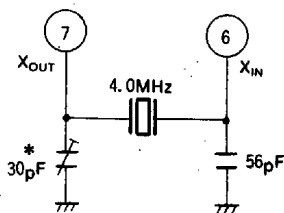
(1) When the control method selection pin SW is set to Vcc(V)



(2) When the control method selection pin SW is set to GND



CRYSTAL OSCILLATOR CONNECTION DIAGRAM



CRYSTAL OSCILLATOR CHARACTERISTICS

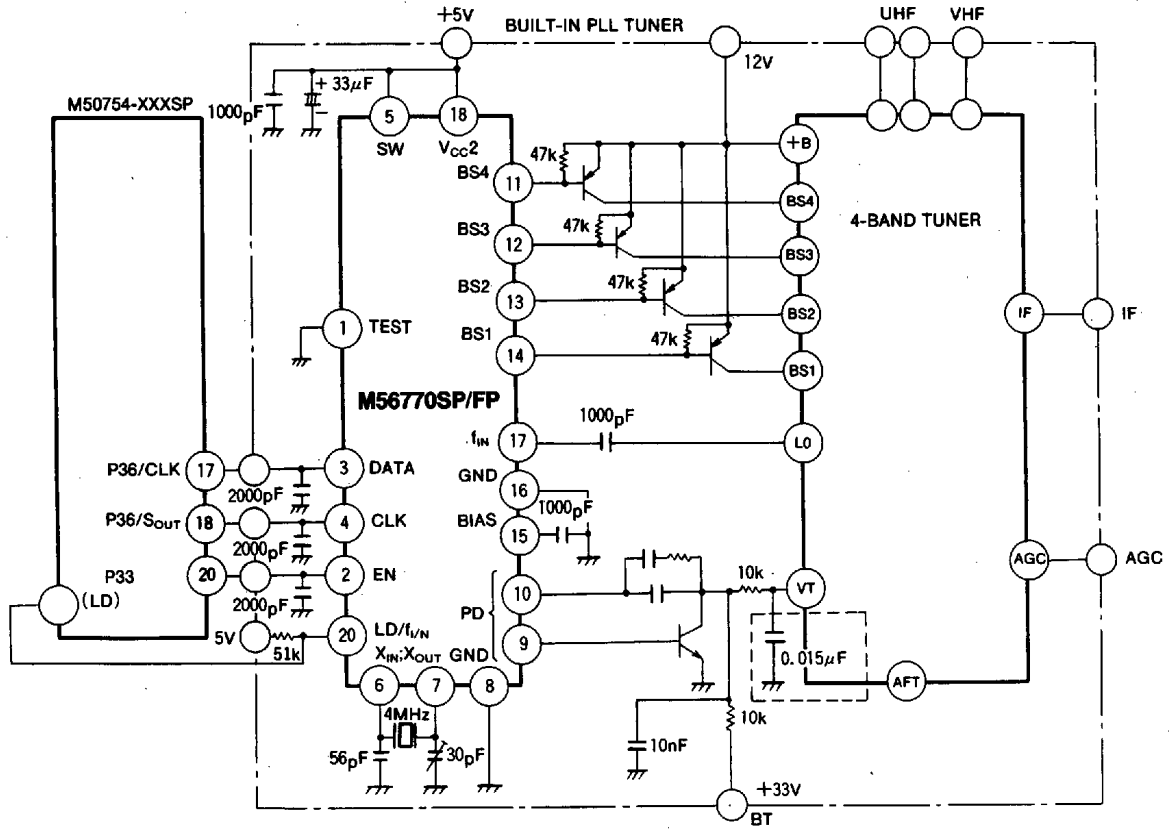
Actual resistance : less than 100Ω

Load capacitance : 20pF

* This trimmer is used to compensate for frequency variations of around ±20~30 ppm due to the crystal oscillator characteristics and oscillator circuit capacitance.

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

APPLICATION EXAMPLE



Unit Resistance : Ω
 Capacitance : F

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

DESCRIPTION OF PIN

No.	Pin	Name	Description of Function
①	TEST	Test input	Pin is used for testing, and is normally set low, in which case LD is selected and f_{REF} is set low. When set high, f_{REF} and $f_{1/N}$ outputs are selected and phase comparator output enters high impedance state.
②	EN	Enable input	Pin is normally set low. When set high, data and clock signals are read, and data is read into latch at falling edge of 19th clock signal pulse. Clock signal then becomes invalid.
③	DATA	Data input	Programmable divider division set input
④	CLK	Clock input	When SW pin is set to V_{CC} or OPEN, data is read into shift register when clock signal drops from high to low. When SW pin is set to GND, data is read into shift register when clock signal rises from low to high.
⑤	SW	Control method selection pin	When SW pin is set to V_{CC} or OPEN, division ratio of programmable divider is set for enable input, data input and clock input pins. When SW pin is set to GND, division ratio of programmable divider is set for data input and clock input pins only.
⑥ ⑦	X_{IN} X_{OUT}	Crystal oscillator connect pin	4.0MHz crystal oscillator is connected.
⑧	GND ₁	GND ₁	Connect to 0V.
⑨ ⑩	PD ₂ PD ₁	Phase comparator output 2 Phase comparator output 1	When programmable divider division output ($f_{1/N}$) is advanced with respect to reference frequency (f_{REF}), this output becomes high. When programmable divider division output is delayed, it becomes low. When the two are in sync, output enters high-impedance state.
⑪ ⑫ ⑬ ⑭	BS ₄ BS ₃ BS ₂ BS ₁	Band-switching output pin	Open-collector Band-switching output When band-switching data is high, output goes ON, when low, it goes OFF.
⑮	BIAS	Bias input	Prescaler bias pin. Capacitance of 1000pF is inserted between GND and this pin.
⑯	GND ₂	GND ₂	Connected to 0V.
⑰	f_{IN}	Prescaler input pin	Prescaler input pin, to which V. C. O. frequency is applied.
⑱	V_{CC}	Supply voltage	Supply voltage pin, $5.0 \pm 0.5V$ is applied.
⑲	f_{REF}	Reference frequency output	When TEST input is low, there is a constant low-level output. When high, reference frequency output (f_{REF}) is selected. Reference frequency is 3.90625kHz with open-collector output.
⑳	LD/ $f_{1/N}$	Lock detector/ division output	When TEST input is low, lock detector output (LD) is selected. When high, programmable divider division output ($f_{1/N}$) is selected. Open-collector output. When PLL is locked, lock detector output (LD) becomes low, when PLL is unlocked, it becomes high.