DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
μPA2610

P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μPA2610, which has a heat spreader, is P-channel MOS Field Effect Transistor designed for applications such as power switch of portable machine and so on.

FEATURES

- Thin surface mount package with heat spreader
- 1.8 V drive available
- Low on-state resistance

  $R_{DS(on)1}$ = 69 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2.5 A)

  $R_{DS(on)2}$ = 88 mΩ MAX. (V_{GS} = –2.5 V, I_D = –2.5 A)

  $R_{DS(on)3}$ = 142 mΩ MAX. (V_{GS} = –1.8 V, I_D = –1.5 A)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2610T1C	8LD3x2MLPM

Marking: Axxx (xxx: Traceability code)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–20.0	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓8.0	V
Drain Current (DC) Note1	$I_{D(DC)}$	∓5.0	A
Drain Current (pulse) Note2	$I_{D(pulse)}$	∓20.0	A
Total Power Dissipation Note3	P_{T1}	0.2	W
Total Power Dissipation Note1	P_{T2}	1.9	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. Mounted on FR-4 board of 645 mm^2 x 1.6 mm, PW ≤ 10 sec

2. PW ≤ 10 μs, Duty Cycle ≤ 1%

3. Without board

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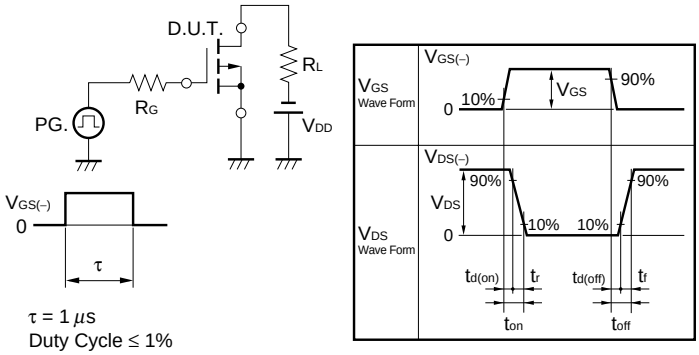
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –20.0 V, V_{GS} = 0 V			–10.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓8.0 V, V_{DS} = 0 V			∓10.0	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10.0 V, I_D = –1.0 mA	–0.45		–1.50	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = –10.0 V, I_D = –2.5 A	4			S
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = –4.5 V, I_D = –2.5 A		55	69	mΩ
	$R_{DS(on)2}$	V_{GS} = –2.5 V, I_D = –2.5 A		66	88	mΩ
	$R_{DS(on)3}$	V_{GS} = –1.8 V, I_D = –1.5 A		85	142	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10.0 V		600		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		120		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		75		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –10.0 V, I_D = –2.5 A		45		ns
Rise Time	t_r	V_{GS} = –4.0 V		200		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		435		ns
Fall Time	t_f			345		ns
Total Gate Charge	Q_G	V_{DD} = –16.0 V		5.5		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –4.0 V		1.2		nC
Gate to Drain Charge	Q_{GD}	I_D = –5.0 A		2.1		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 5.0 A, V_{GS} = 0 V		0.9		V

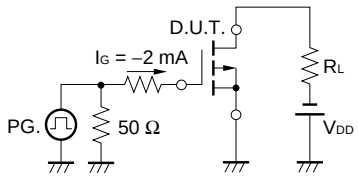
Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

TEST CIRCUIT 1 SWITCHING TIME



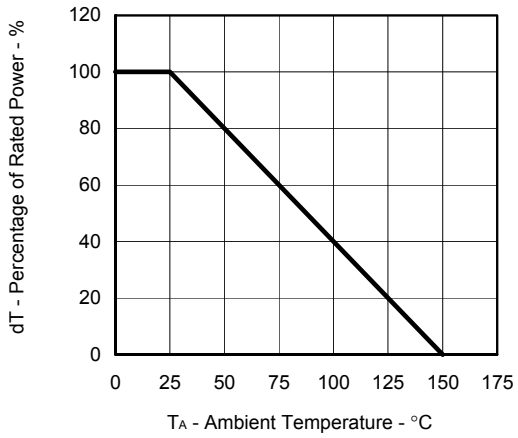
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

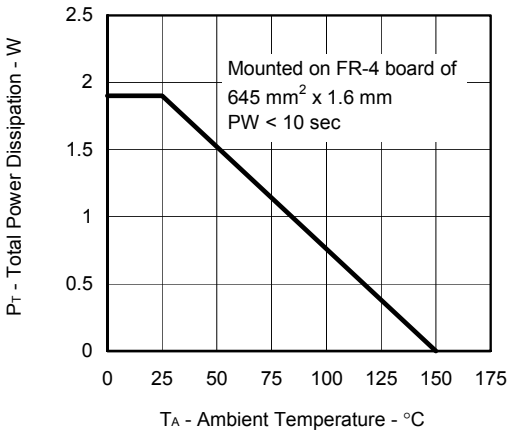


TYPICAL CHARACTERISTICS (T_A = 25°C)

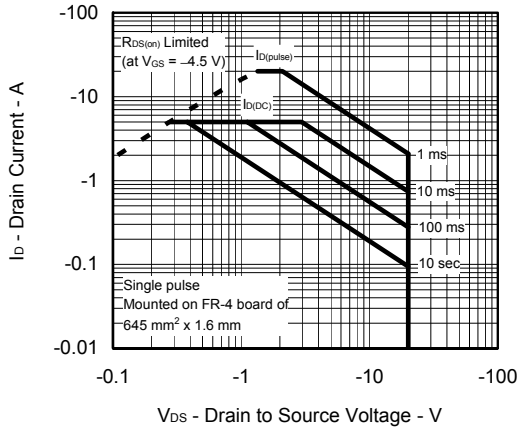
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



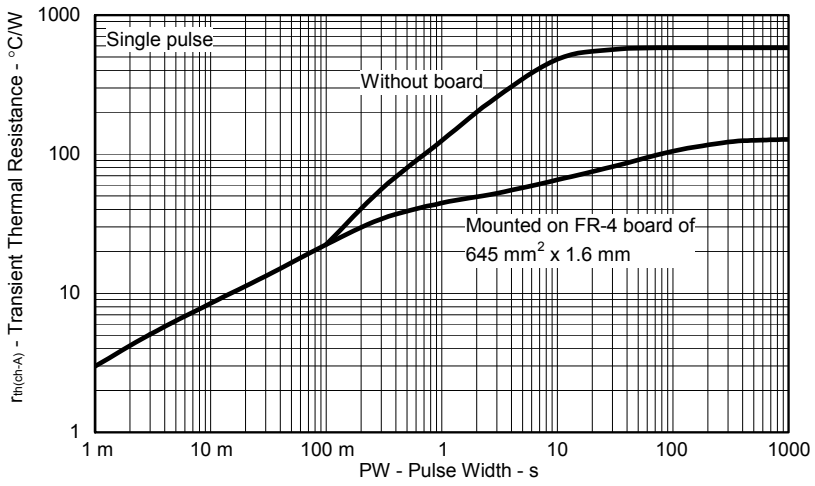
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



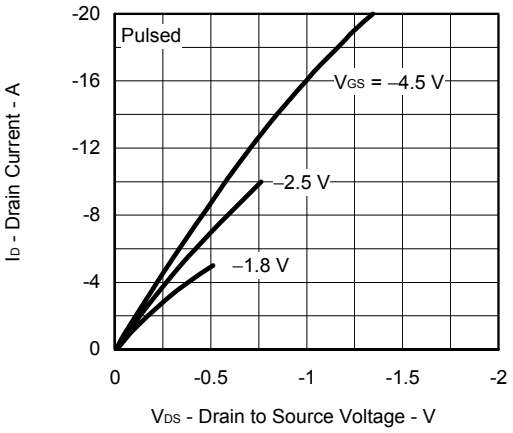
FORWARD BIAS SAFE OPERATING AREA



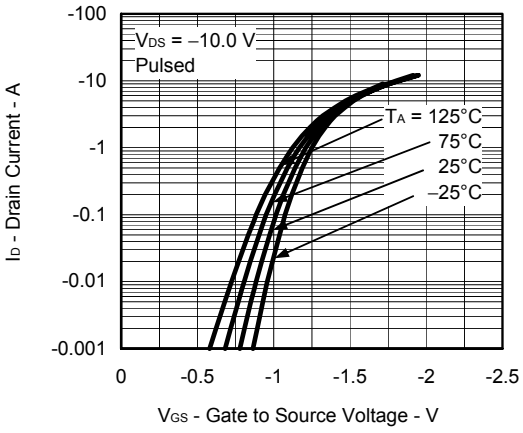
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



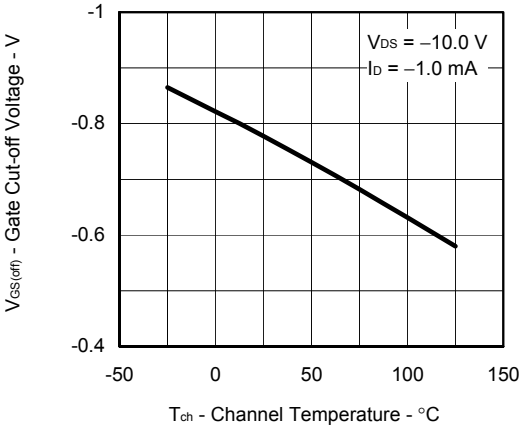
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



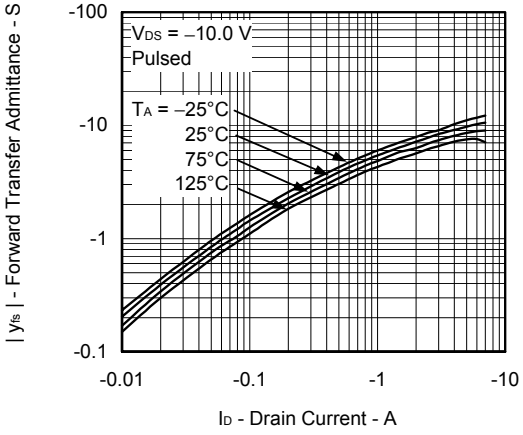
FORWARD TRANSFER CHARACTERISTICS



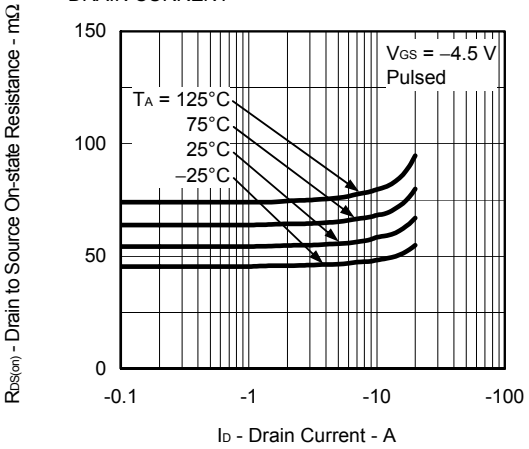
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



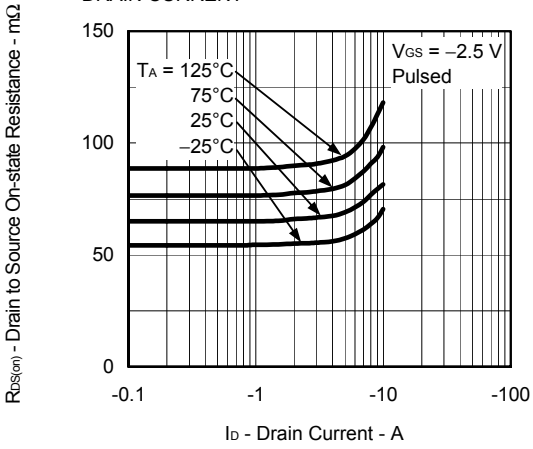
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



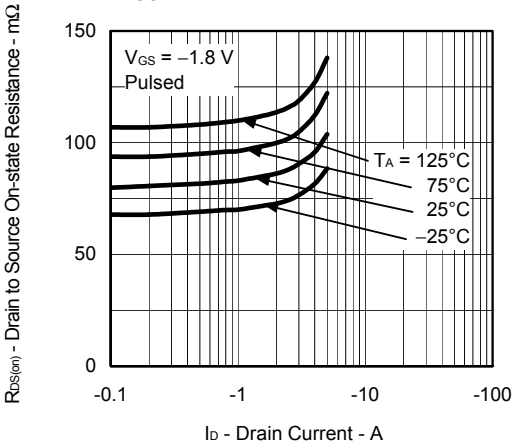
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



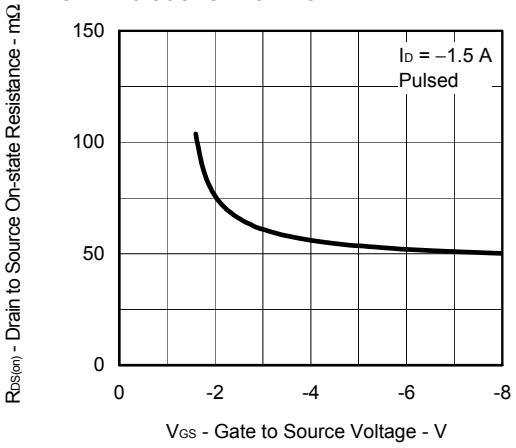
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



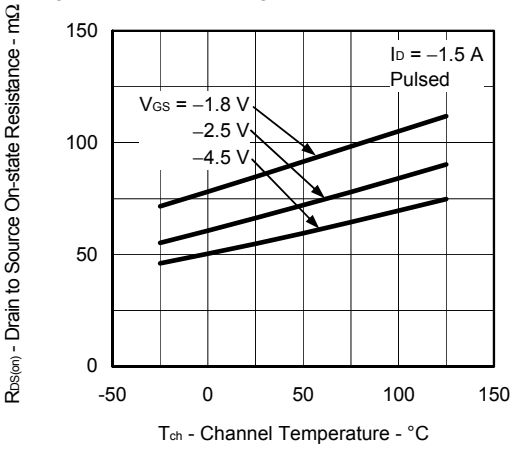
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



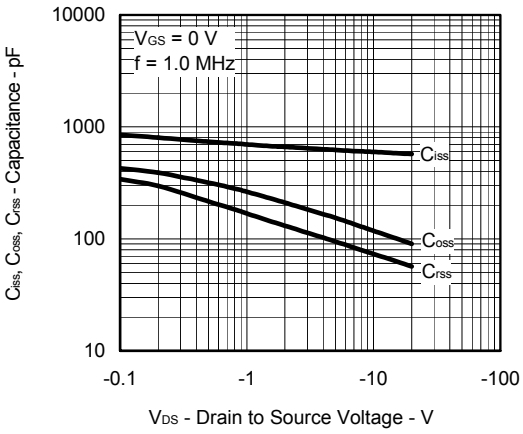
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



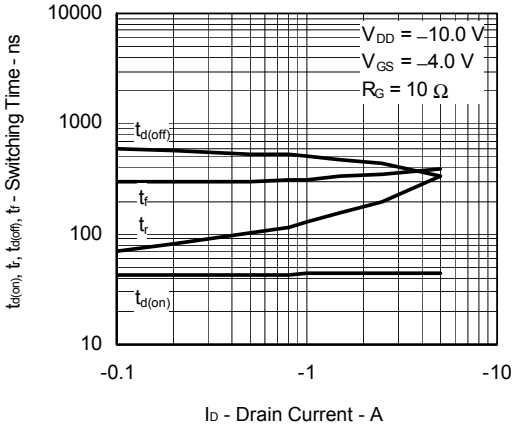
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



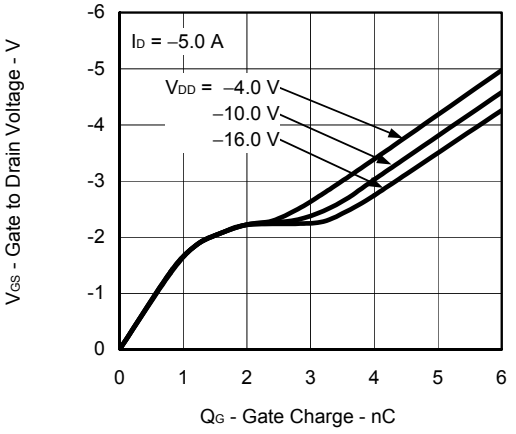
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



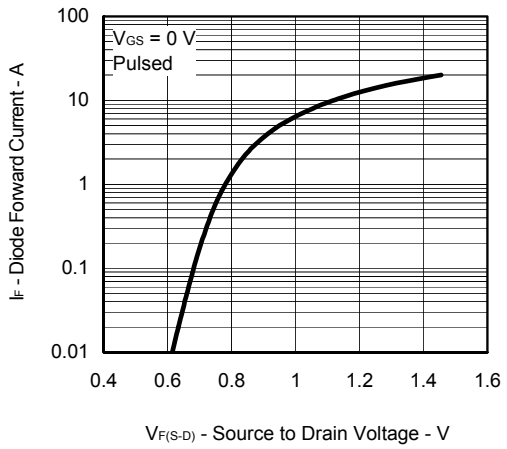
SWITCHING CHARACTERISTICS



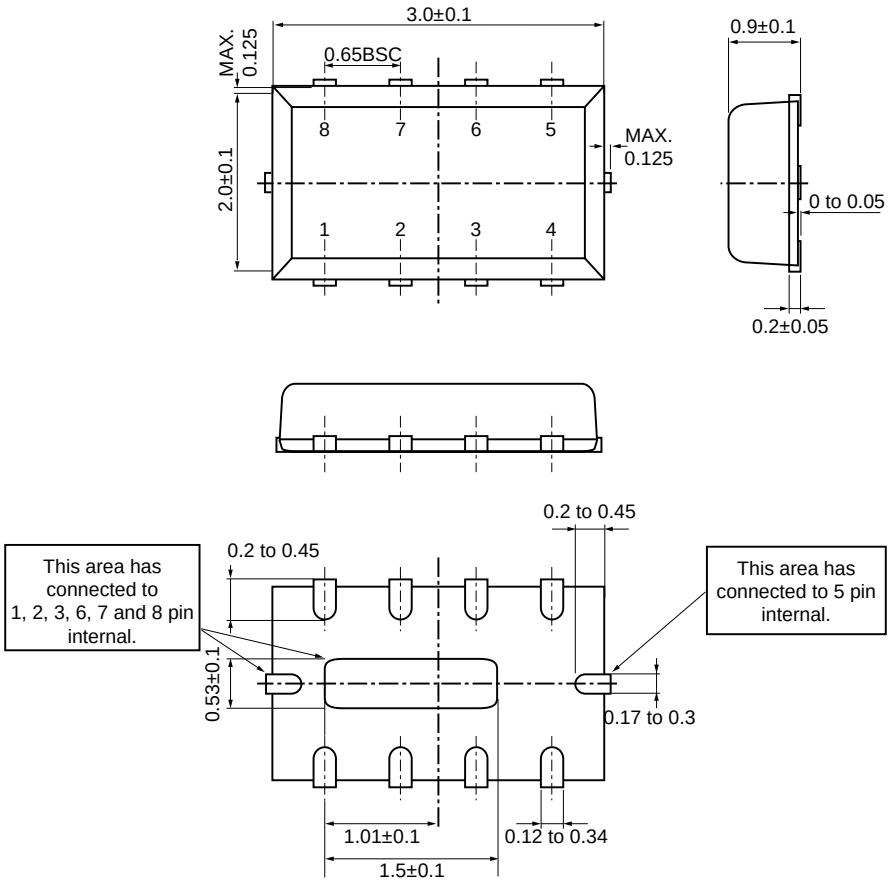
DYNAMIC INPUT CHARACTERISTICS



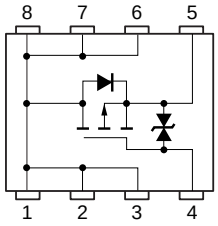
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



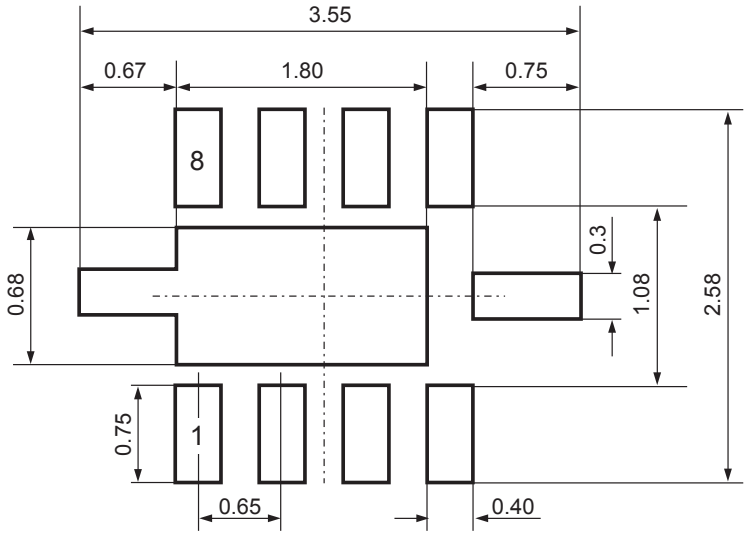
1, 2, 3, 6, 7, 8: Drain
4 : Gate
5 : Source
MARKING SIDE VIEW

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

EXAMPLE OF THE LAND PATTERN

Please optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.

(Unit: mm)



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