# DATA SHEET



## DUAL N-CHANNEL MOSFET FOR SWITCHING

#### DESCRIPTION

NEC

The  $\mu$ PA2353 is a Dual N-channel MOSFET designed for Lithium-Ion battery protection circuit.

Ecologically Flip chip MOSFET for Lithium-Ion battery Protection (EFLIP).

#### **FEATURES**

- Monolithic Dual MOSFET Connecting the Drains on the circuit board is not required because the Drains of the FET1 and the FET2 are internally connected.
- 1.8 V drive available and low on-state resistance  $R_{SS(on)1} = 31 \text{ m}\Omega \text{ MAX}. (V_{GS} = 4.5 \text{ V}, \text{ Is} = 3.0 \text{ A})$   $R_{SS(on)2} = 38 \text{ m}\Omega \text{ MAX}. (V_{GS} = 3.1 \text{ V}, \text{ Is} = 3.0 \text{ A})$   $R_{SS(on)3} = 43 \text{ m}\Omega \text{ MAX}. (V_{GS} = 2.5 \text{ V}, \text{ Is} = 3.0 \text{ A})$  $R_{SS(on)4} = 79 \text{ m}\Omega \text{ MAX}. (V_{GS} = 1.8 \text{ V}, \text{ Is} = 3.0 \text{ A})$
- Built-in G-S protection diode against ESD
- Pb-free Bump

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE
μΡΑ2353Τ1G-E4-Α <sup>Note</sup>	4-pin EFLIP

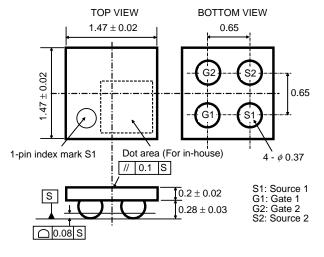
Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

Remark "-E4" indicates the unit orientation (E4 only).

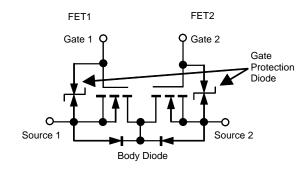
#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^{\circ}C$ )

Source to Source Voltage (VGS = 0 V)	Vsss	20	V
Gate to Source Voltage (Vss = 0 V)	Vgss	±8	V
Source Current (DC) Note1	IS(DC)	±6.0	Α
Source Current (pulse) Note2	S(pulse)	±50	Α
Total Power Dissipation Note1	Р⊤	1.3	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C

**Notes 1.** Mounted on ceramic board of 50 cm<sup>2</sup> x 1.0 mmt **2.** PW  $\leq$  100  $\mu$ s, Single Pulse



**OUTLINE DRAWING (Unit: mm)** 



EQUIVALENT CIRCUIT

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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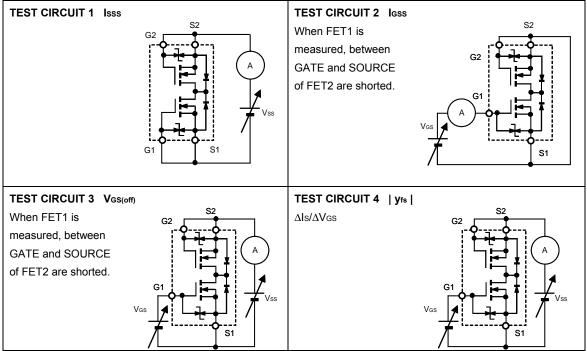
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Source Current	Isss	Vss = 20 V, Vgs = 0 V, TEST CIRCUIT 1			1	μA
Gate Leakage Current	Igss	$V_{GS} = \pm 8 \text{ V},  V_{SS} = 0  \text{V},  \text{TEST CIRCUIT 2}$			±10	μA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	Vss = 10 V, Is = 1.0 mA, TEST CIRCUIT 3	0.4	0.7	1.2	V
Forward Transfer Admittance Note	y <sub>fs</sub>	Vss = 10 V, Is = 3.0 A, TEST CIRCUIT 4	3.0			S
Source to Source On-state	RSS(on)1	V <sub>GS</sub> = 4.5 V, Is = 3.0 A, TEST CIRCUIT 5	19	29	31	mΩ
Resistance Note	RSS(on)2	V <sub>GS</sub> = 3.1 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 5	20	31	38	mΩ
	RSS(on)3	V <sub>GS</sub> = 2.5 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 5	22.5	34	43	mΩ
	RSS(on)4	V <sub>GS</sub> = 1.8 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 5	25	44	79	mΩ
Input Capacitance	Ciss	Vss = 10 V, Vgs = 0 V, f = 1.0 MHz		950		pF
Output Capacitance	Coss	TEST CIRCUIT 7		170		pF
Reverse Transfer Capacitance	Crss			100		pF
Turn-on Delay Time	td(on)	V <sub>DD</sub> = 20 V, Is = 6.0 A,		2.4		μs
Rise Time	tr	$V_{GS}$ = 4.0 V, $R_{G}$ = 6.0 $\Omega$ ,		5.9		μs
Turn-off Delay Time	td(off)	TEST CIRCUIT 8		9.8		μs
Fall Time	tr			12.3		μs
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 16 V, V <sub>G1S1</sub> = 4.0 V, I <sub>S</sub> = 6.0 A, TEST CIRCUIT 9		8.0		nC
Body Diode Forward Voltage Note	VF(S-S)	I⊧ = 6.0 A, V <sub>GS</sub> = 0 V, TEST CIRCUIT 6		0.9		V

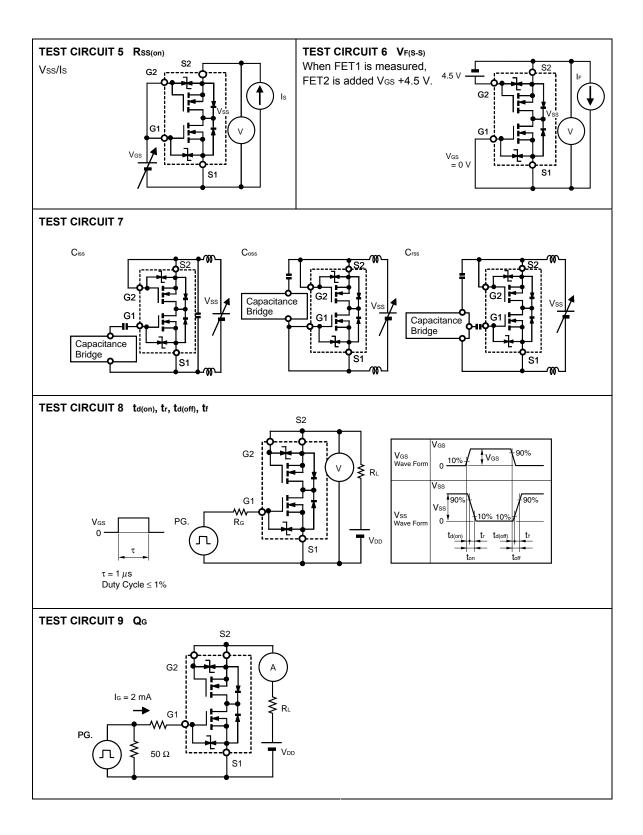
### **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$ ) These are common to FET1 and FET2.

Note Pulsed

#### Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

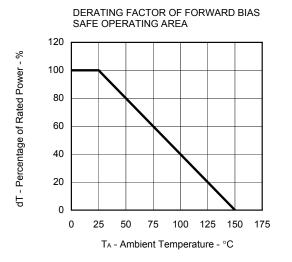


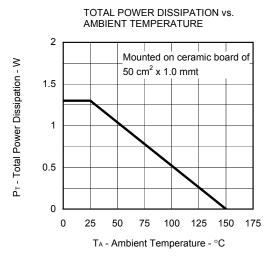
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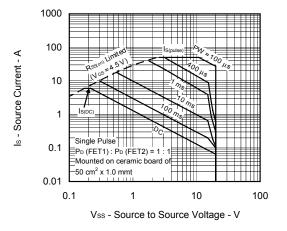
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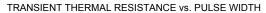
#### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

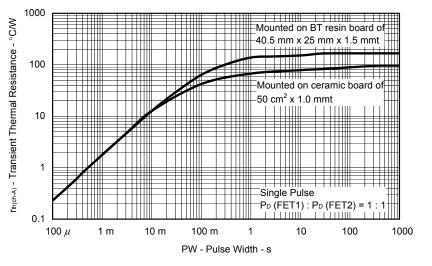






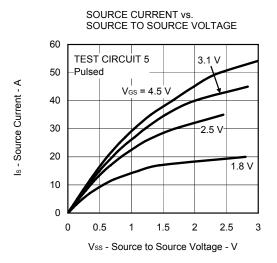




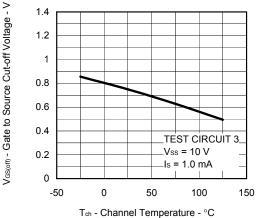


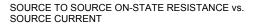
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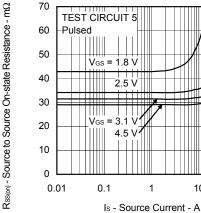
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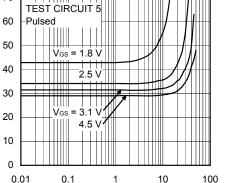




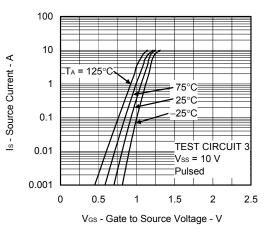




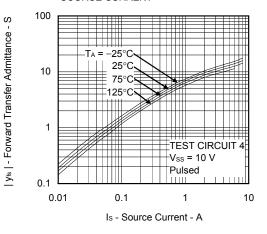




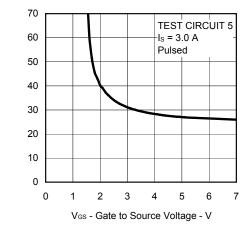
FORWARD TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE vs. SOURCE CURRENT

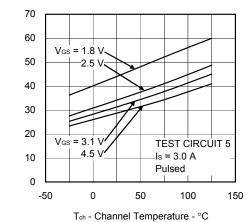


SOURCE TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



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 $Rss_{(m)}$  - Source to Source On-state Resistance -  $m\Omega$ 

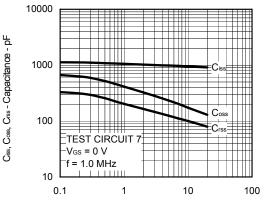


SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

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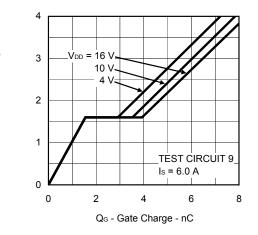
 $Rss_{(on)}$  - Source to Source On-state Resistance - m $\Omega$ 

CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE

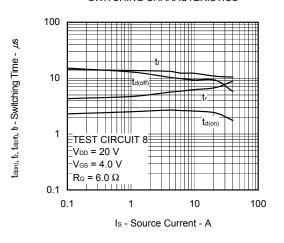


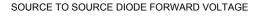
Vss - Source to Source Voltage - V

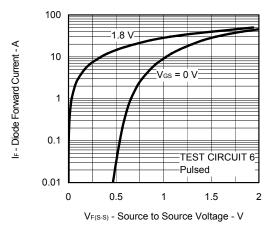




SWITCHING CHARACTERISTICS







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V<sub>GS</sub> - Gate to Source Voltage - V

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