DATA SHEET

NEC

# MOS FIELD EFFECT TRANSISTOR
# μPA2350B

## DUAL N-CHANNEL MOSFET FOR SWITCHING

### DESCRIPTION

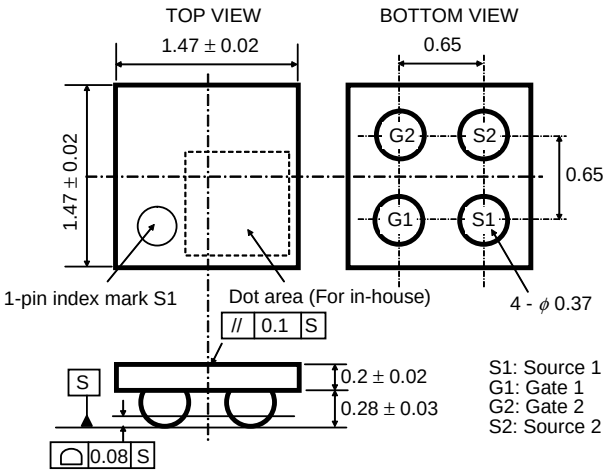
The μPA2350B is a Dual N-channel MOSFET designed for Lithium-Ion battery protection circuit.

Ecologically Flip chip MOSFET for Lithium-Ion battery Protection (EFLIP).

### FEATURES

- Monolithic Dual MOSFET
  Connecting the Drains on the circuit board is not required because the Drains of the FET1 and the FET2 are internally connected.
- 2.5 V drive available and low on-state resistance
  $R_{SS(on)1}$ = 35 mΩ MAX. ($V_{GS}$ = 4.5 V, $I_S$ = 3.0 A)
  $R_{SS(on)2}$ = 37 mΩ MAX. ($V_{GS}$ = 4.0 V, $I_S$ = 3.0 A)
  $R_{SS(on)3}$ = 44 mΩ MAX. ($V_{GS}$ = 3.1 V, $I_S$ = 3.0 A)
  $R_{SS(on)4}$ = 55 mΩ MAX. ($V_{GS}$ = 2.5 V, $I_S$ = 3.0 A)
- Built-in G-S protection diode against ESD
- Pb-free Bump

### OUTLINE DRAWING (Unit: mm)



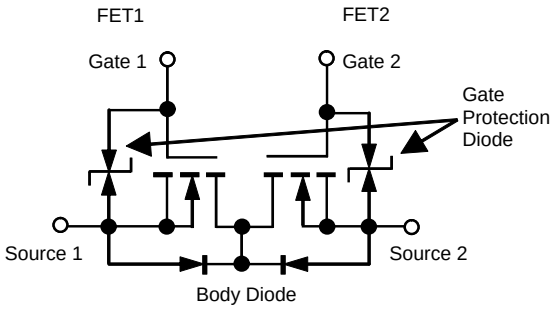

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| μPA2350BT1G-E4-A [Note] | 4-pin EFLIP |

**Note** Pb-free (This product does not contain Pb in the external electrode and other parts.)

**Remark** "-E4" indicates the unit orientation (E4 only).

### EQUIVALENT CIRCUIT




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | |
|---|---|---|---|
| Source to Source Voltage ($V_{GS}$ = 0 V) | $V_{SSS}$ | 20 | V |
| Gate to Source Voltage ($V_{SS}$ = 0 V) | $V_{GSS}$ | ±12 | V |
| Source Current (DC) [Note1] | $I_{S(DC)}$ | 6.0 | A |
| Source Current (pulse) [Note2] | $I_{S(pulse)}$ | ±50 | A |
| Total Power Dissipation [Note1] | $P_T$ | 1.3 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +150 | °C |

**Notes 1.** Mounted on ceramic board of 50 cm² x 1.0 mmt
**2.** PW ≤ 100 μs, Single Pulse

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



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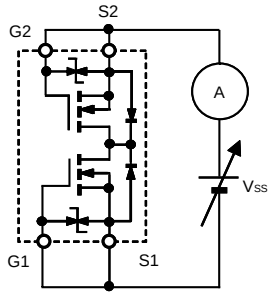
**ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C) These are common to FET1 and FET2.**

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Source Current | $I_{SSS}$ | $V_{SS}$ = 20 V, $V_{GS}$ = 0 V, TEST CIRCUIT 1 | | | 1 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±12 V, $V_{SS}$ = 0 V, TEST CIRCUIT 2 | | | ±10 | μA |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | $V_{SS}$ = 10 V, $I_S$ = 1.0 mA, TEST CIRCUIT 3 | 0.5 | 1.0 | 1.5 | V |
| Forward Transfer Admittance Note | $\|y_{fs}\|$ | $V_{SS}$ = 10 V, $I_S$ = 3.0 A, TEST CIRCUIT 4 | 2.5 | | | S |
| Source to Source On-state Resistance Note | $R_{SS(on)1}$ | $V_{GS}$ = 4.5 V, $I_S$ = 3.0 A, TEST CIRCUIT 5 | 22 | 27 | 35 | mΩ |
| | $R_{SS(on)2}$ | $V_{GS}$ = 4.0 V, $I_S$ = 3.0 A, TEST CIRCUIT 5 | 23 | 28 | 37 | mΩ |
| | $R_{SS(on)3}$ | $V_{GS}$ = 3.1 V, $I_S$ = 3.0 A, TEST CIRCUIT 5 | 24 | 32 | 44 | mΩ |
| | $R_{SS(on)4}$ | $V_{GS}$ = 2.5 V, $I_S$ = 3.0 A, TEST CIRCUIT 5 | 30 | 40 | 55 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{SS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 780 | | pF |
| Output Capacitance | $C_{oss}$ | TEST CIRCUIT 7 | | 140 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 80 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $I_S$ = 6.0 A, | | 3.1 | | μs |
| Rise Time | $t_r$ | $V_{GS}$ = 4.0 V, $R_G$ = 6.0 Ω, | | 6.6 | | μs |
| Turn-off Delay Time | $t_{d(off)}$ | TEST CIRCUIT 8 | | 5.0 | | μs |
| Fall Time | $t_f$ | | | 9.2 | | μs |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 16 V, $V_{GS1}$ = 4.0 V, $I_S$ = 6.0 A, TEST CIRCUIT 9 | | 6.2 | | nC |
| Body Diode Forward Voltage Note | $V_{F(S-S)}$ | $I_F$ = 6.0 A, $V_{GS}$ = 0 V, TEST CIRCUIT 6 | | 1.0 | | V |

**Note** Pulsed

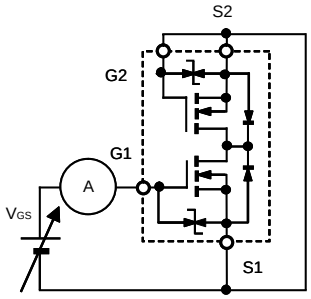
Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

**TEST CIRCUIT 1 $I_{SSS}$**



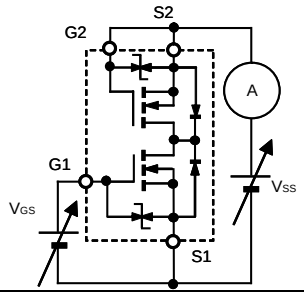

**TEST CIRCUIT 2 $I_{GSS}$**

When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



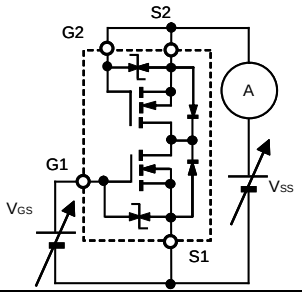

**TEST CIRCUIT 3 $V_{GS(off)}$**

When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



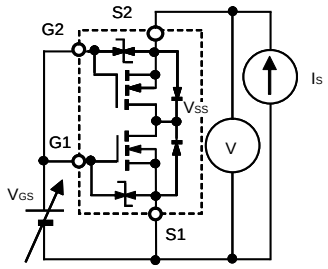

**TEST CIRCUIT 4 $|y_{fs}|$**

ΔIs/ΔVGS



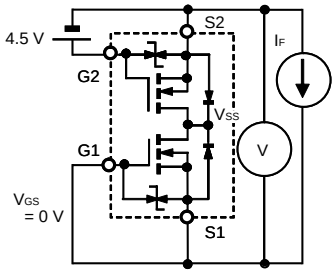
**TEST CIRCUIT 5 $R_{SS(on)}$**

$V_{SS}/I_S$

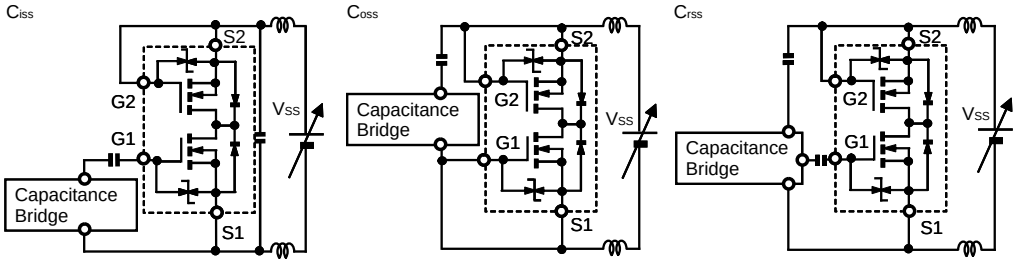



**TEST CIRCUIT 6 $V_{F(S-S)}$**

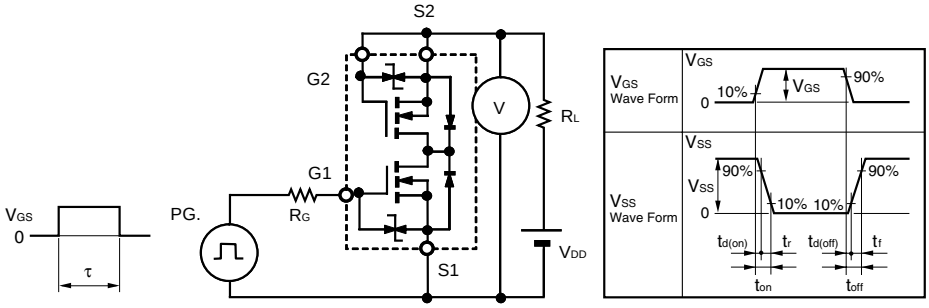
When FET1 is measured, FET2 is added $V_{GS}$ +4.5 V.



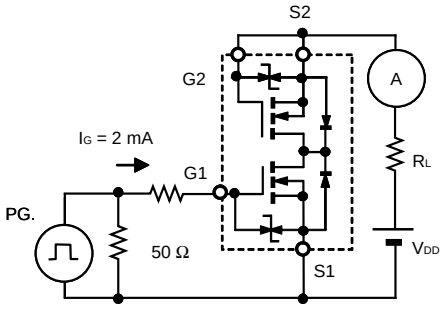

**TEST CIRCUIT 7**




**TEST CIRCUIT 8 $t_{d(on)}$, $t_r$, $t_{d(off)}$, $t_f$**

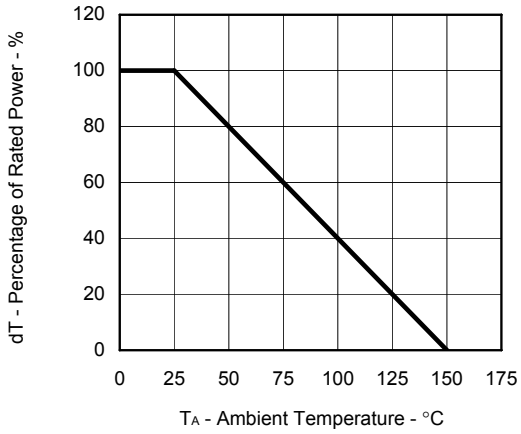



**TEST CIRCUIT 9 $Q_G$**

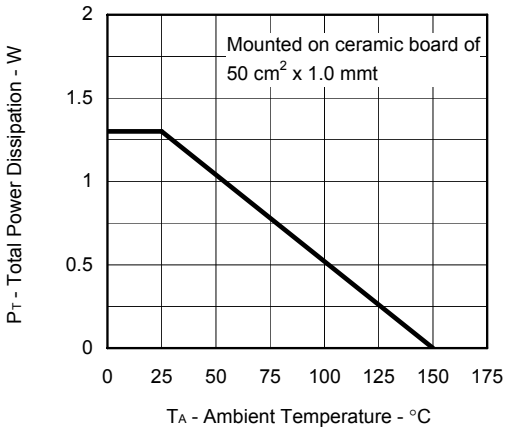


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

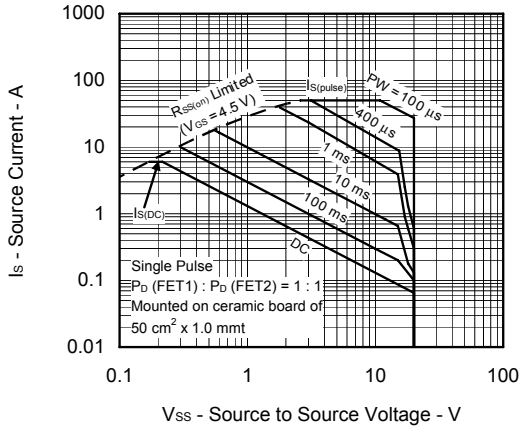
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



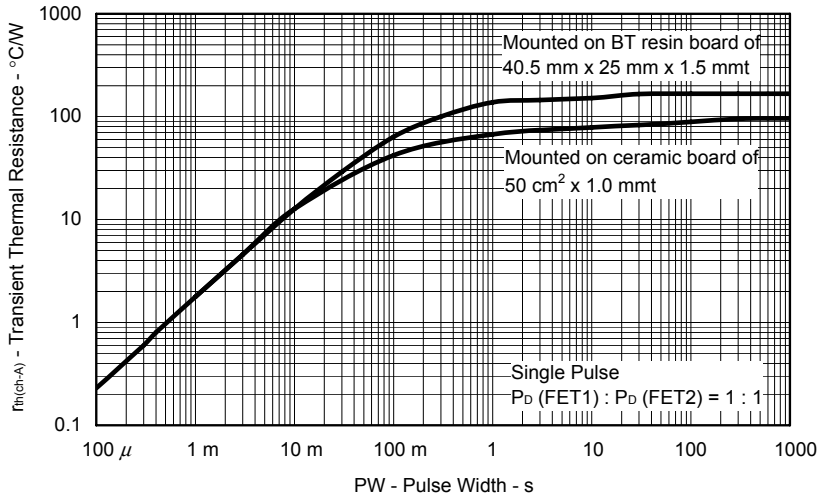

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



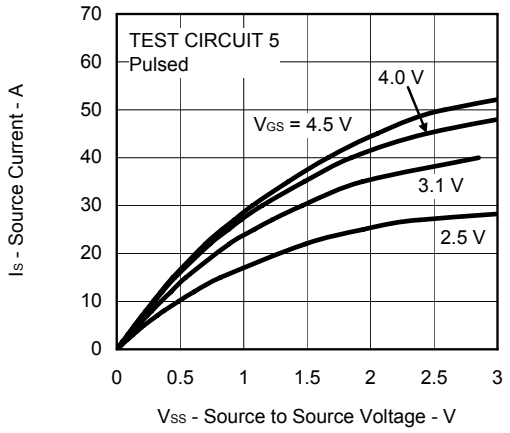

FORWARD BIAS SAFE OPERATING AREA



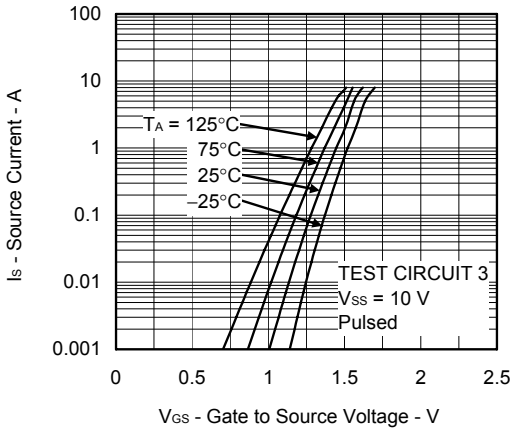

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



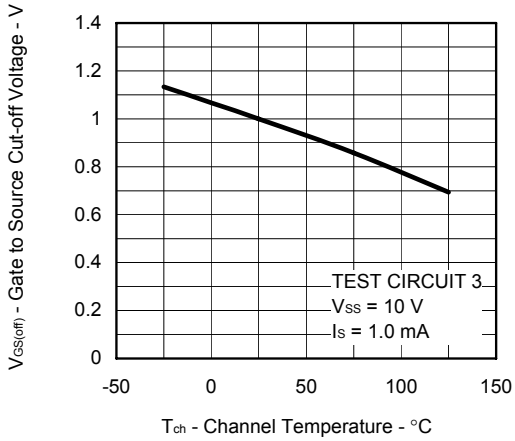
SOURCE CURRENT vs.
SOURCE TO SOURCE VOLTAGE



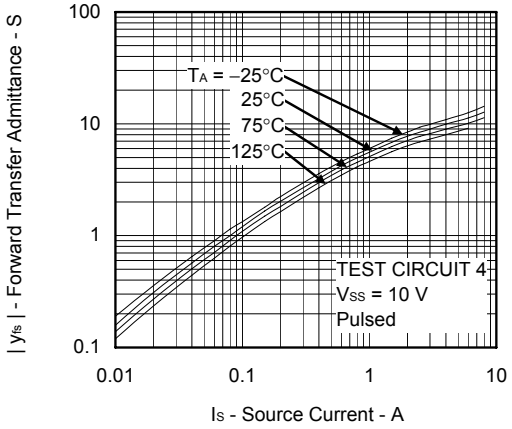

FORWARD TRANSFER CHARACTERISTICS



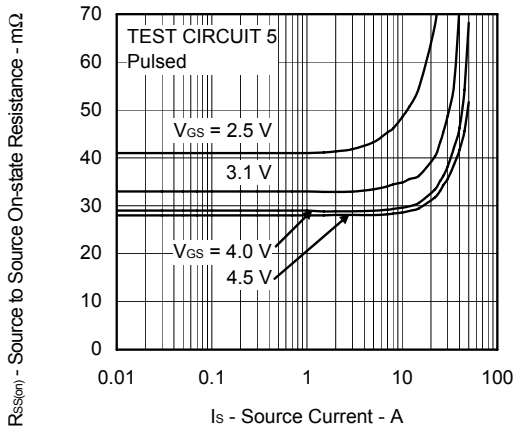

GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



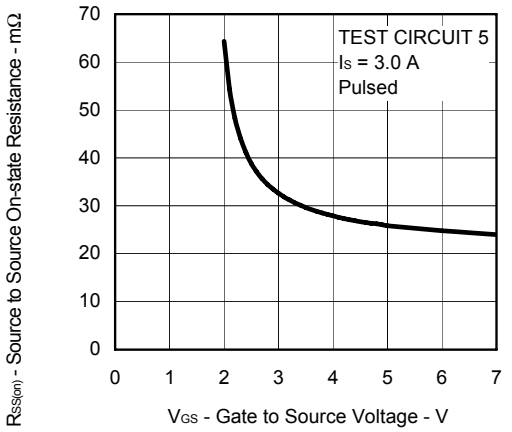

FORWARD TRANSFER ADMITTANCE vs.
SOURCE CURRENT



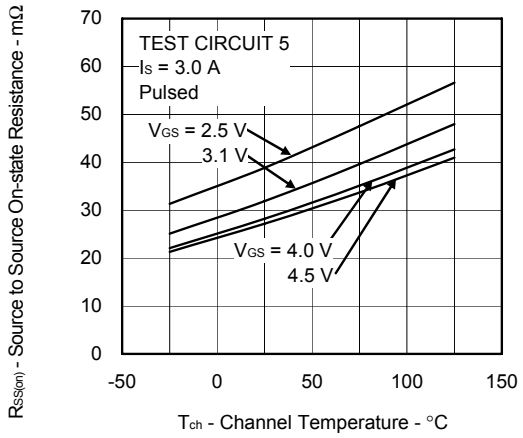

SOURCE TO SOURCE ON-STATE RESISTANCE vs.
SOURCE CURRENT



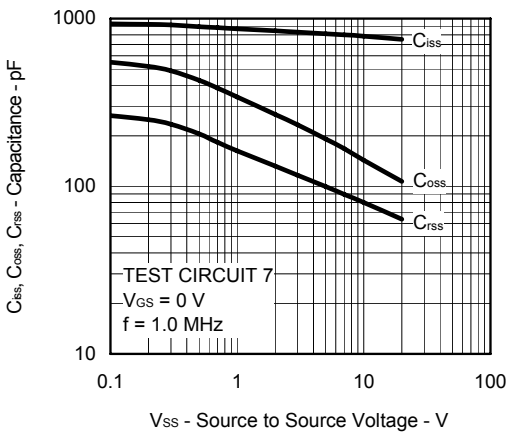

SOURCE TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



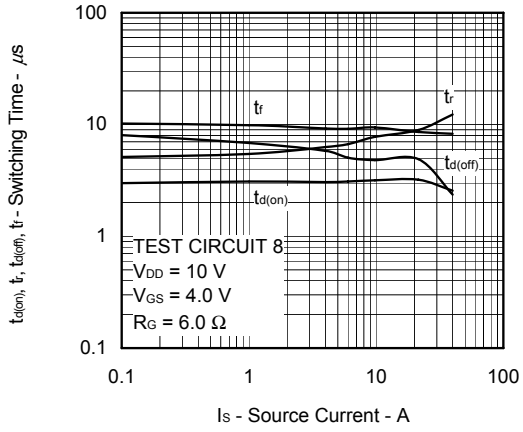
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



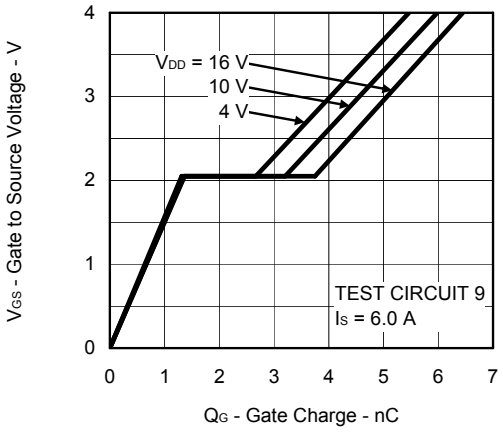

CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



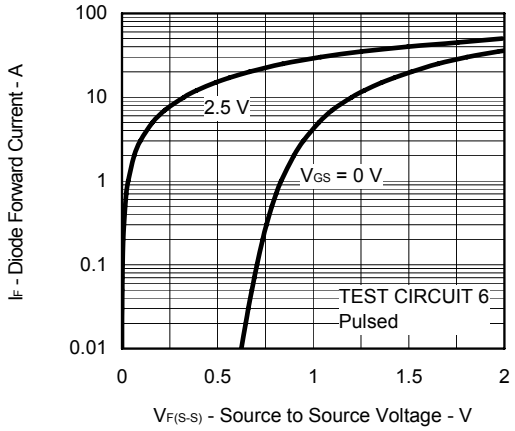

SWITCHING CHARACTERISTICS




DYNAMIC INPUT CHARACTERISTICS




SOURCE TO SOURCE DIODE FORWARD VOLTAGE



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