DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
μPA2510

P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μPA2510, which has a heat spreader, is P-channel MOS Field Effect Transistor designed for power management applications of notebook computers.

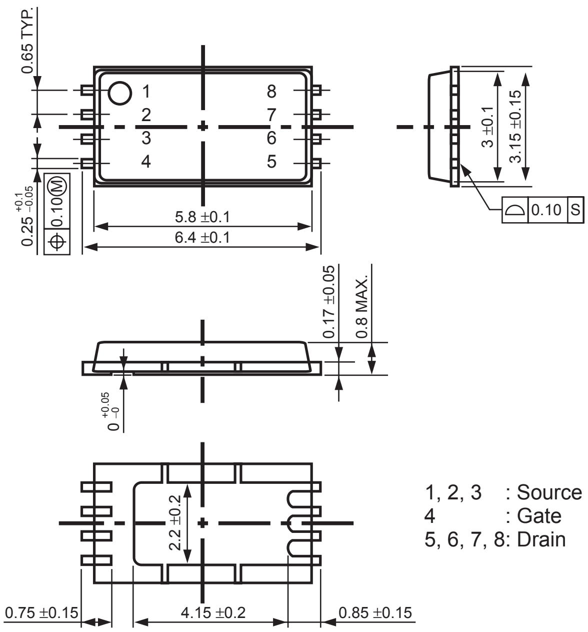
FEATURES

- μPA2510 has a thin surface mount package with a heat spreader. The land size is same as 8-pin TSSOP.
- Low on-state resistance
  $R_{DS(on)1}$ = 10.1 mΩ MAX. (V_{GS} = –10.0 V, I_D = –9.0 A)
  $R_{DS(on)2}$ = 14.0 mΩ MAX. (V_{GS} = –4.5 V, I_D = –9.0 A)
- Low C_{iss}: 3000 pF TYP. (V_{DS} = –10.0 V, V_{GS} = 0 V)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2510TM	8PIN HWSON

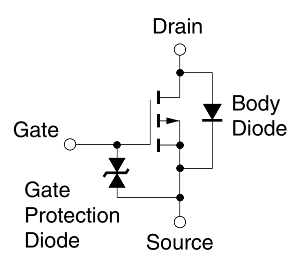
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30.0	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20.0	V
Drain Current (DC) Note1	$I_{D(DC)}$	∓18.0	A
Drain Current (pulse) Note2	$I_{D(pulse)}$	∓72.0	A
Total Power Dissipation Note1	P_T	2.7	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note3	I_{AS}	–18.0	A
Single Avalanche Energy Note3	E_{AS}	32.4	mJ

EQUIVALENT CIRCUIT



Notes 1. Mounted on FR-4 board of 25 cm^2 x 1.6 mm, PW ≤ 10 sec
2. PW ≤ 10 μs, Duty Cycle ≤ 1%
3. Starting T_{ch} = 25°C, V_{DD} = –30 V, R_G = 25 Ω, V_{GS} = –20.0 → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

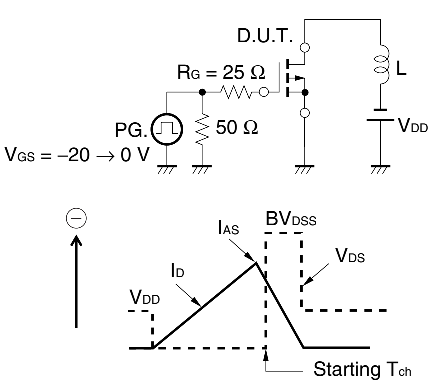
Document No. G16683EJ1V0DS00 (1st edition)
Date Published December 2003 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

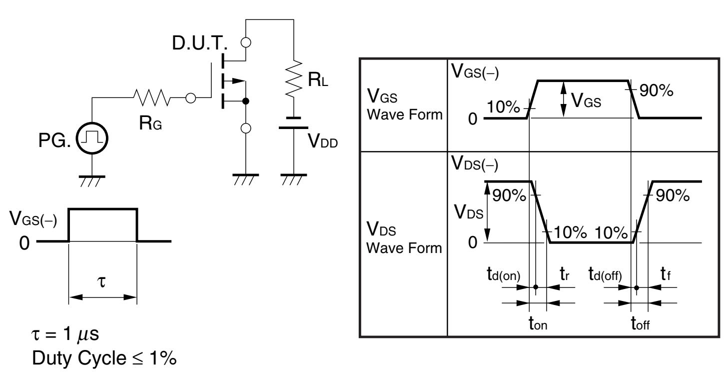
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30.0 V, V_{GS} = 0 V			–1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20.0 V, V_{DS} = 0 V			∓10.0	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10.0 V, I_D = –1.0 mA	–1.0		–2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = –10.0 V, I_D = –9.0 A	12			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10.0 V, I_D = –9.0 A		7.5	10.1	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –9.0 A		9.5	14.0	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10.0 V		3000		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		940		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		500		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15.0 V, I_D = –9.0 A		12		ns
Rise Time	t_r	V_{GS} = –10.0 V		18		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		270		ns
Fall Time	t_f			170		ns
Total Gate Charge	Q_G	V_{DD} = –24.0 V		70		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10.0 V		8		nC
Gate to Drain Charge	Q_{GD}	I_D = –18.0 A		22		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 18.0 A, V_{GS} = 0 V		0.85		V
Reverse Recovery Time	t_{rr}	I_F = 18.0 A, V_{GS} = 0 V		80		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		68		nC

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

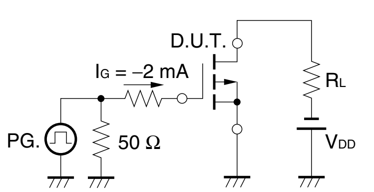
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

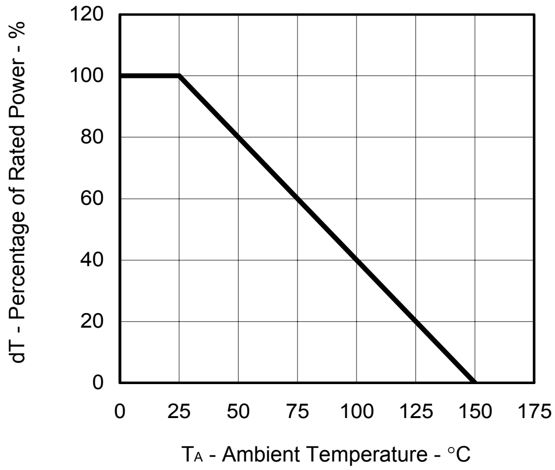


TEST CIRCUIT 3 GATE CHARGE

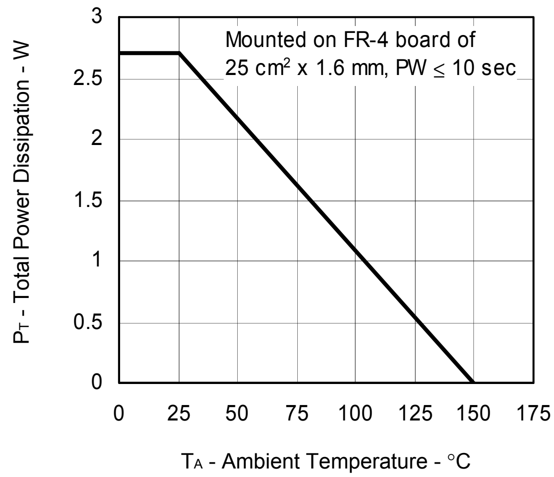


TYPICAL CHARACTERISTICS (T_A = 25°C)

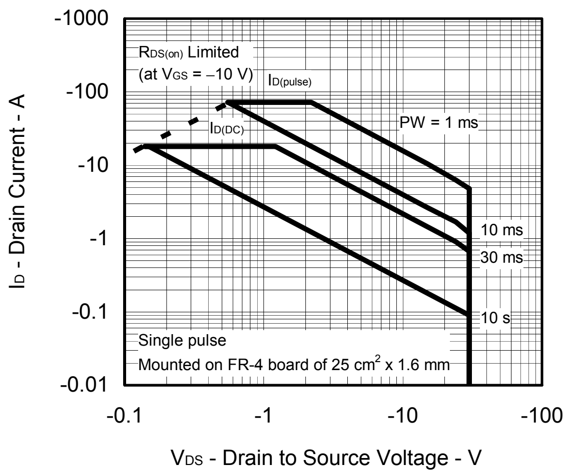
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



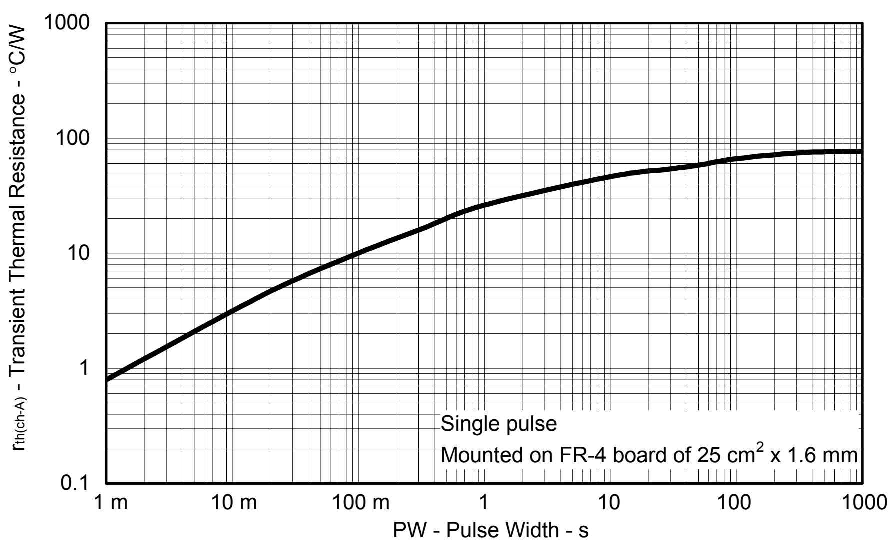
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



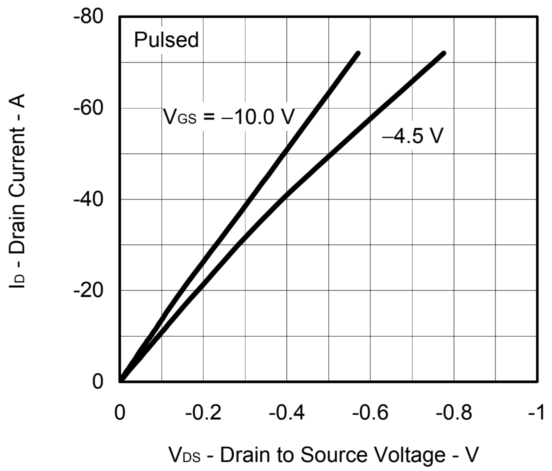
FORWARD BIAS SAFE OPERATING AREA



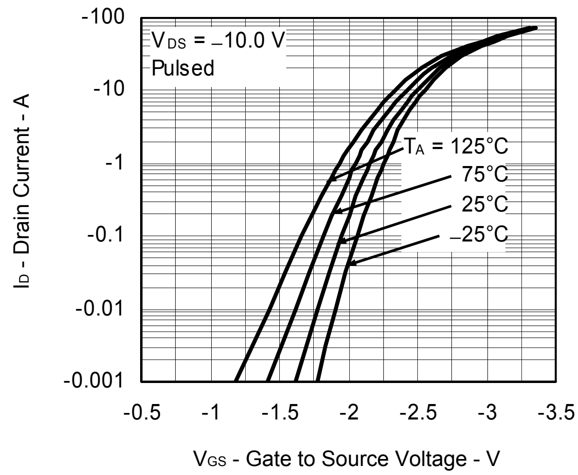
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



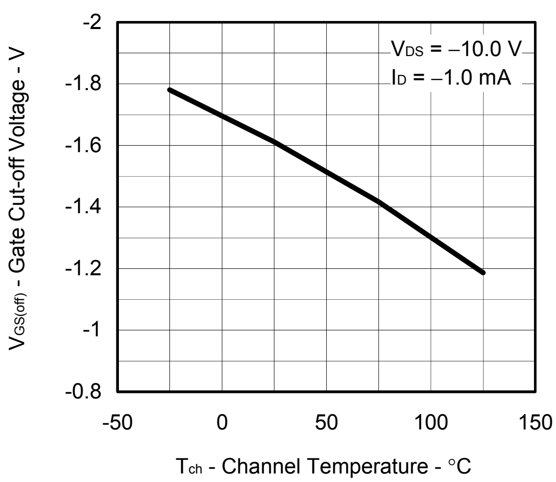
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



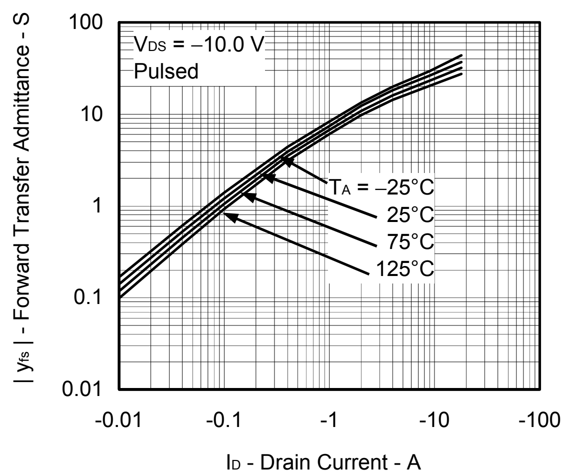
FORWARD TRANSFER CHARACTERISTICS



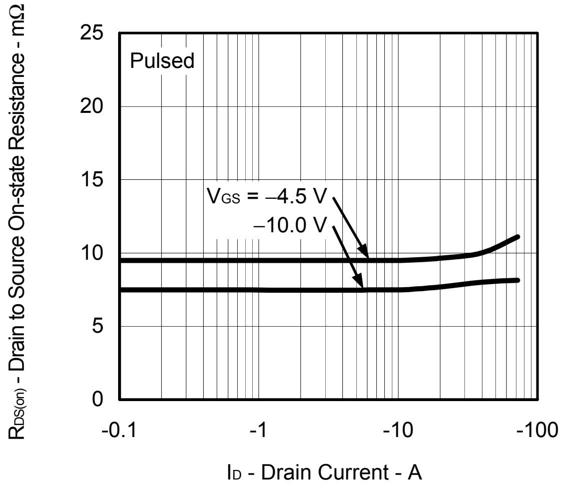
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



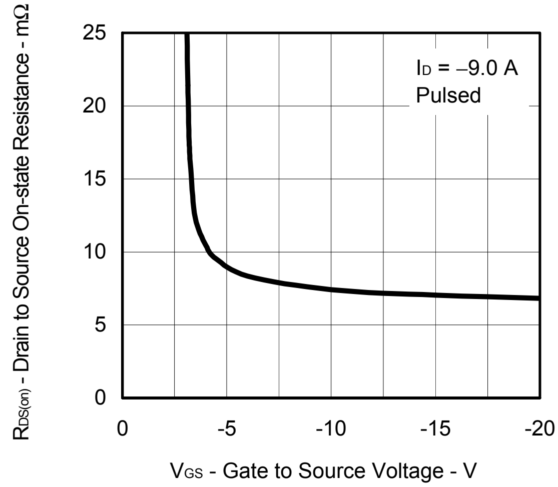
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



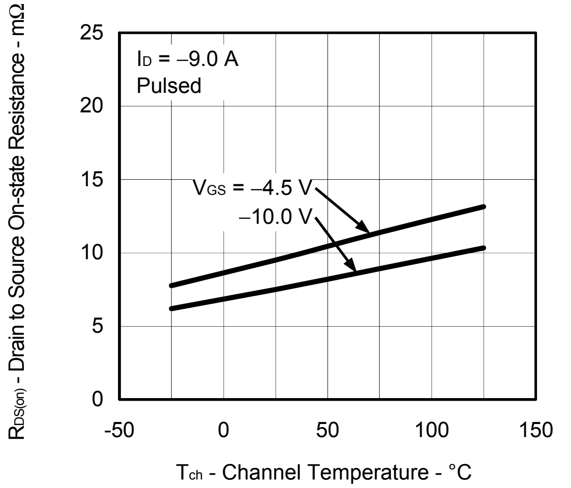
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



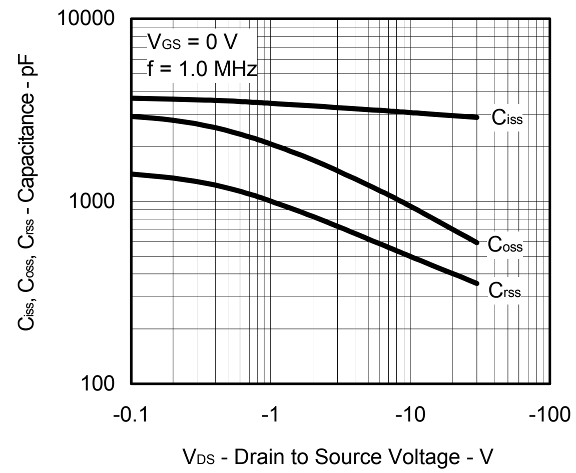
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



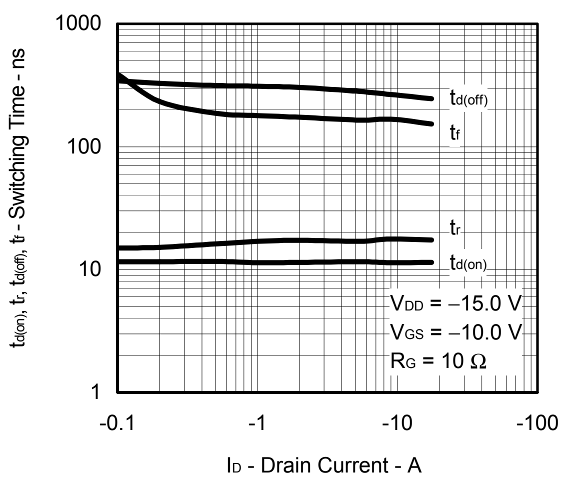
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



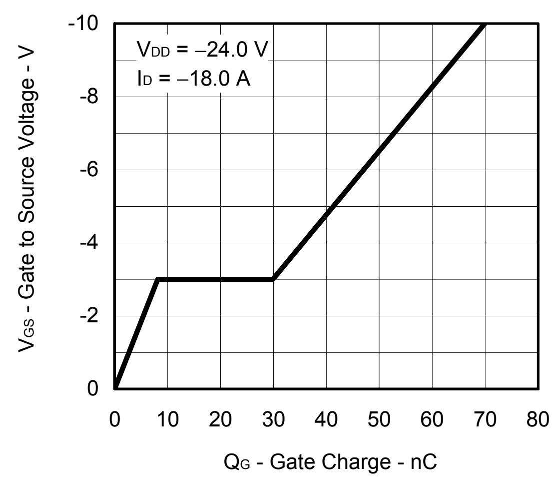
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



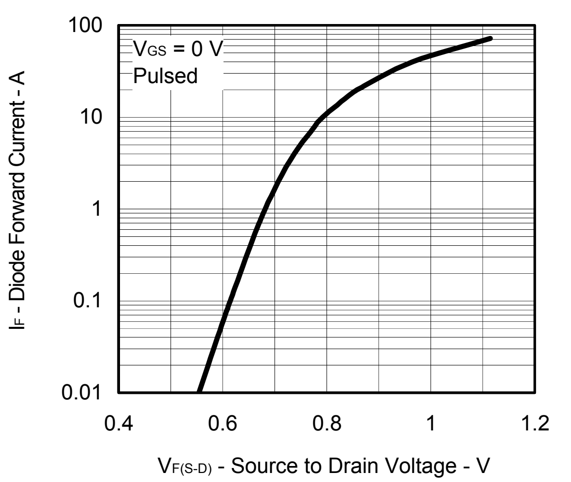
SWITCHING CHARACTERISTICS



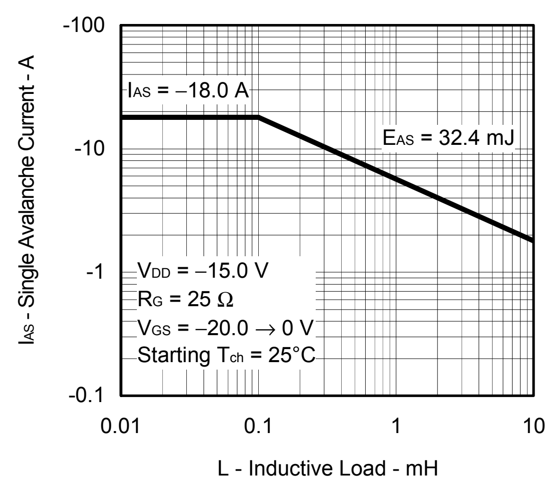
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

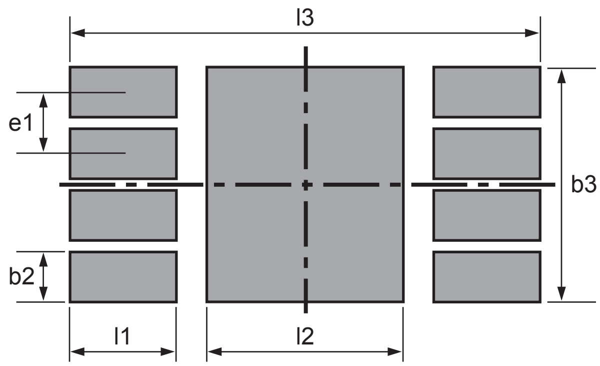


SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



EXAMPLE OF THE LAND PATTERN

Please optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.



e1: 0.65
b2: 0.35
b3: 2.7
l1: 1.3
l2: 3.7
l3: 7.1

(Unit: mm)