

MOS FIELD EFFECT TRANSISTOR μ PA2780GR

SWITCHING N-CHANNEL POWER MOS FET/SCHOTTKY BARRIER DIODE

0.05 MIN

1.27 0.78 MAX.

0.40 ^{+0.10} \oplus 0.12 M

DESCRIPTION

The μ PA2780GR is N-channel Power MOSFET, which built a Schottky Barrier Diode inside.

This product is designed for synchronous DC/DC converter application.

FEATURES

- · Built a Schottky Barrier Diode
- · Low on-state resistance

 $R_{DS(on)1} = 6.2 \text{ m}\Omega \text{ TYP.}$ (Vgs = 10 V, ID = 7 A)

 $R_{DS(on)2} = 8.7 \text{ m}\Omega \text{ TYP.} \text{ (Vgs} = 4.5 \text{ V, Ip} = 7 \text{ A)}$

RDS(on)3 = 10.3 m Ω TYP. (Vgs = 4.0 V, ID = 7 A)

- Low Ciss: Ciss = 1200 pF TYP.
- Small and surface mount package (Power SOP8)

1, 2, 3 : Source 4 : Gate 5, 6, 7, 8: Drain

PACKAGE DRAWING (Unit: mm)

ORDERING INFORMATION

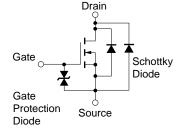
PART NUMBER	PACKAGE
μPA2780GR	Power SOP8

EQUIVALENT CIRCUIT

□ 0.10

ABSOLUTE MAXIMUM RATINGS (TA = 25°C. All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) [MOSFET]	ID(DC)	±14	Α
Drain Current (pulse) Note1	ID(pulse)	±56	Α
Average Forward Current Note2 [SCHOTTKY]	I F(AV)	2.5	Α
Total Power Dissipation Note3 [MOSFET]	PT	2	W
Total Power Dissipation Note3 [SCHOTTKY]	P⊤	1	W
Channel & Junction Temperature	T_{ch}, T_{j}	150	°C
Storage Temperature	Tstg	-55 to + 150	°C



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Rectangle wave, 50% Duty Cycle
 - 3. Mounted on ceramic substrate of 1200 mm² x 2.2 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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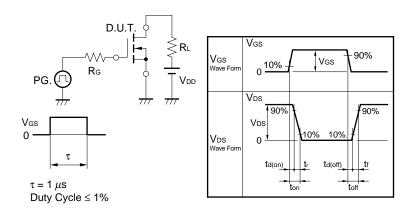


ELECTRICAL CHARACTERISTICS (TA = 25°C, unless otherwise noted. All terminals are connected.)

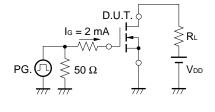
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current Note	IDSS	V _{DS} = 24 V, V _{GS} = 0 V			50	μΑ
		V _{DS} = 24 V, V _{GS} = 0 V, T _A = 125°C			10	mA
Gate Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = 10 V, ID = 7 A		6.2	7.5	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 7 A		8.7	11.6	mΩ
	RDS(on)3	Vgs = 4.0 V, ID = 7 A		10.3	13.7	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		1200		pF
Output Capacitance	Coss	V _G S = 0 V		570		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		160		pF
Turn-on Delay Time	td(on)	V _{DD} = 15 V, I _D = 7 A		10		ns
Rise Time	tr	Vgs = 10 V		13		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		44		ns
Fall Time	t _f			11		ns
Total Gate Charge	Q G	V _{DD} = 15 V		12		nC
Gate to Source Charge	Qgs	Vgs = 5 V		4		nC
Gate to Drain Charge	Q _{GD}	I _D = 14 A		6		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = 1 A, VGS = 0 V		0.45	0.5	V
		IF = 1 A, VGS = 0 V, TA = 125°C		0.37		V
Reverse Recovery Time	trr	IF = 7 A, VGS = 0 V		31		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		22		nC

Note Pulsed: PW \leq 350 μ s, Duty Cycle \leq 2%

TEST CIRCUIT 1 SWITCHING TIME



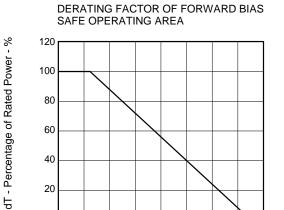
TEST CIRCUIT 2 GATE CHARGE



0

0 20 40 60

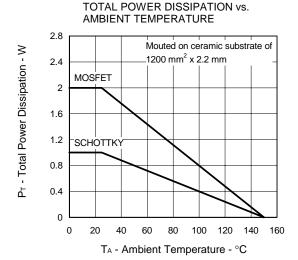
TYPICAL CHARACTERISTICS (TA = 25°C. All terminals are connected.)



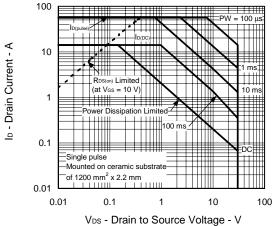
80 TA - Ambient Temperature - °C

100

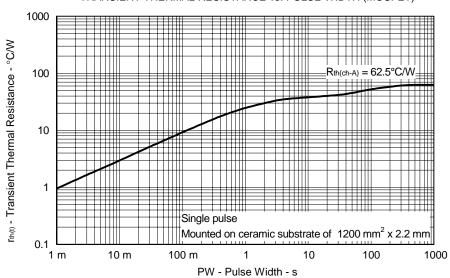
120 140 160



FORWARD BIAS SAFE OPERATING AREA

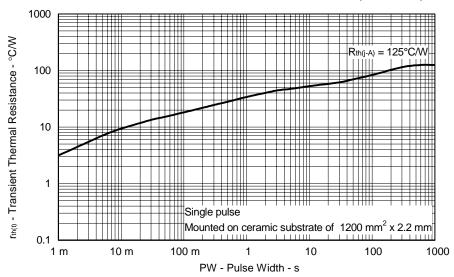


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (MOSFET)



3

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (SCHOTTKY)

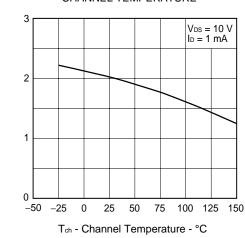


VGS(Off) - Gate Cut-off Voltage - V

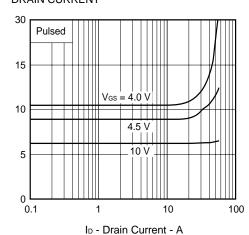
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

80 70 Ip - Drain Current - A 60 Vgs = 10 V 4.5 V 50 40 4.0 V 30 20 10 Pulsed O 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 V_{DS} - Drain to Source Voltage - V

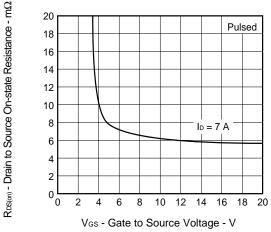
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

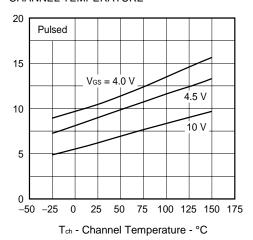


 $\mathsf{R}_{\mathsf{DS}(m)}$ - Drain to Source On-state Resistance - $m\Omega$

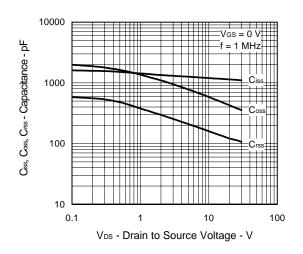
 $\mathsf{R}_{\mathsf{DS}(\sigma)}$ - Drain to Source On-state Resistance - $m\Omega$

ta(on), tr, ta(off), tr - Switching Time - ns

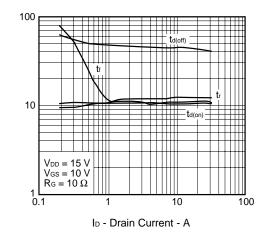
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



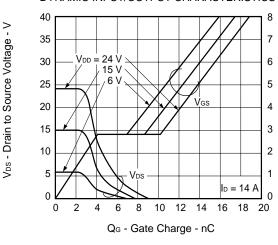
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



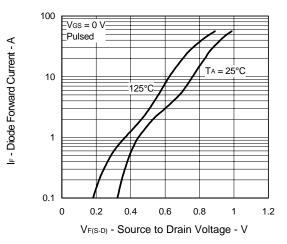
SWITCHING CHARACTERISTICS



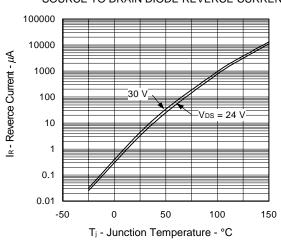
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



SOURCE TO DRAIN DIODE REVERCE CURRENT



Ves - Gate to Source Voltage - V

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