

MOS FIELD EFFECT TRANSISTOR μ PA2782GR

SWITCHING N-CHANNEL POWER MOS FET/SCHOTTKY BARRIER DIODE

DESCRIPTION

The μ PA2782GR is N-Channel Power MOSFET, which built a Schottky Barrier Diode inside.

This product is designed for synchronous DC/DC converter application.

FEATURES

- · Built a Schottky Barrier Diode
- · Low on-state resistance

RDS(on)1 = 11 m Ω TYP. (Vgs = 10 V, ID = 5.5 A)

RDS(on)2 = 16 m Ω TYP. (VGS = 4.5 V, ID = 5.5 A)

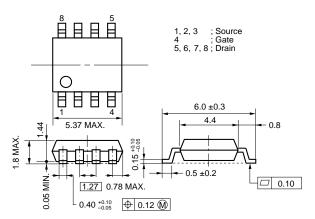
RDS(on)3 = 19 m Ω TYP. (VGS = 4.0 V, ID = 5.5 A)

- Low Ciss: Ciss = 660 pF TYP.
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2782GR	Power SOP8

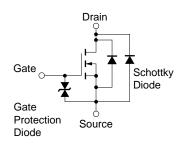
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}$ C. All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) [MOSFET]	ID(DC)	±11	Α
Drain Current (pulse) Note1	ID(pulse)	±44	Α
Average Forward Current Note2 [SCHOTTKY]	I F(AV)	2.5	Α
Total Power Dissipation Note3 [MOSFET]	PT	2	W
Total Power Dissipation Note3 [SCHOTTKY]	Рт	1	W
Channel & Junction Temperature	T_{ch}, T_{j}	150	°C
Storage Temperature	T _{stg}	-55 to + 150	$^{\circ}$

EQUIVALENT CIRCUIT



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Rectangle wave, 50% Duty Cycle
 - 3. Mounted on ceramic substrate of 1200 mm² x 2.2 mm

Caution Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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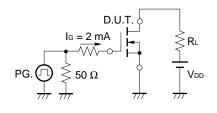
ELECTRICAL CHARACTERISTICS (TA = 25°C, unless other wise noted. All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current Note	Ipss	Vps = 24 V, Vgs = 0 V			50	μΑ
		V _{DS} = 24 V, V _{GS} = 0 V, T _A = 125° C			10	mA
Gate Leakage Current	Igss	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = 10 V, ID = 5.5 A		11	15	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 5.5 A		16	22.5	mΩ
	RDS(on)3	Vgs = 4.0 V, ID = 5.5 A		19	29	mΩ
Input Capacitance	Ciss	Vps = 10 V		660		pF
Output Capacitance	Coss	Vgs = 0 V		340		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		83		pF
Turn-on Delay Time	t _{d(on)}	VDD = 15 V, ID = 5.5 A		9		ns
Rise Time	tr	Vgs = 10 V		5		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 10 \Omega$		29		ns
Fall Time	tf			6		ns
Total Gate Charge	Q _G	V _{DD} = 15 V		7.1		nC
Gate to Source Charge	Qgs	Vgs = 5 V		2.1		nC
Gate to Drain Charge	Q _{GD}	ID = 11 A		3.1		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 1 A, VGS = 0 V		0.45	0.5	V
		IF = 1 A, VGS = 0 V, TA = 125° C		0.37		V
Reverse Recovery Time	trr	IF = 7 A, VGS = 0 V		25		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		14		nC

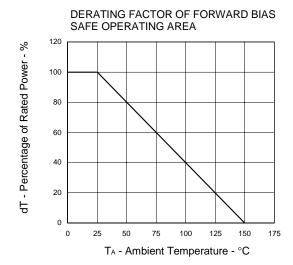
Note Pulsed: PW \leq 350 μ s, Duty Cycle \leq 2%

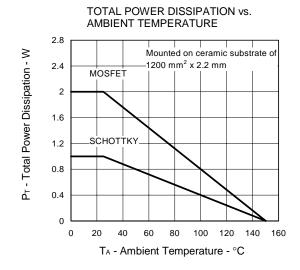
TEST CIRCUIT 1 SWITCHING TIME

TEST CIRCUIT 2 GATE CHARGE



TYPICAL CHARACTERISTICS (TA = 25°C. All terminals are connected.)

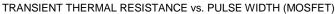


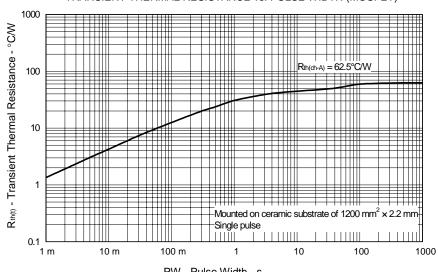


100 PW = 100 μs lo - Drain Current - A 10 (at Vgs = 10 V) 100 ms Single pulse Mounted on ceramic substrate of 1200 mm² x 2.2 mm

FORWARD BIAS SAFE OPERATING AREA

VDS - Drain to Source Voltage - V

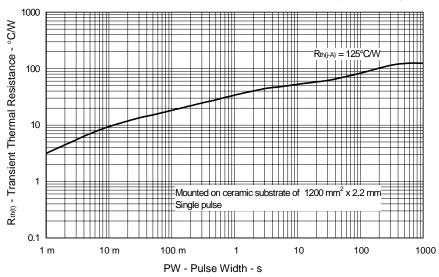




PW - Pulse Width - s

0.01

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (SCHOTTKY)

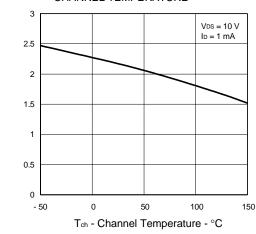


VGS(off) - Gate Cut-off Voltage - V

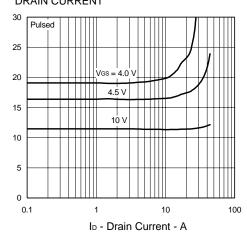
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

50 Pulsed 45 40 lo - Drain Current - A Vgs = 10 V 35 30 4.0 V 25 20 15 10 5 0 0.5 1.5 2 0 V_{DS} - Drain to Source Voltage - V

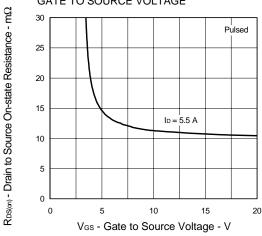
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

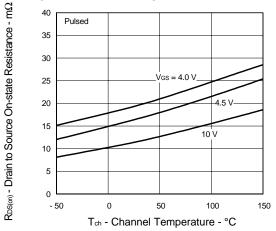


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

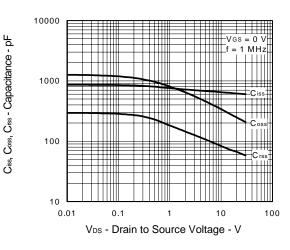


RDS(m) - Drain to Source On-state Resistance - mΩ

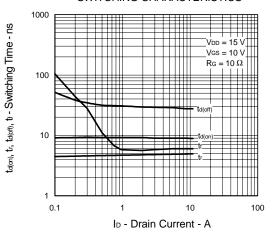
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



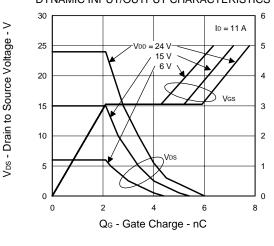
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



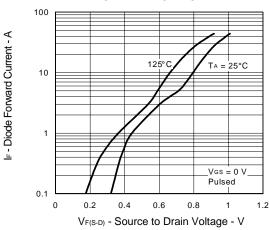
SWITCHING CHARACTERISTICS



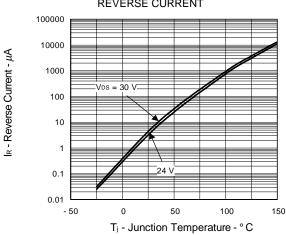
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



SOURCE TO DRAIN DIODE REVERSE CURRENT



5

Ves - Gate to Source Voltage - V

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