

# MOS FIELD EFFECT TRANSISTOR $\mu$ PA2754GR

# SWITCHING N-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The  $\mu$ PA2754GR is Dual N-channel MOS Field Effect Transistor designed for Li-ion battery protection circuit and power management application.

#### **FEATURES**

- · Dual chip type
- Low on-state resistance

RDS(on)1 = 14.5 m $\Omega$  MAX. (Vgs = 4.5 V, ID = 5.5 A)

 $R_{DS(on)2} = 15.0 \text{ m}\Omega$  MAX. (Vgs = 4.0 V, ID = 5.5 A)

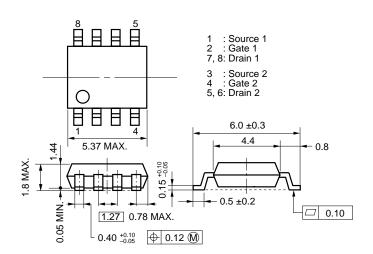
RDS(on)4 = 18.6 m $\Omega$  MAX. (Vgs = 2.5 V, ID = 5.5 A)

- Low Ciss: Ciss = 1940 pF TYP. (VDS = 10 V, VGS = 0 V)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2754GR	Power SOP8

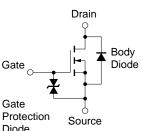
# PACKAGE DRAWING (Unit: mm)



## ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V	
Gate to Source Voltage (Vps = 0 V)	Vgss	±12	V	EQUI
Drain Current (DC) Note2	I <sub>D(DC)</sub>	±11	Α	
Drain Current (pulse) Note1	ID(pulse)	±88	Α	
Total Power Dissipation (2 units) Note2	PT	2.0	W	
Total Power Dissipation (1 unit) Note2	Рт	1.7	W	
Channel Temperature	Tch	150	°C	Gate
Storage Temperature	Tstg	-55 to +150	°C	, and the second se
Single Avalanche Current Note3	las	11	Α	Gate
Single Avalanche Energy Note3	Eas	12.1	mJ	Protec Diode

EQUIVALENT CIRCUIT (1/2 circuit)



- **Notes 1.** PW  $\leq$  10  $\mu$ s, Duty cycle  $\leq$  1%
  - **2.**  $T_A = 25^{\circ}C$ , Mounted on ceramic substrate of 2000 mm<sup>2</sup> x 2.2 mm
  - 3. Starting Tch = 25°C, Vdd = 15 V, Rg = 25  $\Omega$ , Vgs = 12  $\rightarrow$  0 V

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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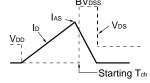
# **ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μΑ
Gate Leakage Current	Igss	Vgs = ±12 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage Note	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	0.5		1.5	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.5 A	8	16		S
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = 4.5 V, ID = 5.5 A		11.5	14.5	mΩ
	RDS(on)2	Vgs = 4.0 V, ID = 5.5 A		11.8	15.0	mΩ
	RDS(on)3	Vgs = 3.1 V, ID = 5.5 A		12.7	16.9	mΩ
	RDS(on)4	Vgs = 2.5 V, ID = 5.5 A		13.9	18.6	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		1940		pF
Output Capacitance	Coss	Vgs = 0 V		385		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		270		pF
Turn-on Delay Time	td(on)	VDD = 15 V, ID = 5.5 A		21		ns
Rise Time	tr	Vgs = 4.5 V		45		ns
Turn-off Delay Time	td(off)	$R_G = 10 \Omega$		75		ns
Fall Time	tf			30		ns
Total Gate Charge	<b>Q</b> G	V <sub>DD</sub> = 24 V		25		nC
Gate to Source Charge	Qgs	V <sub>G</sub> S = 4.5 V		3		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 11 A		10		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 11 A, VGS = 0 V		0.81	1.2	V
Reverse Recovery Time	trr	IF = 11 A, VGS = 0 V		47		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		41		nC

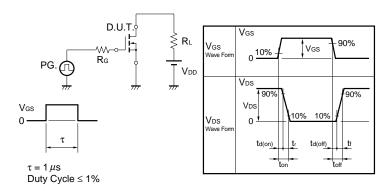
**Note** Pulsed: PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $R_{G} = 25 \Omega$ $V_{CS} = 20 \rightarrow 0 V$ $R_{G} = 25 \Omega$ $V_{DU}$ $V_{DD}$ $V_{DD}$



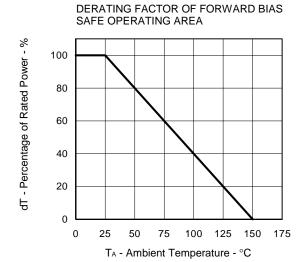
## TEST CIRCUIT 2 SWITCHING TIME

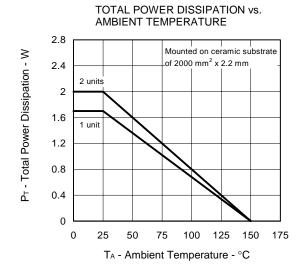


# **TEST CIRCUIT 3 GATE CHARGE**

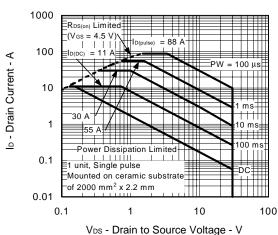
$$\begin{array}{c|c}
D.U.T. \\
I_G = 2 \text{ mA} \\
\hline
NOTICE \\
\hline
PG. \bigcirc \\
\hline
S 50 \Omega
\end{array}$$

# TYPICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

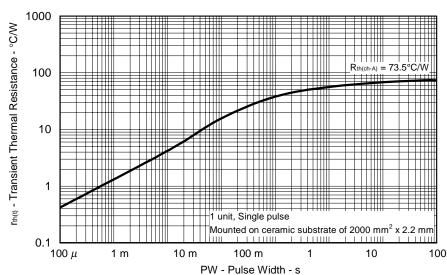




#### FORWARD BIAS SAFE OPERATING AREA

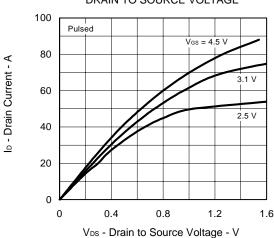


#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

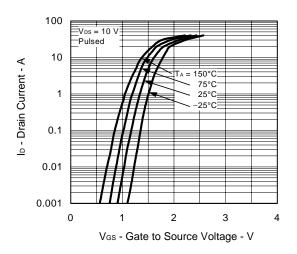


3

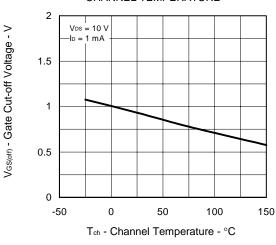
# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



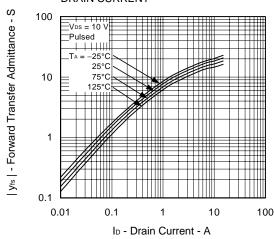
#### FORWARD TRANSFER CHARACTERISTICS



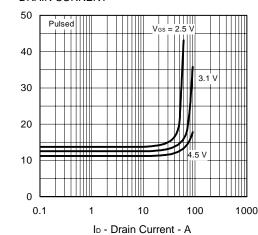
# GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



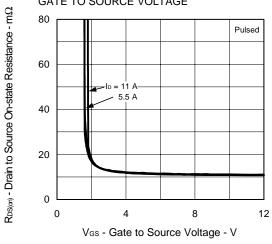
# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



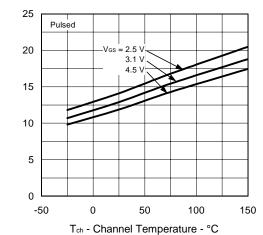
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



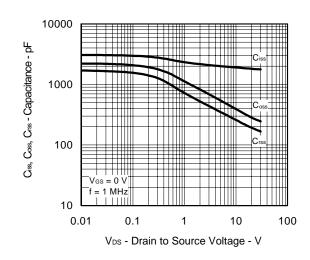
R<sub>DS(σ1)</sub> - Drain to Source On-state Resistance - mΩ

 $\mathsf{Ros}_{(\alpha)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

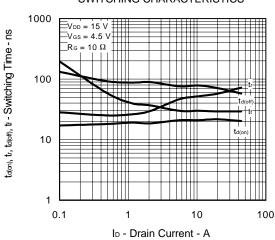
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



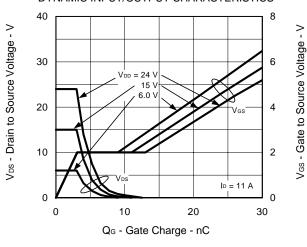
#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



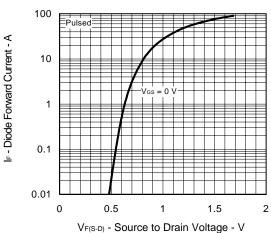
#### SWITCHING CHARACTERISTICS



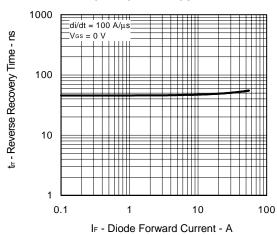
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



# SOURCE TO DRAIN DIODE FORWARD VOLTAGE

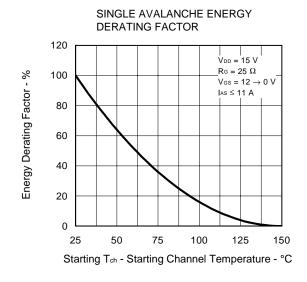


# REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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# SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD 100 Inductive Load - mH



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