DATA SHEET

# MOS FIELD EFFECT TRANSISTOR
# μPA2754GR

## SWITCHING
## N-CHANNEL POWER MOS FET

### DESCRIPTION

The μPA2754GR is Dual N-channel MOS Field Effect Transistor designed for Li-ion battery protection circuit and power management application.

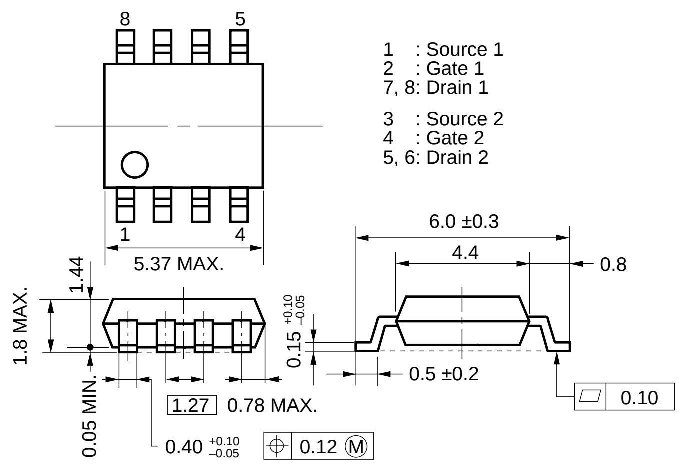
### FEATURES

- Dual chip type
- Low on-state resistance
  $R_{DS(on)1}$ = 14.5 mΩ MAX. ($V_{GS}$ = 4.5 V, $I_D$ = 5.5 A)
  $R_{DS(on)2}$ = 15.0 mΩ MAX. ($V_{GS}$ = 4.0 V, $I_D$ = 5.5 A)
  $R_{DS(on)4}$ = 18.6 mΩ MAX. ($V_{GS}$ = 2.5 V, $I_D$ = 5.5 A)
- Low $C_{iss}$: $C_{iss}$ = 1940 pF TYP. ($V_{DS}$ = 10 V, $V_{GS}$ = 0 V)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| μPA2754GR | Power SOP8 |

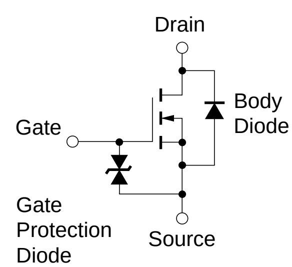
### PACKAGE DRAWING (Unit: mm)




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, All terminals are connected.)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | 30 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ±12 | V |
| Drain Current (DC) Note2 | $I_{D(DC)}$ | ±11 | A |
| Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ±88 | A |
| Total Power Dissipation (2 units) Note2 | $P_T$ | 2.0 | W |
| Total Power Dissipation (1 unit) Note2 | $P_T$ | 1.7 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| Single Avalanche Current Note3 | $I_{AS}$ | 11 | A |
| Single Avalanche Energy Note3 | $E_{AS}$ | 12.1 | mJ |

### EQUIVALENT CIRCUIT
### (1/2 circuit)




**Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1%

**2.** $T_A$ = 25°C, Mounted on ceramic substrate of 2000 mm$^2$ x 2.2 mm

**3.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = 15 V, $R_G$ = 25 Ω, $V_{GS}$ = 12 → 0 V

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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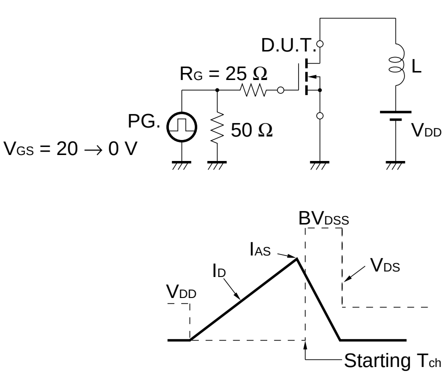
Document No. G15816EJ1V0DS00 (1st edition)
Date Published January 2003 NS CP(K)
Printed in Japan

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C, All terminals are connected.)

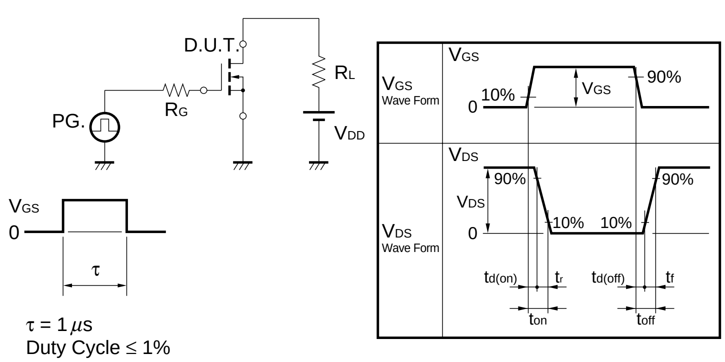
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V | | | 1 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Gate Cut-off Voltage Note | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 0.5 | | 1.5 | V |
| Forward Transfer Admittance Note | $\| y_{fs} \|$ | $V_{DS}$ = 10 V, $I_D$ = 5.5 A | 8 | 16 | | S |
| Drain to Source On-state Resistance Note | $R_{DS(on)1}$ | $V_{GS}$ = 4.5 V, $I_D$ = 5.5 A | | 11.5 | 14.5 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4.0 V, $I_D$ = 5.5 A | | 11.8 | 15.0 | mΩ |
| | $R_{DS(on)3}$ | $V_{GS}$ = 3.1 V, $I_D$ = 5.5 A | | 12.7 | 16.9 | mΩ |
| | $R_{DS(on)4}$ | $V_{GS}$ = 2.5 V, $I_D$ = 5.5 A | | 13.9 | 18.6 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V | | 1940 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 385 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 270 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15 V, $I_D$ = 5.5 A | | 21 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = 4.5 V | | 45 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 10 Ω | | 75 | | ns |
| Fall Time | $t_f$ | | | 30 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 24 V | | 25 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 4.5 V | | 3 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = 11 A | | 10 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 11 A, $V_{GS}$ = 0 V | | 0.81 | 1.2 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 11 A, $V_{GS}$ = 0 V | | 47 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 41 | | nC |

**Note** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

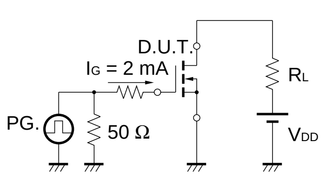
### TEST CIRCUIT 1 AVALANCHE CAPABILITY



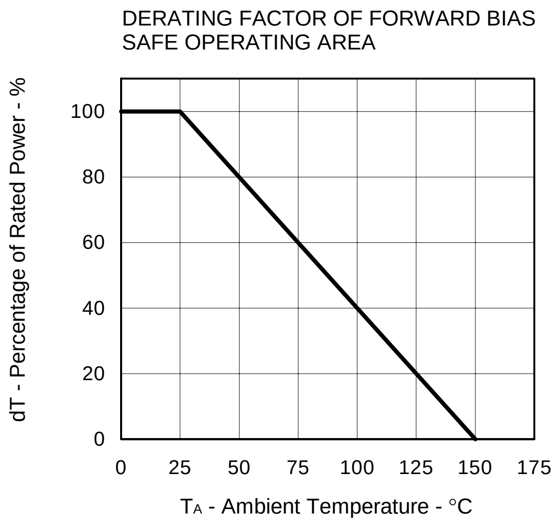

### TEST CIRCUIT 2 SWITCHING TIME

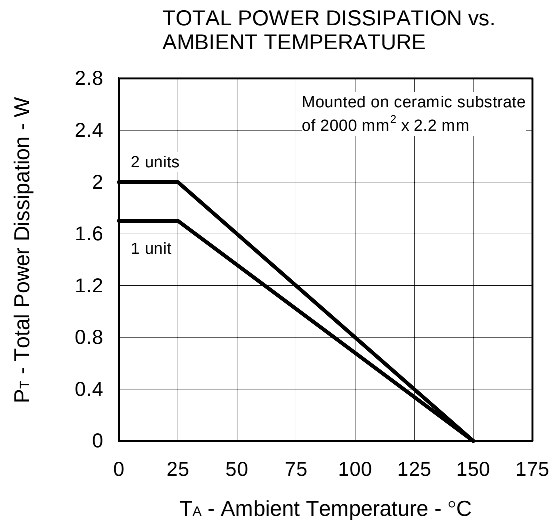


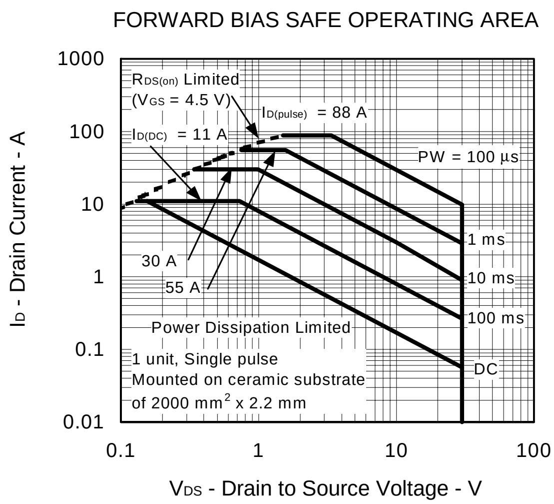

### TEST CIRCUIT 3 GATE CHARGE

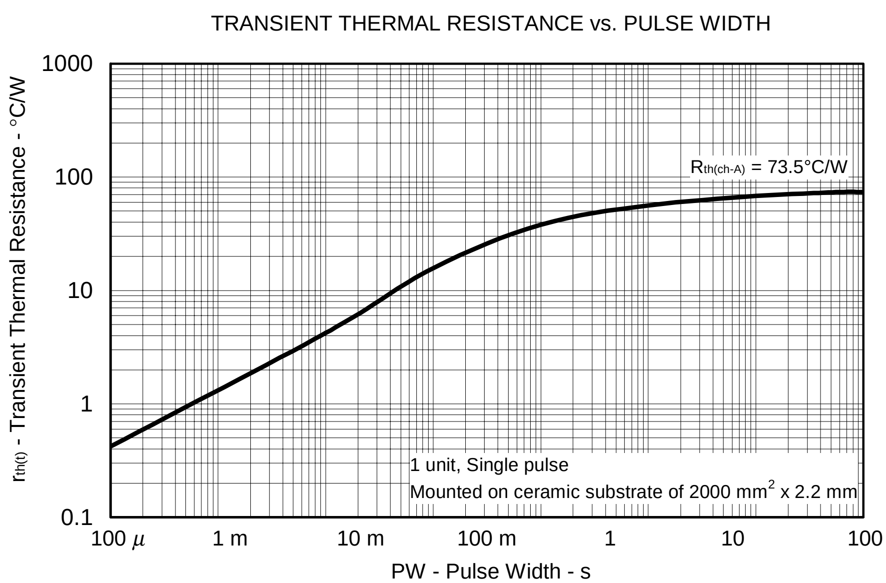


**TYPICAL CHARACTERISTICS ($T_A$ = 25°C, All terminals are connected.)**

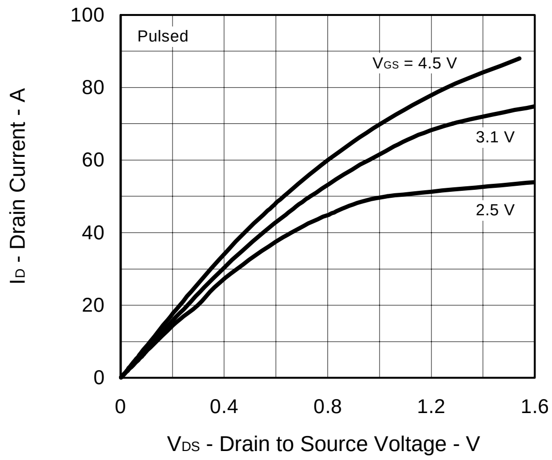


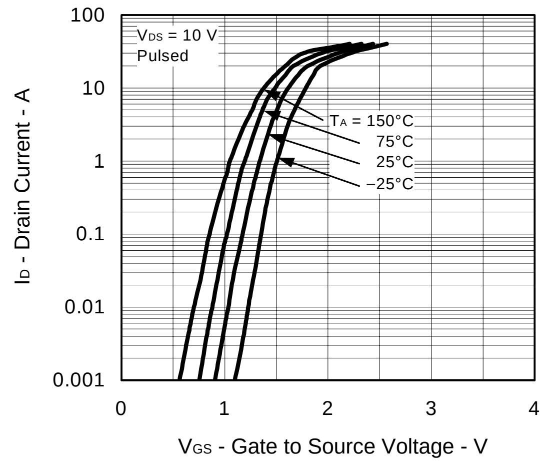



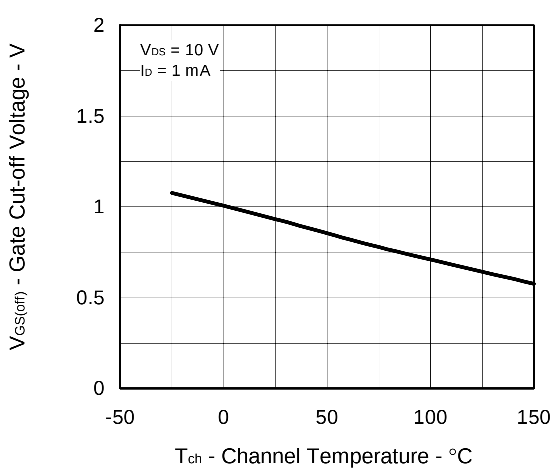
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



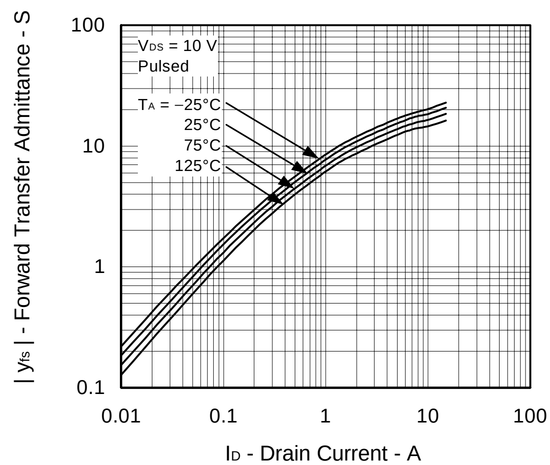

FORWARD TRANSFER CHARACTERISTICS



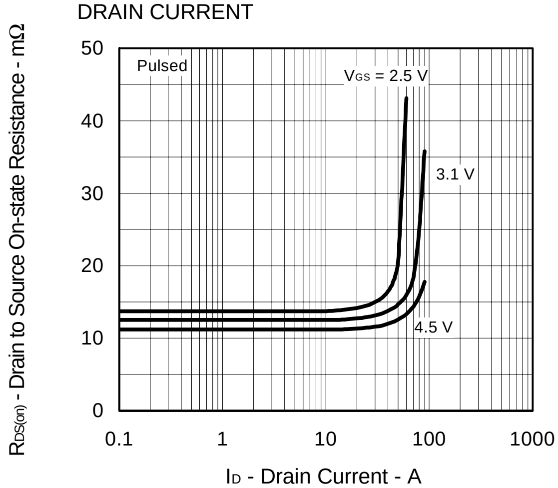

GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



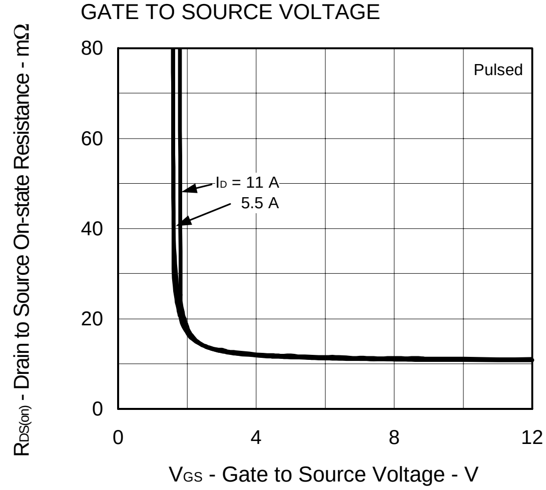

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



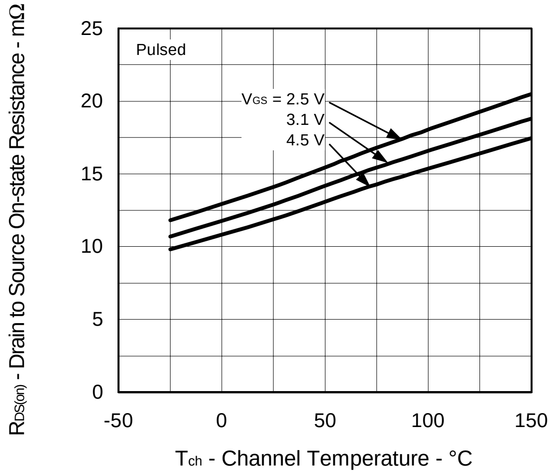

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



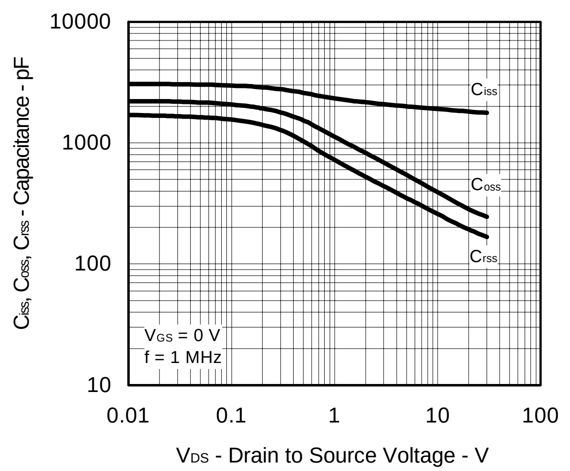

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



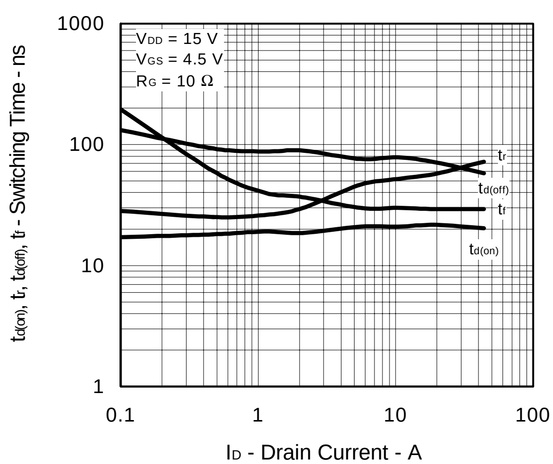
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



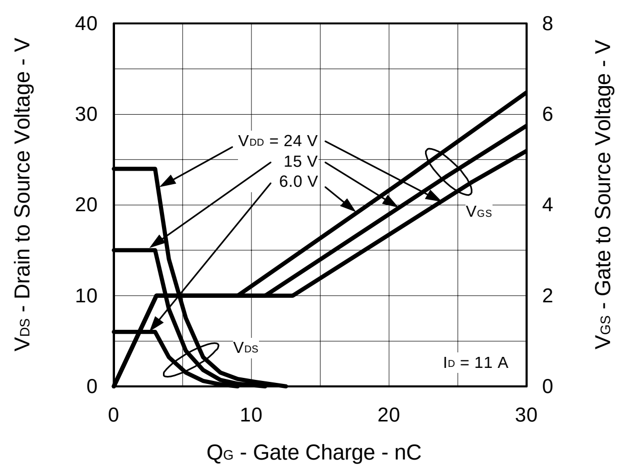

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



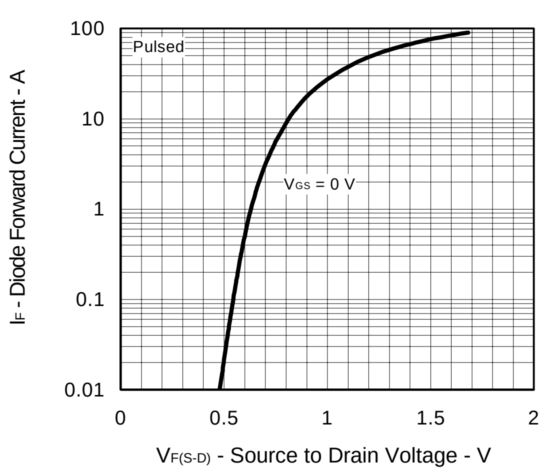

SWITCHING CHARACTERISTICS



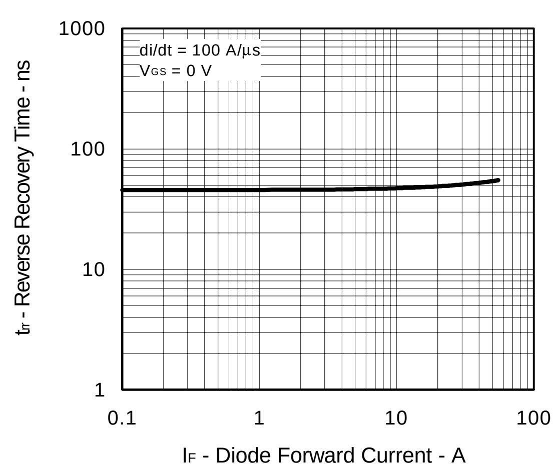

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



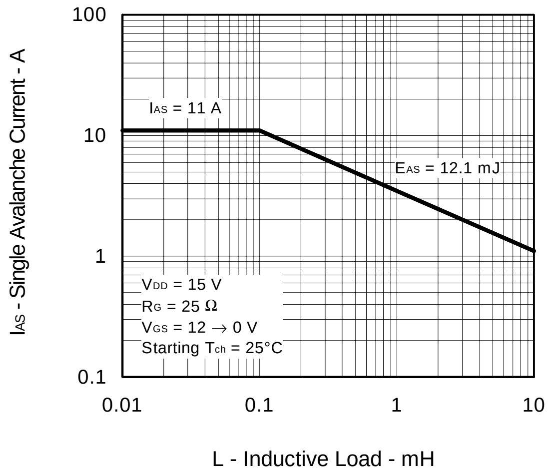

SOURCE TO DRAIN DIODE FORWARD VOLTAGE




REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD




SINGLE AVALANCHE ENERGY DERATING FACTOR