

MOS FIELD EFFECT TRANSISTOR μ PA2733GR

SWITCHING P-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2733GR is P-channel MOS Field Effect Transistor designed for power management applications of notebook computers and so on.

FEATURES

· Low on-state resistance

 $R_{DS(on)1}$ = 38 m Ω MAX. (Vgs = -10 V, Ip = -2.5 A)

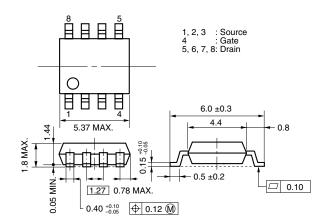
 $R_{DS(on)2} = 53 \text{ m}\Omega \text{ MAX.}$ (Vgs = -4.5 V, ID = -2.5 A)

- Low Ciss: Ciss = 870 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

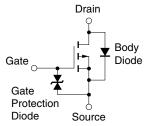
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2733GR-E1	Power SOP8
μ PA2733GR-E1-A $^{ m f Note}$	Power SOP8
μ PA2733GR-E2	Power SOP8
μ PA2733GR-E2-A Note	Power SOP8

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



μ PA2733GR-E2-A ^{Note}	Power SOP8					
Note Pb-free (This product does not contain Pb in external electrode and other part						

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC)	ID(DC)	∓5	Α
Drain Current (pulse) Note1	D(pulse)	∓20	Α
Total Power Dissipation Note2	P _{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) Note2	PT2	2.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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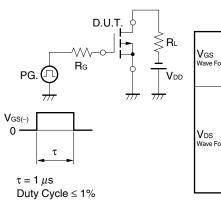


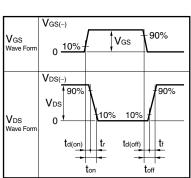
ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -30 V, V _{GS} = 0 V			-1	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.0		-2.5	V
Forward Transfer Admittance Note	y _{fs}	$V_{DS} = -10 \text{ V}, I_{D} = -2.5 \text{ A}$	2.5			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = -10 V, I _D = -2.5 A		30	38	mΩ
	RDS(on)2	V _{GS} = -4.5 V, I _D = -2.5 A		39	53	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		870		pF
Output Capacitance	Coss	V _{GS} = 0 V		200		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		150		pF
Turn-on Delay Time	t _{d(on)}	$V_{DD} = -15 \text{ V}, I_D = -2.5 \text{ A}$		7.7		ns
Rise Time	tr	V _{GS} = -10 V		9.5		ns
Turn-off Delay Time	t d(off)	R _G = 10 Ω		108		ns
Fall Time	t _f			64		ns
Total Gate Charge	Q _G	V _{DD} = -24 V		18		nC
Gate to Source Charge	Qgs	V _{GS} = -10 V		2.6		nC
Gate to Drain Charge	Q _{GD}	I _D = -5 A		5.8		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 5 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	trr	I _F = 5 A, V _{GS} = 0 V		98		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>μ</i> s		93		nC

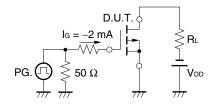
Note Pulsed

TEST CIRCUIT 1 SWITCHING TIME



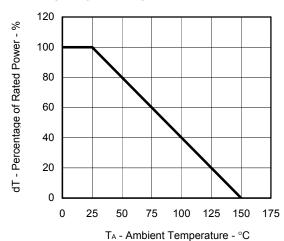


TEST CIRCUIT 2 GATE CHARGE

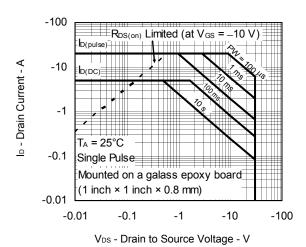


<R> TYPICAL CHARACTERISTICS (TA = 25°C)

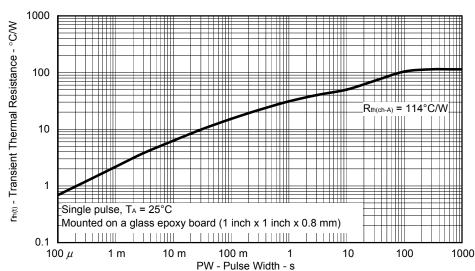
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



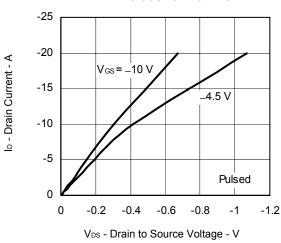
FORWARD BIAS SAFE OPERATING AREA



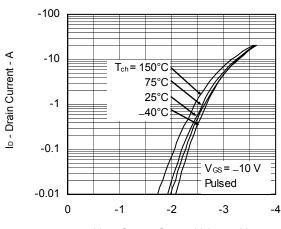
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



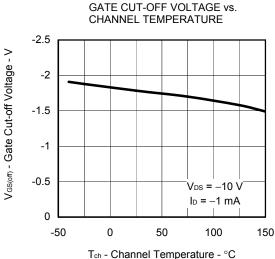
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS

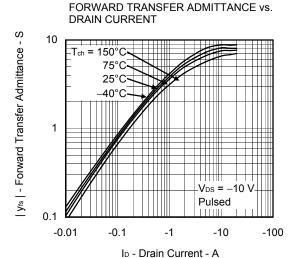


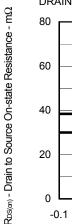
V_{GS} - Gate to Source Voltage - V

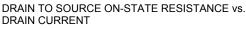


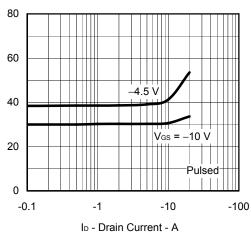


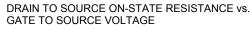
R_{DS(m)} - Drain to Source On-state Resistance - mΩ

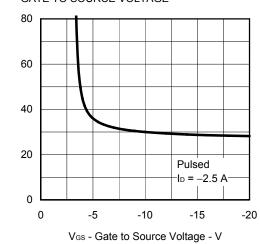




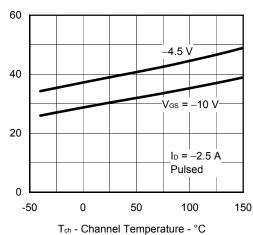




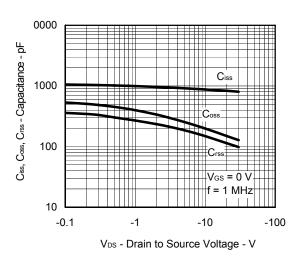




DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

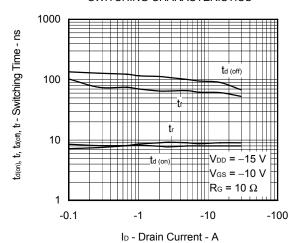


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

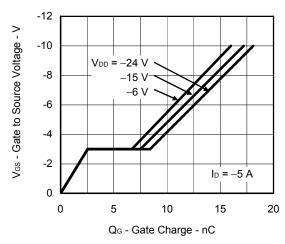


R_{DS(m)} - Drain to Source On-state Resistance - mΩ

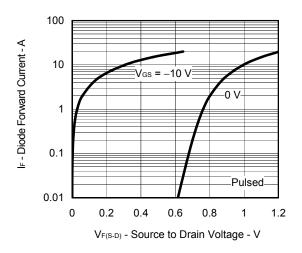
SWITCHING CHARACTERISTICS



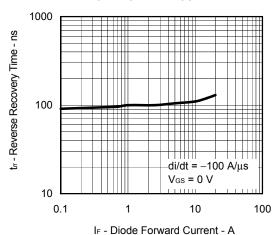
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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