

MOS FIELD EFFECT TRANSISTOR μ PA2710GR

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2710GR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

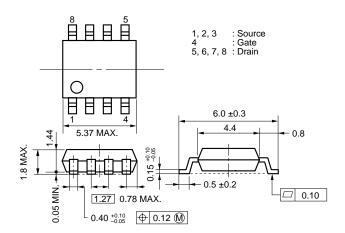
FEATURES

- · Low on-state resistance
 - RDS(on)1 = $5.5 \text{ m}\Omega$ MAX. (VGS = -10 V, ID = -7.5 A)
 - $R_{DS(on)2}$ = 9.0 m Ω MAX. (Vgs = -4.5 V, ID = -7.5 A)
 - RDS(on)3 = 11 m Ω MAX. (VGS = -4.0 V, ID = -7.5 A)
- ★ Low Ciss: Ciss = 4300 pF TYP.
 - Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2710GR	Power SOP8

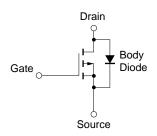
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vss = 0 V)	Voss	-30	V
Gate to Source Voltage (Vps = 0 V)	Vgss	∓20	V
Drain Current (DC)	ID(DC)	∓15	Α
Drain Current (pulse) Note1	I _{D(pulse)}	∓100	Α
Total Power Dissipation Note2	P _{T1}	2	W
Total Power Dissipation Note3	P _{T2}	2	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to + 150	°C
Single Avalanche Current Note4	las	-15	Α
Single Avalanche Energy Note4	Eas	22.5	mJ

EQUIVALENT CIRCUIT



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm
 - 3. Mounted on a glass epoxy board (1 inch x 1 inch x 0.8 mm), PW = 10 sec
 - **4.** Starting T_{ch} = 25°C, V_{DD} = -15 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = -20 \rightarrow 0 V

Remark

Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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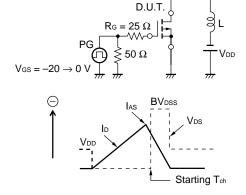


★ ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

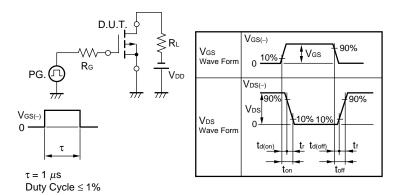
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	V _{DS} = -30 V, V _{GS} = 0 V			-1	μΑ
Gate Leakage Current	Igss	V _G S = ∓20 V, V _D S = 0 V			∓100	nA
Gate Cut-off Voltage Note	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.0		-2.5	V
Forward Transfer Admittance Note	yfs	$V_{DS} = -10 \text{ V}, I_{D} = -7.5 \text{ A}$	14	31		S
Drain to Source On-state Resistance Note	RDS(on)1	V _G S = -10 V, I _D = -7.5 A		4.7	5.5	mΩ
	RDS(on)2	V _G S = -4.5 V, I _D = -7.5 A		6.4	9.0	mΩ
	R _{DS(on)3}	V _G S = -4.0 V, I _D = -7.5 A		7.2	11	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		4300		pF
Output Capacitance	Coss	V _G S = 0 V		1200		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		690		pF
Turn-on Delay Time	td(on)	$V_{DD} = -15 \text{ V}, I_D = -7.5 \text{ A}$		11		ns
Rise Time	tr	V _G S = -10 V		22		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		420		ns
Fall Time	t f			240		ns
Total Gate Charge	Q _G	V _{DD} = -24 V		97		nC
Gate to Source Charge	Qgs	Vgs = -10 V		12		nC
Gate to Drain Charge	Q _{GD}	I _D = -15 A		29		nC
Body Diode Forward Voltage	V _F (S-D)	IF = 15 A, VGS = 0 V		0.79		V
Reverse Recovery Time	trr	I _F = 15 A, V _G s = 0 V		119		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/μs		84		nC

Note Pulsed PW≤350 μs, Duty Cycle≤2%

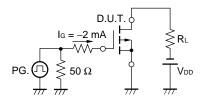
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

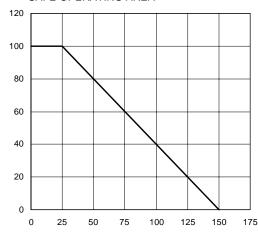


dT - Percentage of Rated Power - %

lo - Drain Current - A

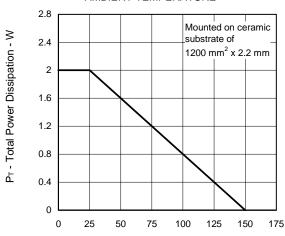
TYPICAL CHARACTERISTICS (TA = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



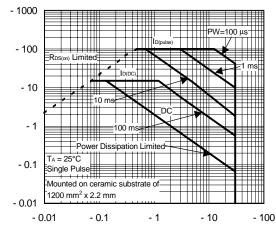
T_A - Ambient Temperature - °C

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



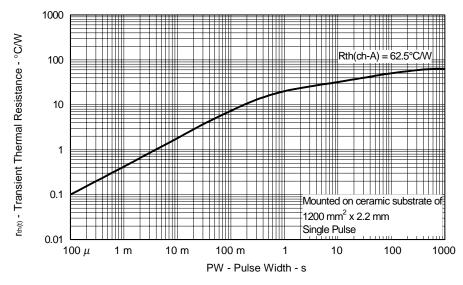
T_A - Ambient Temperature - °C

★ FORWARD BIAS SAFE OPERATING AREA



V_{DS} - Drain to Source Voltage - V

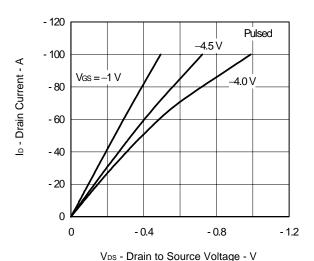
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



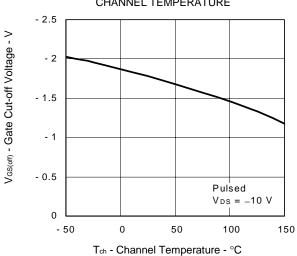
Data Sheet G15978EJ3V0DS

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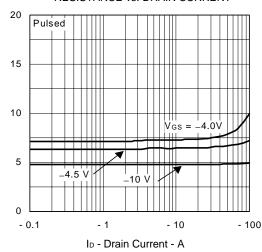
★ DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



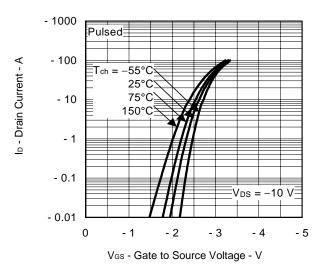
★ GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



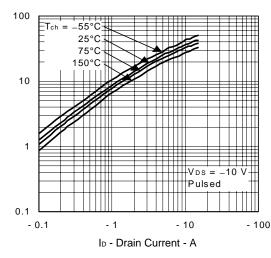
★ DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



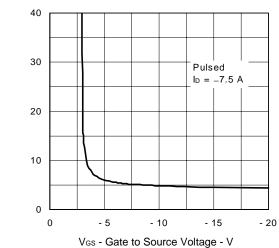
★ FORWARD TRANSFER CHARACTERISTICS



★ FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



★ DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



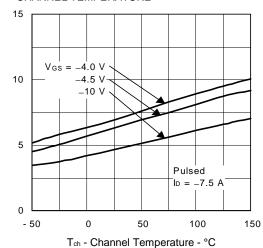
RDS(m) - Drain to Source On-state Resistance - m\Omega

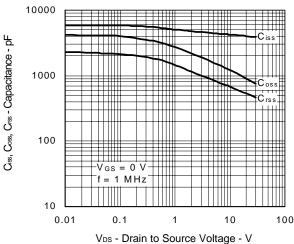
| y_{fs} | - Forward Transfer Admittance - S

 $R_{DS(m)}$ - Drain to Source On-state Resistance - $m\Omega$

RDS(m) - Drain to Source On-state Resistance - m\Omega

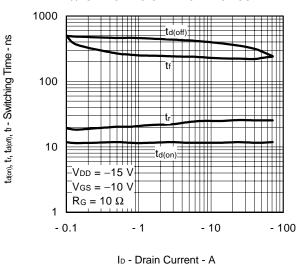
DRAIN TO SOURCE ON-STATERESISTANCE vs. CHANNEL TEMPERATURE



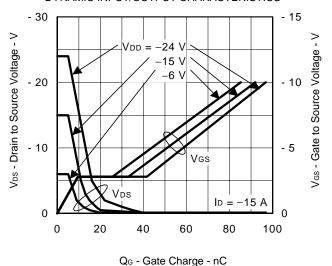


★ CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

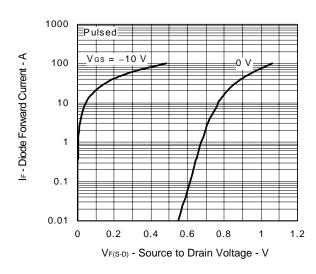
★ SWITCHING CHARACTERISTICS



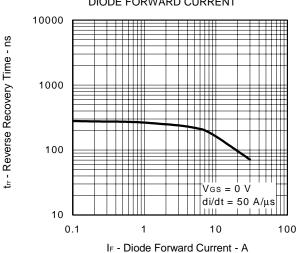
★ DYNAMIC INPUT/OUTPUT CHARACTERISTICS



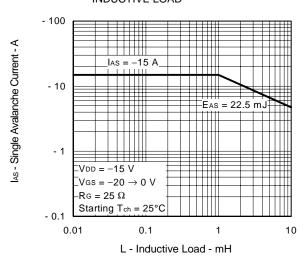
★ SOURCE TO DRAIN DIODE FORWARD VOLTAGE



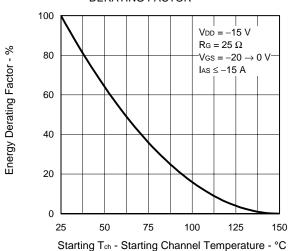
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



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