DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
μPA2719AGR

SWITCHING
P-CHANNEL POWER MOS FET

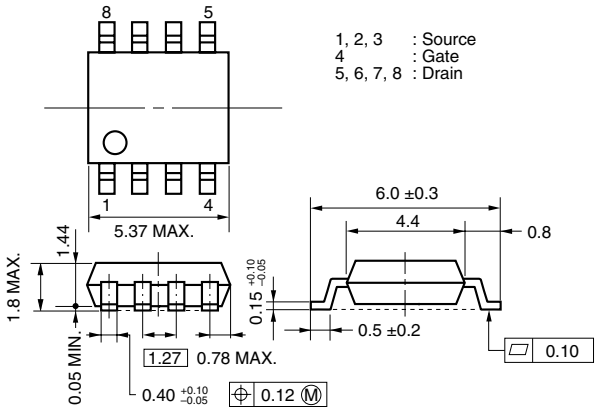
DESCRIPTION

The μPA2719AGR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Lithium-Ion battery protection circuit.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 13 mΩ MAX. (V_{GS} = –10 V, I_D = –5.0 A)
  $R_{DS(on)2}$ = 20.9 mΩ MAX. (V_{GS} = –4.5 V, I_D = –5.0 A)
- Low input capacitance
  C_{iss} = 2010 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

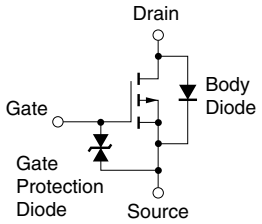
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓10	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓100	A
Total Power Dissipation Note2	P_{T1}	2	W
Total Power Dissipation Note3	P_{T2}	2	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note4	I_{AS}	–10	A
Single Avalanche Energy Note4	E_{AS}	10	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm

3. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm, PW = 10 sec

4. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = –20 → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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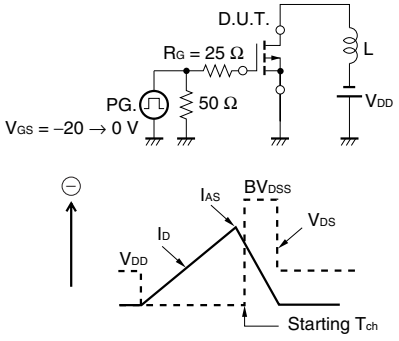
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

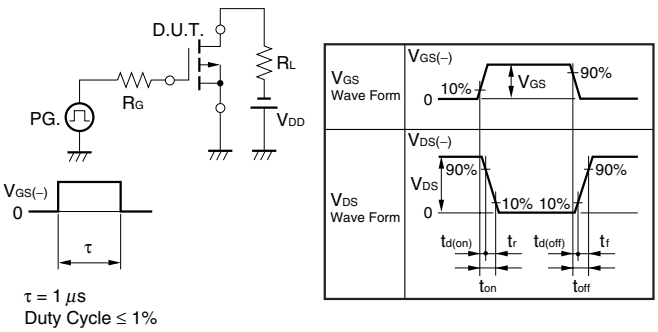
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0		–2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –5.0 A	8			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –5.0 A		10.6	13	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –5.0 A		14.2	20.9	mΩ
	$R_{DS(on)3}$	V_{GS} = –4.0 V, I_D = –5.0 A		16.6	25.5	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		2010		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		460		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		350		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –5.0 A		12		ns
Rise Time	t_r	V_{GS} = –10 V		15		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		290		ns
Fall Time	t_f			180		ns
Total Gate Charge	Q_G	V_{DD} = –24 V		43		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		5.5		nC
Gate to Drain Charge	Q_{GD}	I_D = –10 A		12		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 10 A, V_{GS} = 0 V		0.84		V
Reverse Recovery Time	t_{rr}	I_F = 10 A, V_{GS} = 0 V		105		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		6.7		nC

Note Pulsed

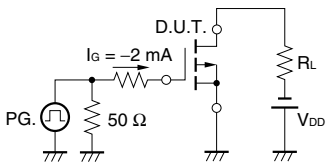
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

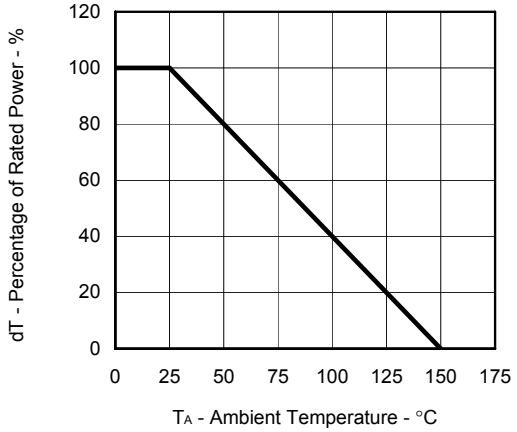


TEST CIRCUIT 3 GATE CHARGE

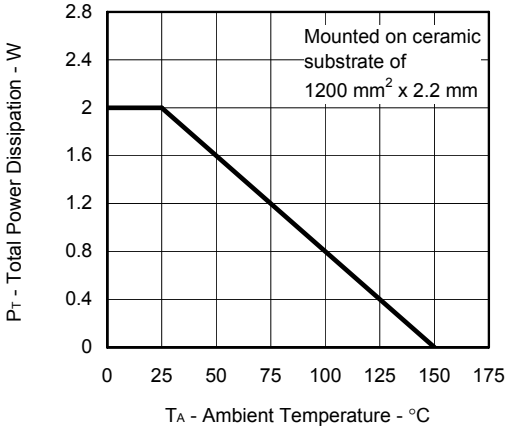


ELECTRICAL CHARACTERISTICS (T_A = 25°C)

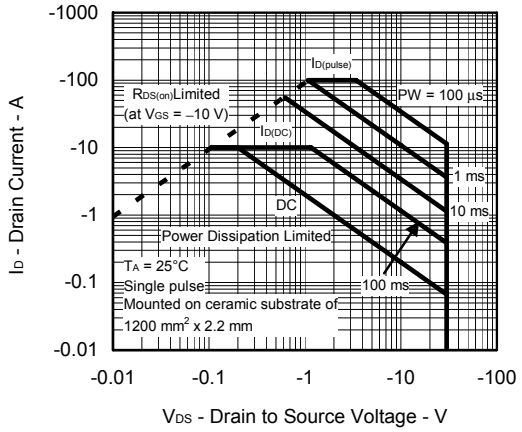
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



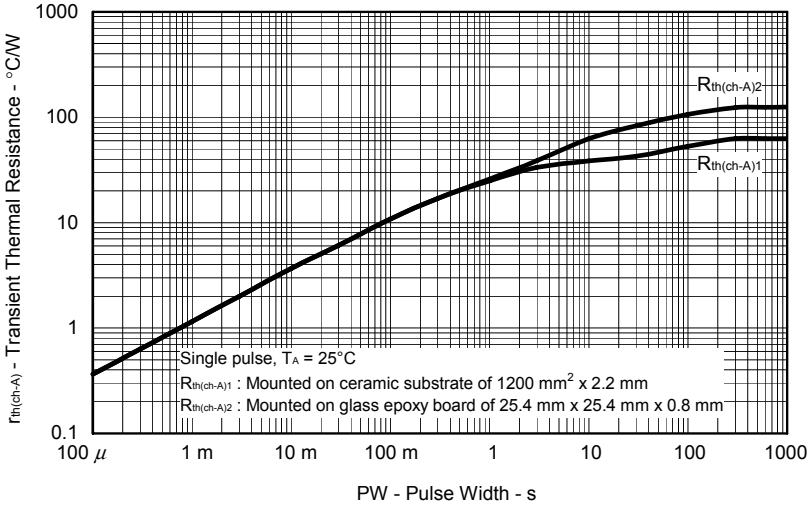
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



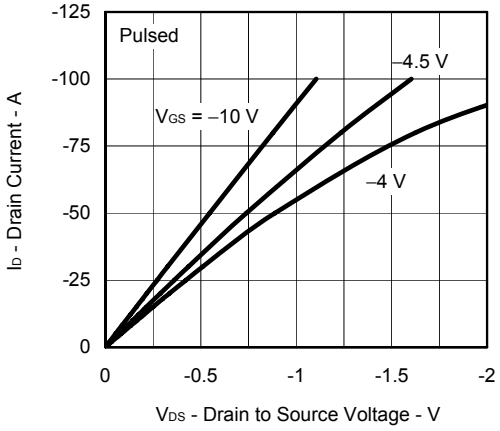
FORWARD BIAS SAFE OPERATING AREA



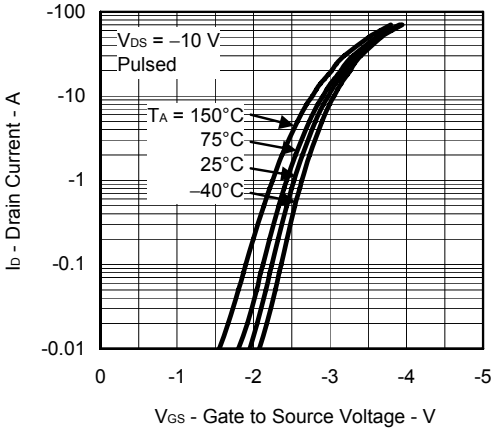
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



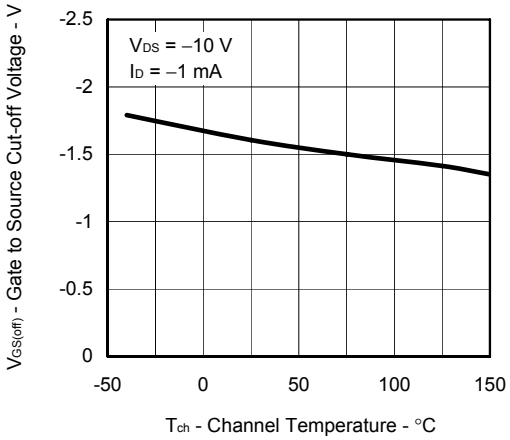
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



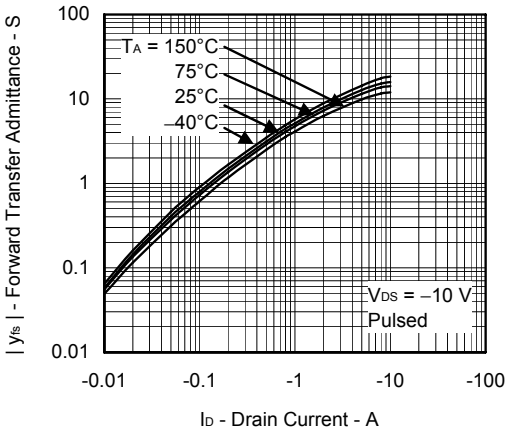
FORWARD TRANSFER CHARACTERISTICS



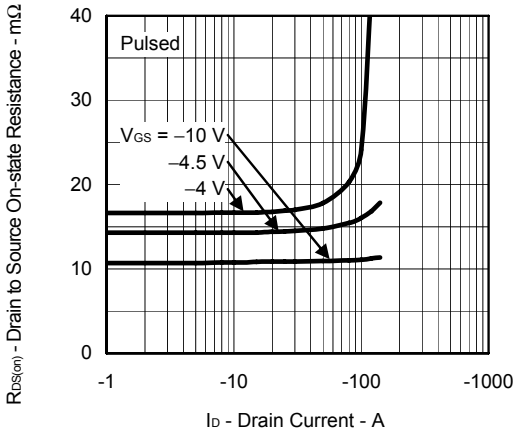
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



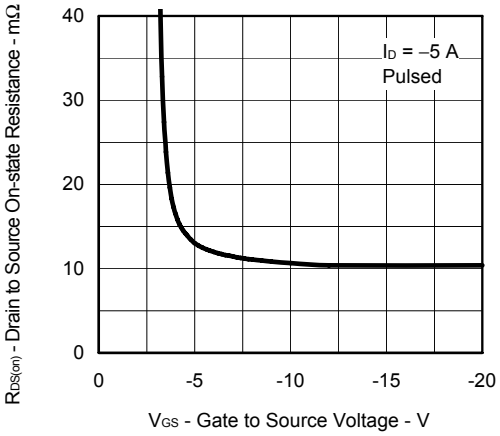
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



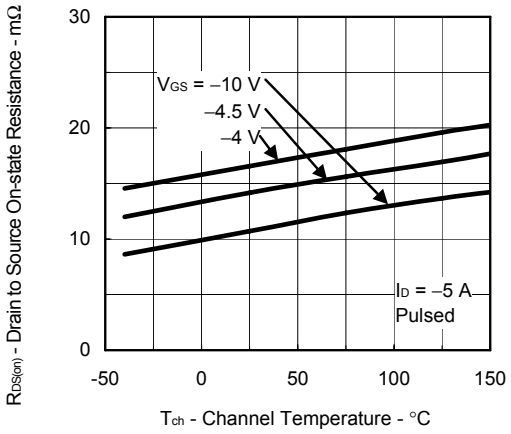
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



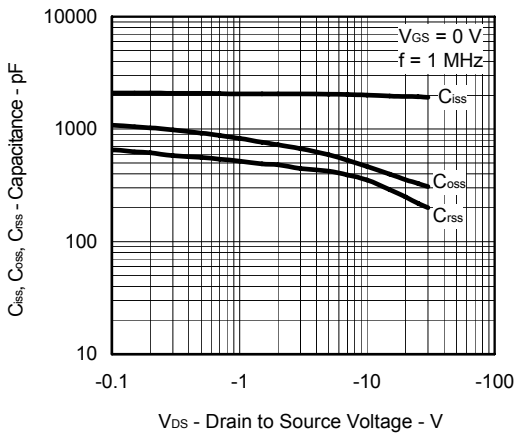
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



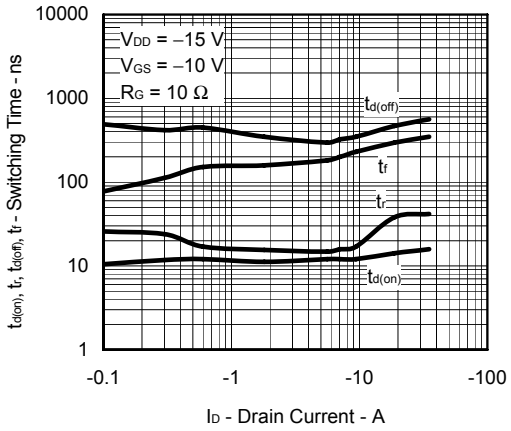
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



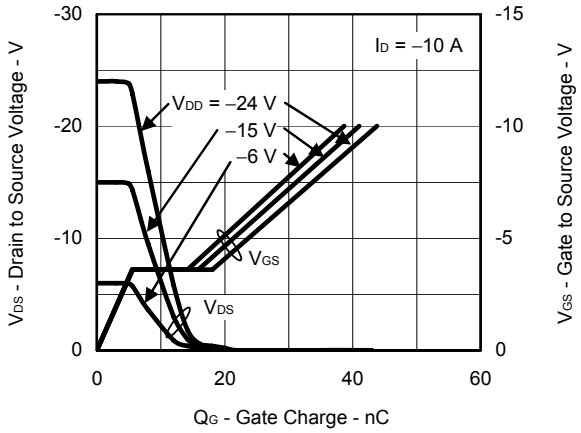
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



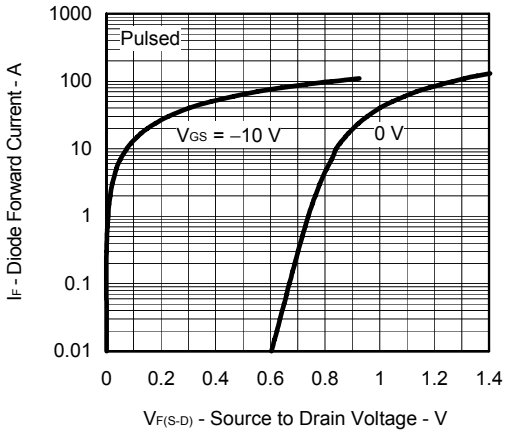
SWITCHING CHARACTERISTICS



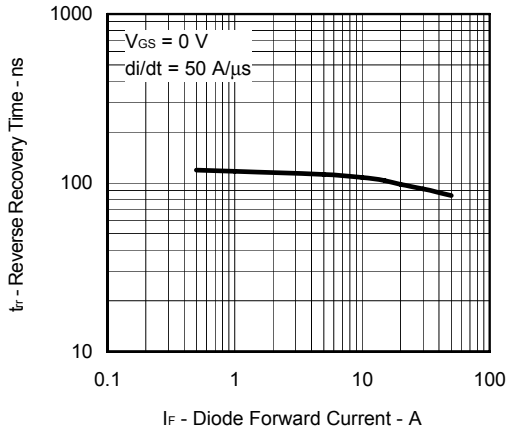
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



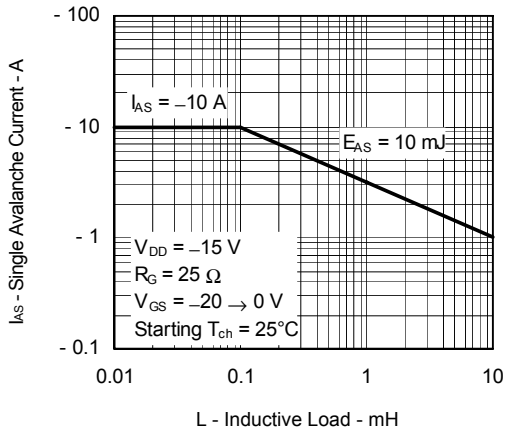
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



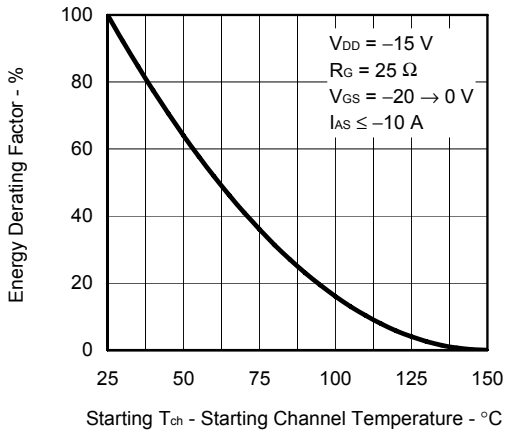
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2719AGR-E1-AT Note	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8 0.08 g TYP.
μPA2719AGR-E2-AT Note			

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

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